Linear Circuits Data Book
1989

Volume 1
Amplifiers, Comparators, and Special Functions

TEXAS INSTRUMENTS

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Information contained in this data book supersedes all data for this technology published by TI in the United States of America before January 1989.

INTRODUCTION

Texas Instruments offers an extensive line of industry-standard integrated circuits designed for applications to sense, amplify, and condition analog or digital signals.

The technologies represented by the amplifiers, comparators, and many special functions in this book include traditional bipolar through BIDFET, BIFET, IMPACT™, LinCMOS™, and Advanced LinCMOS™ processes. The IMPACT™ oxide-isolated technology provides the linear families with improved speed and power characteristics. LinCMOS™ and Advanced LinCMOS™ technologies feature a step-function improvement in impedance, speed, power requirements, and threshold stability.

This data book (Volume 1 of 3) provides information on the following types of products:

- Operational Amplifiers
- Video Amplifiers
- Voltage Comparators
- Timers
- Disk Drive Circuits for Control, Reading, or Writing
- Hall-Effect Circuits
- Current Mirrors
- Sonar Functions
- Sound Generators

These products cover the dynamic development of Linear circuits from the classical voltage converter to low-noise quad operational amplifiers. New surface-mount packages (8 to 28 leads) include both ceramic and plastic chip-carriers, and the small-outline (D) plastic packages that optimize board density with minimum impact on power-dissipation capability. Test equipment with handlers and automated assembly strengthen the production capabilities to provide an improved-cost-performance ratio. TI continues to enhance the quality and reliability of integrated circuits by improving materials, processes, test methods, and test equipment. In addition, specifications and programs are continuously updated. Quality and performance are monitored throughout all phases of manufacturing.

The alphanumeric listing in this data book includes all devices in Volumes 1, 2, and 3. Products in this data book are shown in **bold** type. The alphanumeric index provides a method of quickly locating the correct device type in this data book. The selection guide includes a functional description of each device that provides key parameter information and packaging types. Ordering information and mechanical data are in the last section of the data book.

While this volume offers design and specification data for linear circuit components only, complete technical data for any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

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We sincerely feel that the new 1989 Amplifiers and Comparators data book will be a significant addition to your library of technical literature from Texas Instruments.

Contents

General Information

noncompensated, single

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance, Bipolar	±5	±22	2	75	50	1	0.5	LM101A	FK,JG,U,W	2-13
High Performance, Low Bias Current, Bipolar	±2	±20	2	2	50	1	0.3	LM108	L	2-21
High Performance, Low Bias Current, Bipolar	±2	±20	0.5	2	80	1	0.3	LM108A	L	2-21
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL060M	JG	2-357
BIFET, General Purpose	±3.5	±18	6	0.2	25	3	13	TL080M	JG	2-403
General Purpose,Precision Input, Bipolar	±9	±18	2	200	Typ 45	1	0.3	uA709AM	J,JG,U,W	2-833
General Purpose, Bipolar	±9	±18	5	500	Typ 45	1	0.3	uA709M	J,JG,U,W	2-833
General Purpose, Bipolar	±2	±22	5	500	50	1	0.5	uA748M	JG,U	2-851

industrial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance, Bipolar	±5	±22	2	75	50	1	0.5	LM201A	D,JG,P	2-13
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL060I	D,JG,P	2-357
BIFET, Low Noise	±3.5	±18	6	200	50	3	13	TL070I	D,JG,P	2-387
BIFET, Low Power	±3.5	±18	6	400	25	3	13	TL080I	D,JG,P	2-403

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	±5	±18	7.5	250	15	1	7.5	LM301A	D,JG,P	2-13
High Performance	±2	±18	7.5	2	25	1	0.3	LM308	D,JG,P	2-21
High Performance	±2	±18	0.5	2	80	1	0.3	LM308A	D,JG,P	2-21
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL060AC	D,JG,P	2-357
BIFET, Low Power	±3.5	±18	3	0.2	4	1	3.5	TL060BC	D,JG,P	2-357
BIFET, Low Power	±3.5	±18	15	0.4	3	1	3.5	TL060C	D,JG,P	2-357
BIFET, Low Noise	±3.5	±18	6	0.2	50	3	13	TL070AC	D,JG,P	2-387
BIFET, Low Noise	±3.5	±18	10	0.2	25	3	13	TL070C	D,JG,P	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL080AC	D,JG,P	2-403
BIFET, General Purpose	±3.5	±18	15	0.4	25	3	13	TL080C	D,JG,P	2-403
General Purpose, Bipolar	±9	±18	7.5	1500	15	1	0.3	uA709C	D,JG,P	2-833
General Purpose, Bipolar	±2	±18	6	500	20	1	0.5	uA748C	D,JG,P	2-851

internally compensated, single

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	±5	±20	2	75	50	1	0.5	LM107	J,JG,U,W	2-17
Precision	±5	±22	0.015	2	450	0.8	0.25	LT1001AM	JG,L	2-63
Precision	±5	±22	0.06	4	400	0.8	0.25	LT1001M	JG,L	2-63
Low Noise, High Speed, Precision Input	±2.5	±22	0.025	35	7000	8	2.5	LT1007AM	JG,L	2-83
Low Noise, High Speed, Precision Input	±2.5	±22	0.060	55	5000	8	2.5	LT1007M	JG,P	2-83
Ultra Precision	±2.5	±20	0.035	0.1	300	0.8	2	LT1012M	L	2-123
Low Noise, High Performance	±4.5	±16	0.12	150	300	25	15	LT1028AM	D,JG,L,P	2-127
Low Noise, High Performance	±4.5	±20	0.18	300	200	25	15	LT1028M	D,JG,L,P	2-127
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±2.5	±22	0.025	35	7000	60	15	LT1037AM	JG,L	2-83
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±2.5	±22	0.060	55	5000	60	15	LT1037M	JG,L	2-83
Chopper-Stabilized	±1.9	±8	0.005	0.03	1000	1.2	4	LTC1052M	J,JG,L	5-5
Low Noise, High Speed	±3.5	±22	0.025	40	1000	8	2.8	OP-27A	JG,L	2-151
Low Noise, High Speed	±3.5	±22	0.1	80	700	8	2.8	OP-27C	JG,L	2-151
Low Noise, High Speed Noncompensated, $A_{VL} \geq 5$	±4	±22	0.025	40	1000	40	17	OP-37A	JG,L	2-151
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±4	±22	0.1	80	700	40	17	OP-37C	JG,L	2-151
Low Noise, High Performance	±3	±22	2	800	50	10	13	SE5534	FK,JG	2-181
Low Noise, High Performance	±3	±22	2	800	50	10	13	SE5534A	FK,JG	2-181
BIFET, Low Power, Precision	±3.5	±18	0.8	0.2	5	1.1	2.9	TL031AM	FK,JG,L	2-191
BIFET, Low-Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL031M	FK,JG,L	2-191
BIFET, Precision	±3.5	±18	0.8	0.2	50	3.1	20	TL051AM	FK,JG,L	2-273
BIFET, Precision	±3.5	±18	1.5	0.2	50	3.1	20	TL051M	FK,JG,L	2-273
BIFET, Low Power	±1.5	±18	6	0.2	4	1	3.5	TL061M	FK,JG,U	2-357
BIFET, Adjustable, Low-Power	±1.2	±18	6	0.2	4	1	3.5	TL066M	FK,JG	2-373
BIFET, Low Noise	±3.5	±18	6	0.2	35	3	13	TL071M	FK,JG	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	25	3	13	TL081M	FK,JG	2-403
BIFET, Low V_{IO}	±3.5	±18	3	0.4	50	3	13	TL088M	JG,U	2-417
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271M	FK,JG	2-479
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271M	FK,JG	2-479
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271M	FK,JG	2-479
LinCMOS, Low Noise, Precision	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AM	D,FK,JG,L,P	2-763

internally compensated, single

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Low Noise, Precision, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BM	D,FK,JG,L,P	2-763
LinCMOS, Low Noise, Precision	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201M	D,FK,JG,L,P	2-763
LinCMOS, Precision, Chopper Stablilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AM	D,FK,J,JG, L,N,P	2-789
LinCMOS, Precision Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652M	D,FK,J,JG, L,N,P	2-789
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AM	D,FK,J,JG, L,N,P	2-811
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	2.2	2	TLC2654M	D,FK,J,JG, L,N,P	2-811
Excalibur, High-Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021M	D,FK,JG,L,P	5-9
General Purpose	±2	±22	5	500	50	1	0.5	uA741M	FK,J,JG,U	2-837

internally compensated, single

automotive temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
High Performance	±5	±22	2	75	50	1	0.5	LM207	D,J,JG, N,P,W	2-17
High Performance	±5	±20	4	250	50	15	70	LM218	D,JG,P	2-51
Chopper-Stabilized	±1.9	±8	0.005	0.03	1000	1.2	4	LTC1052C	J,JG,L,N,P	5-5
Chopper-Stabilized	±1.9	±8	0.005	0.03	1000	1.2	4	LTC7652C	L	5-5
Low Noise, High Speed	±3.5	±22	0.025	40	1000	8	2.8	OP-27E	JG,L,P	2-151
Low Noise, High Speed	±3.5	±22	0.1	80	700	8	2.8	OP-27G	JG,L,P	2-151
Low Noise, High Speed Noncompensated, $A_{VL} \geq 5$	±4	±22	0.025	40	1000	40	17	OP-37E	JG,L,P	2-151
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±4	±22	0.1	80	700	40	17	OP-37G	JG,P	2-151
BIFET, Low Power, Precision	±3.5	±18	0.8	0.2	5	1.1	2.9	TL031AI	D,JG,L,P	2-191
BIFET, Low Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL031I	D,JG,L,P	2-191
BIFET, Precision	±3.5	±18	0.8	0.2	50	3.1	20	TL051AI	D,JG,L,P	2-273
BIFET, Precision	±3.5	±18	1.5	0.2	50	3.1	20	TL051I	D,JG,L,P	2-273
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL061I	D,JG,P	2-357
BIFET, Adjustable, Low Power	±1.2	±18	6	0.2	4	1	3.5	TL066I	D,JG,P	2-373
BIFET, Low Noise	±3.5	±18	6	0.2	50	3	13	TL071I	D,JG,P	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL081I	D,JG,P	2-403
BIFET, Low Offset Voltage	±3.5	±18	0.5	0.2	50	3	13	TL087I	D,JG,P	2-417
BIFET, Low Offset Voltage	±3.5	±18	1	0.2	50	3	13	TL088I	D,JG,P	2-417
LinCMOS, Programmable, Low Bias	4	18	5	Typ 0.007	50	0.11	0.04	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	5	Typ 0.007	25	0.64	0.56	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	5	Typ 0.007	10	2.2	4.6	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, Low Bias	4	18	2	Typ 0.007	50	0.11	0.04	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	2	Typ 0.007	25	0.64	0.56	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	2	Typ 0.007	10	2.2	4.6	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271I	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271I	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271I	D,JG,P	2-479
LinCMOS, Low Noise Precision	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AI	D,JG,L,P	2-763

internally compensated, single

automotive temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Low Noise Precision, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BI	D,JG,L,P	2-763
LinCMOS, Low Noise Precision	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201I	D,JG,L,P	2-763
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AI	D,J,JG,L,N,P	2-789
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652I	D,J,JG,L,N,P	2-789
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AI	D,J,JG,L,N,P	2-811
LinCMOS, Low Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654I	D,J,JG,L,N,P	2-811
Excalibur, High-Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021	D,FK,JG,L,P	5-9

internally compensated, single

industrial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
Chopper-Stabilized	±1.9	±8	0.005	0.03	1000	1.2	4	LTC1052C	J,JG,L,N,P	5-5
Chopper-Stabilized	±1.9	±8	0.005	0.03	1000	1.2	4	LTC7652C	L	5-5
Low Noise, High Speed	±3.5	±22	0.025	40	1000	8	2.8	OP-27E	JG,L,P	2-151
Low Noise, High Speed	±3.5	±22	0.1	80	700	8	2.8	OP-27G	JG,L,P	2-151
Low Noise, High Speed, Bipolar, Noncompensated, $A_{VL} \geq 5$	±4	±22	0.025	40	1000	40	17	OP-37E	JG,L,P	2-151
Low Noise, High Speed, Bipolar, Noncompensated, $A_{VL} \geq 5$	±4	±22	0.1	80	700	40	17	OP-37G	JG,L,P	2-151
BIFET, Low Power, Precision	±3.5	±18	0.8	0.2	5	1.1	2.9	TL031AI	D,JG,L,P	2-191
BIFET, Low Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL031I	D,JG,L,P	2-191
BIFET, Precision	±3.5	±18	0.8	0.2	50	3.1	20	TL051AI	D,JG,L,P	2-273
BIFET, Precision	±3.5	±18	1.5	0.2	50	3.1	20	TL051I	D,JG,L,P	2-273
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL061I	D,JG,P	2-357
BIFET, Adjustable, Low-Power	±1.2	±18	6	0.2	4	1	3.5	TL066I	D,JG,P	2-373
BIFET, Low Noise	±3.5	±18	6	0.2	50	3	13	TL071I	D,JG,P	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL081I	D,JG,P	2-403
BIFET, Low Offset Voltage	±3.5	±18	0.5	0.2	50	3	13	TL087I	D,JG,P	2-417
BIFET, Low Offset Voltage	±3.5	±18	1	0.2	50	3	13	TL088I	D,JG,P	2-417
Single LM324, S/S	3	30	5	−150	50	0.6	0.3	TL321I	JG,P	2-441
High Performance D/S	±1.5	±15								
LinCMOS, Programmable, Low Bias	4	18	5	Typ 0.007	50	0.11	0.04	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	5	Typ 0.007	25	0.64	0.56	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	5	Typ 0.007	10	2.2	4.6	TLC271AI	D,JG,P	2-479
LinCMOS, Programmable, Low Bias	4	18	2	Typ 0.007	50	0.11	0.04	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	2	Typ 0.007	25	0.64	0.56	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	2	Typ 0.007	10	2.2	4.6	TLC271BI	D,JG,P	2-479
LinCMOS, Programmable, Low Bias	4	18	10	Typ 0.007	50	0.11	0.04	TLC271I	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	4	18	10	Typ 0.007	25	0.64	0.56	TLC271I	D,JG,P	2-479
LinCMOS, Programmable, High Bias	4	18	10	Typ 0.007	10	2.2	4.6	TLC271I	D,JG,P	2-479
LinCMOS, Precision, Low Noise	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AI	D,JG,L,P	2-763
LinCMOS, Precision, Low Noise, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BI	D,JG,L,P	2-763
LinCMOS, Precision, Low Noise	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201I	D,JG,L,P	2-763
LinCMOS, Precision, Chopper Stabililzed	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AI	D,J,JG,L,N,P	2-789
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652I	D,J,JG, L,N,P	2-789
LinCMOS, Low-Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AI	D,J,JG, L,N,P	2-811
LinCMOS, Low-Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654I	D,J,JG, L,N,P	2-811
Excalibur, High-Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021I	D,FK,JG,L,P	5-9

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

internally compensated, single

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET	±3.5	±18	10	0.2	25	3	13	LF351	D,JG,P	2-5
BIFET	±3.5	±18	2	0.2	25	3	13	LF411C	D,JG,P	2-9
High Performance	±2	±18	7.5	250	25	1	0.5	LM307	D,J,JG, N,P,W	2-17
High Performance	±5	±20	10	250	25	15	70	LM318	D,JG,P	2-51
Precision	±5	±22	0.025	2	450	0.8	0.25	LT1001AC	JG,L,P	2-63
Precision	±5	±22	0.06	4	400	0.8	0.25	LT1001C	JG,L,P	2-63
Low Noise, High Speed, Precision Input	±2.5	±22	0.025	35	7000	8	1.7	LT1007AC	JG,P	2-83
Low Noise, High Speed, Precision Input	±2.5	±22	0.060	55	5000	8	1.7	LT1007C	JG,P	2-83
Ultra Precision	±2.5	±20	0.05	0.15	200	—	0.2	LT1012C	L,P	2-123
Low Noise, High Performance	±4.5	±18	0.08	120	500	75	15	LT1028AC	D,JG,L,P	2-127
Low Noise, High Performance	±4.5	±18	0.13	240	300	75	15	LT1028C	D,JG,L,P	2-127
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±2.5	±22	0.025	35	7000	60	15	LT1037AC	JG,P	2-83
Low Noise, High Speed, Noncompensated, $A_{VL} \geq 5$	±2.5	±22	0.060	55	5000	60	15	LT1037C	JG,P	2-83
Low Noise, High Performance	±3	±22	4	1500	25	10	13	NE5534	D,JG,P	2-181
Low Noise, High Performance	±3	±22	4	1500	25	10	13	NE5534A	D,JG,P	2-181
Ultra-Low Offset Voltage	±3	±22	0.15	7	120	0.6	0.3	OP-07C	D,JG,P	2-147
Ultra-Low Offset Voltage	±3	±22	0.15	12	120	0.6	0.3	OP-07D	D,JG,P	2-147
Ultra-Low Offset Voltage	±3	±22	0.075	4	200	0.6	0.3	OP-07E	D,JG,P	2-147

internally compensated, single

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
BIFET, Low Power, Precision	±3.5	±18	0.8	0.2	5	1.1	2.9	TL031AC	D,FK,JG,L,P	2-191
BIFET, Low Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL031C	D,FK,JG,L,P	2-191
BIFET, Precision	±3.5	±18	0.8	0.2	50	3.1	20	TL051AC	D,FK,JG,L,P	2-273
BIFET, Precision	±3.5	±18	1.5	0.2	50	3.1	20	TL051C	D,FK,JG,L,P	2-273
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL061AC	D,JG,P	2-357
BIFET, Low Power	±3.5	±18	3	0.2	4	1	3.5	TL061BC	D,JG,P	2-357
BIFET, Low Power	±3.5	±18	15	0.2	3	1	3.5	TL061C	D,JG,P	2-357
BIFET, Adjustable, Low-Power	±1.2	±18	6	0.2	4	1	3.5	TL066AC	D,JG,P	2-373
BIFET, Adjustable, Low-Power	±1.2	±18	3	0.2	4	1	3.5	TL066BC	D,JG,P	2-373
BIFET, Adjustable, Low-Power	±1.2	±18	15	0.4	3	1	3.5	TL066C	D,JG,P	2-373
BIFET, Low Noise	±3.5	±18	6	0.2	50	3	13	TL071AC	D,JG,P	2-387
BIFET, Low Noise	±3.5	±18	3	0.2	50	3	13	TL071BC	D,JG,P	2-387
BIFET, Low Noise	±3.5	±18	10	0.2	25	3	13	TL071C	D,JG,P	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL081AC	D,JG,P	2-403
BIFET, General Purpose	±3.5	±18	3	0.2	50	3	13	TL081BC	D,JG,P	2-403
BIFET, General Purpose	±3.5	±18	15	0.4	25	3	13	TL081C	D,JG,P	2-403
BIFET, Low V_{IO}	±3.5	±18	0.5	0.2	50	3	13	TL087C	D,JG,L,P	2-417
BIFET, Low V_{IO}	±3.5	±18	1	0.2	50	3	13	TL088C	D,JG,L,P	2-417
Single LM324, High Performance S/S	3	30	7	−250	25	0.6	0.3	TL321C	JG,P	2-441
Single LM324, High Performance D/S	1.5	15								
LinCMOS, Programmable, Low Bias	1.4	18	5	Typ 0.001	30	0.1	0.04	TLC251AC	D,JG,P	2-451
LinCMOS, Programmable, Medium Bias	1.4	18	5	Typ 0.001	20	0.7	0.6	TLC251AC	D,JG,P	2-451
LinCMOS, Programmable, High Bias	1.4	18	5	Typ 0.001	10	2.3	4.5	TLC251AC	D,JG,P	2-451
LinCMOS, Programmable, Low Bias	1.4	18	2	Typ 0.001	30	0.1	0.04	TLC251BC	D,JG,P	2-451
LinCMOS, Programmable, Medium Bias	1.4	18	2	Typ 0.001	20	0.7	0.6	TLC251BC	D,JG,P	2-451
LinCMOS, Programmable, High Bias	1.4	18	2	Typ 0.001	10	2.3	4.5	TLC251BC	D,JG,P	2-451
LinCMOS, Programmable, Low Bias	1.4	18	10	Typ 0.001	30	0.1	0.04	TLC251C	D,JG,P	2-451
LinCMOS, Programmable, Medium Bias	1.4	18	10	Typ 0.001	20	0.7	0.6	TLC251C	D,JG,P	2-451
LinCMOS, Programmable, High Bias	1.4	18	10	Typ 0.001	10	2.3	4.5	TLC251C	D,JG,P	2-451
LinCMOS, Programmable, Low Bias	3	18	5	Typ 0.007	50	0.11	0.04	TLC271AC	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	3	18	5	Typ 0.007	25	0.64	0.56	TLC271AC	D,JG,P	2-479
LinCMOS, Programmable, High Bias	3	18	5	Typ 0.007	10	2.2	4.6	TLC271AC	D,JG,P	2-479

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

internally compensated, single

commercial temperature range **(Values specified for T_A = 25°C**

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, Programmable, Low Bias	3	18	2	Typ 0.007	50	0.11	0.04	TLC271BC	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	3	18	2	Typ 0.007	25	0.64	0.56	TLC271BC	D,JG,P	2-479
LinCMOS, Programmable, High Bias	3	18	2	Typ 0.007	10	2.2	4.6	TLC271BC	D,JG,P	2-479
LinCMOS, Programmable, Low Bias	3	18	10	Typ 0.007	50	0.11	0.04	TLC271C	D,JG,P	2-479
LinCMOS, Programmable, Medium Bias	3	18	10	Typ 0.007	25	0.64	0.56	TLC271C	D,JG,P	2-479
LinCMOS, Programmable, High Bias	3	18	10	Typ 0.007	10	2.2	4.6	TLC271C	D,JG,P	2-479
LinCMOS, Precision, Low Noise	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201AC	D,JG,L,P	2-763
LinCMOS, Precision, Low Noise, 100% Noise Tested	4.6	16	0.2	Typ 0.001	400	1.9	2.7	TLC2201BC	D,JG,L,P	2-763
LinCMOS, Precision, Low Noise	4.6	16	0.5	Typ 0.001	400	1.9	2.7	TLC2201C	D,JG,L,P	2-763
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.001	Typ 0.004	5600	1.9	2.8	TLC2652AC	D,J,JG,L,N,P	2-789
LinCMOS, Precision, Chopper Stabilized	3.8	16	0.003	Typ 0.004	1000	1.9	2.8	TLC2652C	D,J,JG,L,N,P	2-789
LinCMOS, Low-Noise, Precision, Chopper Stabilized	4.6	16	0.01	Typ 0.05	5600	1.9	2	TLC2654AC	D,J,JG,L,N,P	2-811
LinCMOS, Low-Noise, Precision, Chopper Stabilized	4.6	16	0.02	Typ 0.05	1000	1.9	2	TLC2654C	D,J,JG,L,N,P	2-811
Excalibur, High-Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2021C	D,FK,JG,L,P	5-9
General Purpose	±2	±18	6	500	20	1	0.5	uA741C	D,JG,P	2-837

internally compensated, dual

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
High Gain, Low Power, Bipolar	S/S	3	30	5	−150	50	0.6	0.2	LM158	FK,JG,U	2-43
	D/S	±1.5	±15								
General Purpose		±2	±22	5	500	50	1	0.5	MC1558	FK,JG,U	2-133
Precision		±5	±22	0.15	20	1500	0.7	0.4	LT1013AM	JG,L	5-3
Precision		±5	±22	0.3	30	1200	0.7	0.4	LT1013M	JG,L	5-3
High Performance		±4	±22	5	500	50	3.5	1.7	RM4558	JG	2-177
Low Power		±2	±22	5	100	1	0.5	0.5	TL022M	U	2-187
BIFET, Low Power, Precision		±3.5	±18	0.8	0.2	5	1.1	2.9	TL032AM	FK,JG,L	2-219
BIFET, Low Power, Precision		±3.5	±18	1.5	0.2	5	1.1	2.9	TL032M	FK,JG,L	2-219
BIFET, Precision		±3.5	±18	0.8	0.2	50	3	16	TL052AM	FK,JG,L	2-299
BIFET, Precision		±3.5	±18	1.5	0.2	50	3	16	TL052M	FK,JG,L	2-299
BIFET, Low Power		±3.5	±18	6	0.2	4	1	3.5	TL062M	FK,JG,U	2-357
BIFET, Low Noise		±3.5	±18	6	0.2	35	3	13	TL072M	FK,JG	2-387
BIFET, General Purpose		±3.5	±18	16	0.2	25	3	13	TL082M	FK,JG	2-403
BIFET, General Purpose		±3.5	±18	6	0.2	25	3	13	TL083M	FK,J	2-403
BIFET, General Purpose		±3.5	±18	3	0.4	50	3	13	TL287M	JG,U	2-417
BIFET, General Purpose		±3.5	±18	3	0.4	50	3	13	TL288M	JG,U	2-417
LinCMOS, High Bias		4	18	10	Typ 0.005	10	2.2	5.3	TLC272M	FK,JG	2-543
LinCMOS, High Bias		4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277M	FK,JG	2-543
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2M	FK,JG	2-607
LinCMOS, Low Bias		4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7M	FK,JG	2-607
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2M	FK,JG	2-671
LinCMOS, Medium Bias		4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7M	FK,JG	2-671
LinCMOS, Micro Power, Precision		4	18	0.6	Typ 0.007	500	0.11	0.5	TLC1078M	FK,JG	2-735
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2022M	FK,JG,L	5-9

internally compensated, dual

automotive temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
High Gain, Low Power, Bipolar	S/S	3	30	5	−150	50	0.6	0.2	LM258	D,JG,P,U	2-43
	D/S	±1.5	±1.5								
High Gain, Low Power, Bipolar	S/S	3	30	3	−80	50	0.6	0.2	LM258A	D,JG,P,U	2-43
	D/S	±1.5	±1.5								
High Gain, Low Power, Bipolar	S/S	3	26	7	−250	Typ 100	0.6	0.2	LM2904	D,JG,P,U	2-43
	D/S	±1.5	±13								
High Performance		±4	±18	6	−500	20	3	1.7	RV4558	D,JG,P	2-177
BIFET, Low Power, Precision		±3.5	±18	0.8	0.2	5	1.1	2.9	TL032AI	D,JG,L,P	2-219
BIFET, Low Power, Precision		±3.5	±18	1.5	0.2	5	1.1	2.9	TL032I	D,JG,L,P	2-219
BIFET, Precision		±3.5	±18	0.8	0.2	50	3	16	TL052AI	D,JG,L,P	2-299
BIFET, Precision		±3.5	±18	1.5	0.2	50	3	16	TL052I	D,JG,L,P	2-299
BIFET, Low Power		±3.5	±18	6	0.2	4	1	3.5	TL062I	D,JG,P	2-357
BIFET, Low Noise		±3.5	±18	6	0.2	50	3	13	TL072I	D,JG,P	2-387
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL082I	D,JG,P	2-403
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL083I	D,JG,P	2-403
BIFET, General Purpose		±3.5	±18	0.5	0.2	50	3	13	TL287I	D,JG,P	2-417
BIFET, General Purpose		±3.5	±18	1	0.2	50	3	13	TL288I	D,JG,P	2-417
Low Power		±1.5	±18	8	−500	20	1	0.6	TL322I	D,JG,P	2-445
LinCMOS, High Bias		4	18	5	Typ 0.005	10	2.2	5.3	TLC272AI	D,JG,P	2-543
LinCMOS, High Bias		4	18	2	Typ 0.005	10	2.2	5.3	TLC272BI	D,JG,P	2-543
LinCMOS, High Bias		4	18	10	Typ 0.005	10	2.2	5.3	TLC272I	D,JG,P	2-543
LinCMOS, High Bias		4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277I	D,JG,P	2-543
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AI	D,JG,P	2-607
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BI	D,JG,P	2-607
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2I	D,JG,P	2-607
LinCMOS, Low Bias		4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7I	D,JG,P	2-607
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AI	D,JG,P	2-671
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BI	D,JG,P	2-671
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2I	D,JG,P	2-671
LinCMOS, Medium Bias		4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7I	D,JG,P	2-671
LinCMOS, Micro Power, Precision		4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078I	D,JG,P	2-735
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2022I	D,JG,L,P	5-9

internally compensated, dual

industrial temperature range

(Values specified for T_A = 25°C

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET, Low Power, Precision	±3.5	±18	0.8	0.2	5	1.1	2.9	TL032AI	D,JG,L,P	2-219
BIFET, Low Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL032I	D,JG,L,P	2-219
BIFET, Precision	±3.5	±18	0.8	0.2	50	3	16	TL052AI	D,JG,L,P	2-299
BIFET, Precision	±3.5	±18	1.5	0.2	50	3	16	TL052I	D,JG,L,P	2-299
BIFET, Low Power	±3.5	±18	6	0.2	4	1	3.5	TL062I	D,JG,P	2-357
BIFET, Low Noise	±3.5	±18	6	0.2	50	3	13	TL072I	D,JG,P	2-387
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL082I	D,JG,P	2-403
BIFET, General Purpose	±3.5	±18	6	0.2	50	3	13	TL083I	D,JG,P	2-403
BIFET, General Purpose	±3.5	±18	0.5	0.2	50	3	13	TL287I	D,JG,P	2-417
BIFET, General Purpose	±3.5	±18	1	0.2	50	3	13	TL288I	D,JG,P	2-417
Low Power	±1.5	±18	8	-500	20	1	0.6	TL322I	D,JG,P	2-445
LinCMOS, High Bias	4	18	5	Typ 0.005	10	2.2	5.3	TLC272AI	D,JG,P	2-543
LinCMOS, High Bias	4	18	2	Typ 0.005	10	2.2	5.3	TLC272BI	D,JG,P	2-543
LinCMOS, High Bias	4	18	10	Typ 0.005	10	2.2	5.3	TLC272I	D,JG,P	2-543
LinCMOS, High Bias	4	18	0.5	Typ 0.005	10	2.2	5.3	TLC277I	D,JG,P	2-543
LinCMOS, Low Bias	4	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AI	D,JG,P	2-607
LinCMOS, Low Bias	4	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BI	D,JG,P	2-607
LinCMOS, Low Bias	4	18	10	Typ 0.005	50	0.1	0.05	TLC27L2I	D,JG,P	2-607
LinCMOS, Low Bias	4	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7I	D,JG,P	2-607
LinCMOS, Medium Bias	4	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AI	D,JG,P	2-671
LinCMOS, Medium Bias	4	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BI	D,JG,P	2-671
LinCMOS, Medium Bias	4	18	10	Typ 0.005	25	0.6	0.6	TLC27M2I	D,JG,P	2-671
LinCMOS, Medium Bias	4	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7I	D,JG,P	2-671
LinCMOS, Micro Power, Precision	4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078I	D,JG.P	2-735
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2022I	D,JG,L,P	5-9

internally compensated, dual

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
BIFET, General Purpose		±3.5	±18	10	0.2	25	3	13	LF353	D,JG,P	2-7
BIFET, Low Offset		±3.5	±18	3	0.2	25	3	13	LF412C	D,JG,P	2-11
High Gain, Low Power, Bipolar	S/S	3	30	7	−250	25	0.6	0.2	LM358	D,JG,P,U	2-43
	D/S	±1.5	±15								
High Gain, Low Power, Bipolar	S/S	3	30	3	−100	25	0.6	0.2	LM358A	D,JG,P,U	2-43
	D/S	±1.5	±15								
Precision		±5	±22	0.15	20	1500	0.7	0.4	LT1013AC	JG,L,P	5-3
Precision		±5	±22	0.3	30	1200	0.7	0.4	LT1013C	JG,L,P	5-3
Precision		±5	±22	0.8	30	1200	0.7	0.4	LT1013D	D,JG,L,P	5-3
General Purpose		±1.5	±18	6	500	20	1	0.5	MC1458	D,JG,P,U	2-133
Low Noise		±3	±20	4	800	25	10	9	NE5532	JG,P	2-143
Low Noise		±3	±20	4	800	25	10	9	NE5532A	JG,P	2-143
High Performance		±4	±18	6	500	20	3	1.7	RC4558	D,JG,P	2-177
High Performance		±4	±18	6	250	20	4	2	RC4559	D,P	2-171
Low Power		±2	±18	5	250	1	0.5	0.5	TL022C	D,JG,P	2-187
BIFET, Low Power, Precision		±3.5	±18	0.8	0.2	5	1.1	2.9	TL032AC	D,JG,L,P	2-219
BIFET, Low Power, Precision		±3.5	±18	1.5	0.2	5	1.1	2.9	TL032C	D,JG,L,P	2-219
BIFET, Precision		±3.5	±18	1.5	0.2	50	3	16	TL052AC	D,JG,L,P	2-299
BIFET, Precision		±3.5	±18	4	0.2	50	3	16	TL052C	D,JG,L,P	2-299
BIFET, Low Power		±3.5	±18	6	0.2	4	1	3.5	TL062AC	D,JG,P	2-357
BIFET, Low Power		±3.5	±18	3	0.2	4	1	3.5	TL062BC	D,JG,P	2-357
BIFET, Low Power		±3.5	±18	15	0.4	3	1	3.5	TL062C	D,JG,P	2-357
BIFET, Low Noise		±3.5	±18	6	0.2	50	3	13	TL072AC	D,JG,P	2-387
BIFET, Low Noise		±3.5	±18	3	0.2	50	3	13	TL072BC	D,JG,P	2-387
BIFET, Low Noise		±3.5	±18	10	0.2	25	3	13	TL072C	D,JG,P	2-387
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL082AC	D,JG,P	2-403
BIFET, General Purpose		±3.5	±18	3	0.2	50	3	13	TL082BC	D,JG,P	2-403
BIFET, General Purpose		±3.5	±18	15	0.4	25	3	13	TL082C	D,JG,P	2-403
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL083AC	D,JG,N	2-403

internally compensated, dual

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
BIFET, General Purpose	±3.5	±18	15	0.4	25	3	13	TL083C	D,JG,N	2-403
BIFET, General Purpose	±3.5	±18	0.5	0.2	50	3	13	TL287C	D,JG,P	2-417
BIFET, General Purpose	±3.5	±18	1	0.2	50	3	13	TL288C	D,JG,P	2-417
Low Power	±1.5	±18	10	−500	20	1	0.6	TL322C	D,JG,P	2-445
LinCMOS, High Bias	1.4	18	5	Typ 0.005	10	2.2	5.3	TLC252AC	D,JG,P	2-461
LinCMOS, High Bias	1.4	18	2	Typ 0.005	10	2.2	5.3	TLC252BC	D,JG,P	2-461
LinCMOS, High Bias	1.4	18	10	Typ 0.005	10	2.2	5.3	TLC252C	D,JG,P	2-461
LinCMOS, Low Bias	1.4	18	5	Typ 0.005	30	0.1	0.05	TLC25L2AC	D,JG,P	2-461
LinCMOS, Low Bias	1.4	18	2	Typ 0.005	30	0.1	0.05	TLC25L2BC	D,JG,P	2-461
LinCMOS, Low Bias	1.4	18	10	Typ 0.005	30	0.1	0.05	TLC25L2C	D,JG,P	2-461
LinCMOS, Medium Bias	1.4	18	5	Typ 0.005	20	0.6	0.6	TLC25M2AC	D,JG,P	2-461
LinCMOS, Medium Bias	1.4	18	2	Typ 0.005	20	0.6	0.6	TLC25M2BC	D,JG,P	2-461
LinCMOS, Medium Bias	1.4	18	10	Typ 0.005	20	0.6	0.6	TLC25M2C	D,JG,P	2-461
LinCMOS, High Bias	3	18	5	Typ 0.005	10	2.2	5.3	TLC272AC	D,JG,P	2-543
LinCMOS, High Bias	3	18	2	Typ 0.005	10	2.2	5.3	TLC272BC	D,JG,P	2-543
LinCMOS, High Bias	3	18	10	Typ 0.005	10	2.2	5.3	TLC272C	D,JG,P	2-543
LinCMOS, High Bias	3	18	0.5	Typ 0.005	10	2.2	5.3	TLC277C	D,JG,P	2-543
LinCMOS, Low Bias	3	18	5	Typ 0.005	50	0.1	0.05	TLC27L2AC	D,JG,P	2-607
LinCMOS, Low Bias	3	18	2	Typ 0.005	50	0.1	0.05	TLC27L2BC	D,JG,P	2-607
LinCMOS, Low Bias	3	18	10	Typ 0.005	50	0.1	0.05	TLC27L2C	D,JG,P	2-607
LinCMOS, Low Bias	3	18	0.5	Typ 0.005	50	0.1	0.05	TLC27L7C	D,JG,P	2-607
LinCMOS, Medium Bias	3	18	5	Typ 0.005	25	0.6	0.6	TLC27M2AC	D,JG,P	2-671
LinCMOS, Medium Bias	3	18	2	Typ 0.005	25	0.6	0.6	TLC27M2BC	D,JG,P	2-671
LinCMOS, Medium Bias	3	18	10	Typ 0.005	25	0.6	0.6	TLC27M2C	D,JG,P	2-671
LinCMOS, Medium Bias	3	18	0.5	Typ 0.005	25	0.6	0.6	TLC27M7C	D,JG,P	2-671
LinCMOS, Micro Power, Precision	1.4	18	0.6	Typ 0.007	500	0.11	0.05	TLC1078C	D,JG,P	2-735
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2022C	D,JG,L,P	5-9
General Purpose	±5	±22	6	500	25	1	0.5	uA747C	D,J,N	2-845

internally compensated, quad

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
General Purpose	3	30	5	−150	50	0.6	0.13	LM124	FK,J,W	2-33
General Purpose	±4	±22	5	100	50	1	0.5	LM148	FK,J	2-39
QUAD uA741, High Performance	±4	±22	4	400	50	3.5	1.7	RM4136	FK,J,W	2-173
BIFET, Low Power, Precision	±3.5	±18	1.5	0.2	5	1.1	2.9	TL034AM	FK,J	2-245
BIFET, Low Power, Precision	±3.5	±18	4	0.2	5	1.1	2.9	TL034M	FK,J	2-245
Low Power	±2	±22	5	100	72	0.5	0.5	TL044M	FK,J,W	2-269
BIFET, Precision	±3.5	±18	1.5	0.2	50	2.7	16	TL054AM	FK,J	2-327
BIFET, Precision	±3.5	±18	4	0.2	50	2.7	16	TL054M	FK,J	2-327
BIFET, Low Power	±3.5	±18	9	0.2	4	1	3.5	TL064M	FK,J,W	2-357
BIFET, Low Noise	±3.5	±18	9	0.2	35	3	13	TL074M	FK,J,W	2-387
BIFET, General Purpose	±3.5	±18	9	0.2	25	3	13	TL084M	FK,J,W	2-403
LinCMOS, High Bias	4	18	10	Typ 0.005	10	2.2	5.3	TLC274M	FK,J	2-575
LinCMOS, High Bias	4	18	1.2	Typ 0.005	10	2.2	5.3	TLC279M	FK,J	2-575
LinCMOS, Low Bias	4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4M	FK,J	2-639
LinCMOS, Low Bias	4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9M	FK,J	2-639
LinCMOS, Medium Bias	4	18	10	Typ 0.005	20	0.6	0.6	TLC27M4M	FK,J	2-703
LinCMOS, Medium Bias	4	18	0.9	Typ 0.005	20	0.6	0.6	TLC27M9M	FK,J	2-703
LinCMOS, Micro Power, Precision	4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079M	D,JG,P	2-749
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2024M	FK,J	5-9

internally compensated, quad

automotive temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
Norton Amplifier, Bipolar	S/S	4.5	32	—	200	1.2	2.5	0.5	LM2900	J,N	2-55
	D/S	±2.2	±16								
Extended Temperature Range LM324		3	26	7	−250	Typ 100	0.6	0.3	LM2902	D,J,N,W	2-33
Low Power, Bipolar	S/S	3	36	8	−500	20	1	0.6	MC3303	D,J,N	2-137
	D/S	±1.5	±18								
Quad uA741		±4.5	±18	6	500	20	3	1.7	RV4136	D,J,N,W	2-173
BIFET, Low Power, Precision		±3.5	±18	1.5	0.2	5	1.1	2.9	TL034AI	D,J,N	2-245
BIFET, Low Power, Precision		±3.5	±18	4	0.2	5	1.1	2.9	TL034I	D,J,N	2-245
BIFET, Precision		±3.5	±18	1.5	0.2	50	2.7	16	TL054AI	D,J,N	2-327
BIFET, Precision		±3.5	±18	4	0.2	50	2.7	16	TL054I	D,J,N	2-327
BIFET, Low Power, Precision		±3.5	±18	6	0.2	4	1	3.5	TL064I	D,J,N	2-357
BIFET, Low Noise, Precision		±3.5	±18	6	0.2	50	3	13	TL074I	D,J,N	2-387
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL084I	D,J,N	2-403
LinCMOS, High Bias		4	18	5	Typ 0.001	10	2.2	5.3	TLC274AI	D,J,N	2-575
LinCMOS, High Bias		4	18	2	Typ 0.001	10	2.2	5.3	TLC274BI	D,J,N	2-575
LinCMOS, High Bias		4	18	10	Typ 0.001	10	2.2	5.3	TLC274I	D,J,N	2-575
LinCMOS, High Bias		4	18	1.2	Typ 0.005	10	2.2	5.3	TLC279I	D,J,N	2-575
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AI	D,J,N	2-639
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BI	D,J,N	2-639
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4I	D,J,N	2-639
LinCMOS, Low Bias		4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9I	D,J,N	2-639
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AI	D,J,N	2-703
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BI	D,J,N	2-703
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M4I	D,J,N	2-703
LinCMOS, Medium Bias		4	18	0.9	Typ 0.005	25	0.6	0.6	TLC27M9I	D,J,N	2-703
LinCMOS, Micro Power, Precision		4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079I	D,JG,P	2-749
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2024I	DW,FK,J,N	5-9

internally compensated, quad

industrial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
		MIN	MAX	MAX	MAX	MIN	TYP	TYP			
General Purpose, Bipolar		3	30	5	−150	50	0.6	0.3	LM224	D,J,N,W	2-33
General Purpose, Bipolar		3	30	3	−80	50	0.6	0.3	LM224A	D,J,N,W	2-33
General Purpose, Bipolar		±4	±18	6	200	25	1	0.5	LM248	D,J,N	2-39
High Gain, Low Power, Bipolar	S/S	3	32	5	−150	50	0.6	0.2	LM258	D,J,N	2-43
	D/S	±1.5	±22								
High Gain, Low Power, Bipolar	S/S	3	32	3	−80	50	0.6	0.2	LM258A	D,J,N	2-43
	D/S	±1.5	±22								
Single Supply, Norton Amplifier, Bipolar	S/S	4	32	—	200	1.2	2.5	0.5	LM2900	D,J,N	2-55
	D/S	±2	±16								
BIFET, Low Power		±3.5	±18	1.5	0.2	5	1.1	2.9	TL034AI	D,J,N	2-245
BIFET, Low Power		±3.5	±18	4	0.2	5	1.1	2.9	TL034I	D,J,N	2-245
BIFET, Precision		±3.5	±18	1.5	0.2	50	2.7	16	TL054AI	D,J,N	2-327
BIFET, Precision		±3.5	±18	4	0.2	50	2.7	16	TL054I	D,J,N	2-327
BIFET, Low Power, Precision		±3.5	±18	6	0.2	4	1	3.5	TL064I	D,J,N	2-357
BIFET, Low Noise, Precision		±3.5	±18	6	0.2	50	3	13	TL074I	D,J,N	2-387
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL084I	D,J,N	2-403
LinCMOS, High Bias		4	18	5	Typ 0.001	10	2.2	5.3	TLC274AI	D,J,N	2-575
LinCMOS, High Bias		4	18	2	Typ 0.001	10	2.2	5.3	TLC274BI	D,J,N	2-575
LinCMOS, High Bias		4	18	10	Typ 0.001	10	2.2	5.3	TLC274I	D,J,N	2-575
LinCMOS, High Bias		4	18	0.9	Typ 0.005	10	2.2	5.3	TLC279I	D,J,N	2-575
LinCMOS, Low Bias		4	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AI	D,J,N	2-639
LinCMOS, Low Bias		4	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BI	D,J,N	2-639
LinCMOS, Low Bias		4	18	10	Typ 0.005	50	0.1	0.05	TLC27L4I	D,J,N	2-639
LinCMOS, Low Bias		4	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9I	D,J,N	2-639
LinCMOS, Medium Bias		4	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AI	D,J,N	2-703
LinCMOS, Medium Bias		4	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BI	D,J,N	2-703
LinCMOS, Medium Bias		4	18	10	Typ 0.005	25	0.6	0.6	TLC27M4I	D,J,N	2-703
LinCMOS, Medium Bias		4	18	0.9	Typ 0.005	25	0.6	0.6	TLC27M9I	D,J,N	2-703
LinCMOS, Micro Power, Precision		4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079I	D,JG,P	2-749
Excalibur, High Speed, Precision		4	40	0.5	25	1000	2	0.9	TLE2024I	DW,FK,J,N	5-9

internally compensated, quad

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION		SUPPLY VOLTAGE (V) MIN	SUPPLY VOLTAGE (V) MAX	V_{IO} (mV) MAX	I_{IB} (nA) MAX	A_{VD} (V/mV) MIN	B_1 (MHz) TYP	SR (V/μs) TYP	TYPE	PACKAGES	PAGE NO.
BIFET, General Purpose		±3.5	±18	10	0.2	25	3	13	LF347	D,J,N	2-3
General Purpose		3	30	7	−250	25	0.6	0.3	LM324	D,J,N,W	2-33
General Purpose		3	30	3	−100	25	0.6	0.3	LM324A	D,J,N,W	2-33
General Purpose		±4	±18	6	200	25	1	0.5	LM348	D,J,N	2-39
Single Supply, Norton Amplifier, Bipolar	S/S	4	32	–	200	1.2	2.5	0.5	LM3900	D,J,N	2-55
	D/S	±2	±16								
Low Power, Bipolar	S/S	3	36	10	−500	20	1	0.6	MC3403	D,J,N	2-137
	D/S	±1.5	±18								
Quad uA741, High Performance		±4	±18	6	500	20	3	1.7	RC4136	D,J,N,W	2-173
BIFET, Low Power, Precision		±3.5	±18	1.5	0.2	5	1.1	2.9	TL034AC	D,J,N	2-245
BIFET, Low Power, Precision		±3.5	±18	4	0.2	5	1.1	2.9	TL034C	D,J,N	2-245
General Purpose		±2	±18	5	250	60	0.5	0.5	TL044C	J,N,W	2-269
BIFET, Precision		±3.5	±18	1.5	0.2	50	2.7	16	TL054AC	D,J,N	2-327
BIFET, Precision		±3.5	±18	4	0.2	50	2.7	16	TL054C	D,J,N	2-327
BIFET, Low Power		±3.5	±18	6	0.2	4	1	3.5	TL064AC	D,J,N	2-357
BIFET, Low Power		±3.5	±18	3	0.2	4	1	3.5	TL064BC	D,J,N	2-357
BIFET, Low Power		±3.5	±18	15	0.4	3	1	3.5	TL064C	D,J,N	2-357
BIFET, Low Noise		±3.5	±18	6	0.2	50	3	13	TL074AC	D,J,N	2-387
BIFET, Low Noise		±3.5	±18	3	0.2	50	3	13	TL074BC	D,J,N	2-387
BIFET, Low Noise		±3.5	±18	10	0.2	50	3	13	TL074C	D,J,N	2-387
BIFET, Low Noise		±3.5	±18	10	0.2	25	3	13	TL075C	J,N	2-387
BIFET, General Purpose		±3.5	±18	6	0.2	50	3	13	TL084AC	D,J,N	2-403
BIFET, General Purpose		±3.5	±18	3	0.2	50	3	13	TL084BC	D,J,N	2-403
BIFET, General Purpose		±3.5	±18	15	0.4	25	3	13	TL084C	D,J,N	2-403
BIFET, General Purpose		±3.5	±18	15	0.4	25	3	13	TL085C	J,N	2-403
High Performance, Bipolar		±4	±18	6	500	20	3	2	TL136C	N	2-437
LinCMOS, High Bias		1.4	18	5	Typ 0.005	10	2.2	5.3	TLC254AC	D,J,N	2-469
LinCMOS, High Bias		1.4	18	2	Typ 0.005	10	2.2	5.3	TLC254BC	D,J,N	2-469
LinCMOS, High Bias		1.4	18	10	Typ 0.005	10	2.2	5.3	TLC254C	D,J,N	2-469
LinCMOS, Low Bias		1.4	18	5	Typ 0.005	30	0.1	0.05	TLC25L4AC	D,J,N	2-469
LinCMOS, Low Bias		1.4	18	2	Typ 0.005	30	0.1	0.05	TLC25L4BC	D,J,N	2-469
LinCMOS, Low Bias		1.4	18	10	Typ 0.005	30	0.1	0.05	TLC25L4C	D,J,N	2-469
LinCMOS, Medium Bias		1.4	18	5	Typ 0.005	20	0.6	0.6	TLC25M4AC	D,J,N	2-469
LinCMOS, Medium Bias		1.4	18	2	Typ 0.005	20	0.6	0.6	TLC25M4BC	D,J,N	2-469
LinCMOS, Medium Bias		1.4	18	10	Typ 0.005	20	0.6	0.6	TLC25M4C	D,J,N	2-469

internally compensated, quad

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (nA)	A_{VD} (V/mV)	B_1 (MHz)	SR (V/μs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	MAX	MIN	TYP	TYP			
LinCMOS, High Bias	3	18	5	Typ 0.005	10	2.2	5.3	TLC274AC	D,J,N	2-575
LinCMOS, High Bias	3	18	2	Typ 0.005	10	2.2	5.3	TLC274BC	D,J,N	2-575
LinCMOS, High Bias	3	18	10	Typ 0.005	10	2.2	5.3	TLC274C	D,J,N	2-575
LinCMOS, High Bias	3	18	0.9	Typ 0.005	10	2.2	5.3	TLC279C	D,J,N	2-575
LinCMOS, Low Bias	3	18	5	Typ 0.005	50	0.1	0.05	TLC27L4AC	D,J,N	2-639
LinCMOS, Low Bias	3	18	2	Typ 0.005	50	0.1	0.05	TLC27L4BC	D,J,N	2-639
LinCMOS, Low Bias	3	18	10	Typ 0.005	50	0.1	0.05	TLC27L4C	D,J,N	2-639
LinCMOS, Low Bias	3	18	0.9	Typ 0.005	50	0.1	0.05	TLC27L9C	D,J,N	2-639
LinCMOS, Medium Bias	3	18	5	Typ 0.005	25	0.6	0.6	TLC27M4AC	D,J,N	2-703
LinCMOS, Medium Bias	3	18	2	Typ 0.005	25	0.6	0.6	TLC27M4BC	D,J,N	2-703
LinCMOS, Medium Bias	3	18	10	Typ 0.005	25	0.6	0.6	TLC27M4C	D,J,N	2-703
LinCMOS, Medium Bias	3	18	0.9	Typ 0.005	25	0.7	0.6	TLC27M9C	D,J,N	2-703
LinCMOS, Micro Power, Precision	1.4	18	1.15	Typ 0.007	500	0.11	0.05	TLC1079C	D,J,N	2-749
Excalibur, High Speed, Precision	4	40	0.5	25	1000	2	0.9	TLE2024C	DW,FK,J,N	5-9

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

ADVANCED LINEAR DEVICES	SUGGESTED TI REPLACEMENT	PAGE NO.
ALD1701 or ALD1702 or ALD1703	TLC271	2-479

ANALOG DEVICES	SUGGESTED TI REPLACEMENT	PAGE NO.
AD510 or AD517	OP-07	2-147

FAIRCHILD	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
uA714		OP-07C	2-147
uA714E		OP-07E	2-147
uA714L		OP-07D1	2-147
uA741	uA741		2-837
uA747	uA747		2-845
uA748	uA748		2-851
uA771		TLO71	2-387
uA771A		TLO71B or TLO81B	2-387
uA771B		TLO71A or TLO81A	2-387
uA771L		TLO81	2-403
uA772		TLO72	2-387
uA772A		TLO72B	2-387
uA772B		TLO72A or TLO82A	2-387
uA772L		TLO82	2-403
uA774		TLO74	2-387
uA774B		TLO74A or TLO74B	2-387
uA774L		TLO84	2-403

GENERAL ELECTRIC	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612, or ICL7613	TLC271	2-479
ICL7621	TLC272	2-543
ICL7641	TLC274 or TLC27L9	2-575
ICL7642	TLC27M9	2-703

HARRIS	SUGGESTED TI REPLACEMENT	PAGE NO.
HA2515	LM318	2-51
HA5130-5	OP-07E	2-147
HA5135-5	OP-07C	2-147

INTERSIL	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612, or ICL7613	TLC271	2-479
ICL7621	TLC272	2-543
ICL7641	TLC274 or TLC27L9	2-575
ICL7642	TLC27M9	2-703

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LT1001		OP-07C, OP-07D, or OP-07E	2-147
LT1007	LT1007		2-83
LT1007A	LT1007A		2-83
LT1037	LT1037		2-83
LT1037A	LT1037A		2-83

MAXIM	SUGGESTED TI REPLACEMENT	PAGE NO.
ICL7611, or ICL7612, or ICL7613	TLC271	2-479
ICL7621	TLC272	2-543
ICL7641	TLC274 or TLC27L9	2-575
ICL7642	TLC27M9	2-703

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC748	uA748		2-851
MC1458	MC1458		2-133
MC1558	MC1558		2-133
MC1709	uA709		2-833
MC1741	uA741		2-837
MC1747	uA747		2-845
MC3303	MC3303		2-137
MC3403	MC3403	RC4136	2-137
MC4558	RC4558		2-177
MC4741	LM348		2-39
MC34001		TL071 or LF351	2-387
MC34002		TL072 or LF353	2-387
MC34004		TL074 or LF347	2-387
MC34004B		TL074A or LF347B	2-387

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LF347	LF347	TL074 or TL084	2-3
LF347B	LF347B	TL074A, TL074B, or TL084A	2-3
LF351	LF351	TL071 or TL081A	2-5
LF353	LF353	TL072, TL072A, or TL082A	2-7
LF411	LF411	TL081A	2-9
LF411A		TL071A, TL071B, TL081A, or TL081B	2-387 2-403
LF412	LF412	TL072A, TL082A, or TL082B	2-11
LF441		TL061	2-357
LF441A		TL061A or TL061B	2-357
LF442		TL062	2-357
LF442A		TL062B	2-357
LF444		TL064	2-357
LF444A		TL064A	2-357
LH0044		OP-07C	2-147
LH0044B		OP-07D	2-147
LH0044C		OP-07E	2-147
LM201A	LM201A		2-13
LM207	LM207		2-17
LM218	LM218		2-51
LM224	LM224		2-33
LM248	LM248		2-39
LM258	LM258		2-43

(Continued)

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM301A	LM301A		2-13
LM307	LM307		2-17
LM318	LM318		2-51
LM324	LM324		2-33
LM348	LM348		2-39
LM358	LM358		2-43
LM709	uA709		2-833
LM741	uA741		2-837
LM883		RC4558	2-177
LM1458	MC1458		2-133
LM2900	LM2900		2-55
LM2902	LM2902		2-33
LM2904	LM2904		2-43
LM3900	LM3900		2-55
LMC660		TLC274	2-575

NEC	SUGGESTED TI REPLACEMENT	PAGE NO.
uPC159	LM318	2-51
uPC251	MC1458	2-133
uPC354	OP-07	2-147
uPC801	TL071, TL081A, or LF351	2-387

PMI	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
OP-02		uA741	2-837
OP-04		uA747	2-845
OP-07C	OP-07C		2-147
OP-07D	OP-07D		2-147
OP-07E	OP-07E		2-147
OP-07F		RC4136	2-173
OP-14C or OP-14E		MC1458	2-133
OP-14J		MC1558	2-133
OP-15F		TL071, TL081A, or LF351	2-387
OP-27E	OP-27E		2-151
OP-27G	OP-27G		2-151
OP-37E	OP-37E		2-151
OP-37G	OP-37G		2-151
OP-215F		TL072, TL082A, or LF353	2-387

RAYTHEON	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
RC4136	RC4136		2-173
RC4156		LM348	2-39
RC4157		LM348	2-39
RC4558	RC4558		2-177
RC4559	RC4559		2-171

RCA	SUGGESTED TI REPLACEMENT	PAGE NO.
CA081A	TL081	2-403
CA081A	TL081A	2-403
CA082	TL082	2-403
CA082A	TL082A	2-403
CA084	TL084	2-403

SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
NE532		LM358 or TL022	2-43
NE5532	NE5532		2-143
NE5532A	NE5532A		2-143
NE5534	NE5534		2-181
NE5534A	NE5534A		2-181
SE5534	SE5534		2-181
SE5534A	SE5534A		2-181

SGS-THOMSON	SUGGESTED TI REPLACEMENT	PAGE NO.
TS271	TLC271	2-479
TS271A	TLC271A	2-479
TS271B	TLC271B	2-479
TS272	TLC272	2-543
TS272A	TLC272A	2-543
TS272B	TLC272B	2-543
TS274	TLC274	2-575
TS274A	TLC274A	2-575
TS274B	TLC274B	2-575
TS27L2	TLC27L2	2-607
TS27L2A	TLC27L2A	2-607
TS27L2B	TLC27L2B	2-607
TS27L4	TLC27L4	2-639
TS27L4A	TLC27L4A	2-639
TS27L4B	TLC27L4B	2-639
TS27M2	TLC27M2	2-671
TS27M2A	TLC27M2A	2-671
TS27M2B	TLC27M2B	2-671
TS27M4	TLC27M4	2-703
TS27M4A	TLC27M4A	2-703
TS27M4B	TLC27M4B	2-703

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to zero or other level, if specified.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left[\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at zero volts.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left[\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at zero volts.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the amplifier to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Maximum Peak Output Voltage Swing (V_{OM})

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP})

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent d-c output voltage is zero.

Large-Signal Voltage Amplification (A_V)

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output voltage to the change in differential input voltage producing it.

Maximum-Output-Swing Bandwidth (B_{OM})

The range of frequencies within which the maximum output voltage swing is above a specified value.

Unity-Gain Bandwidth (B_1)

The range of frequencies within which the open-loop voltage amplification is greater than unity.

Phase Margin (ϕ_m)

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

Gain Margin (A_m)

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

Input Resistance (r_i)

The resistance between the input terminals with either input grounded.

Differential Input Resistance (r_{id})

The small-signal resistance between the two ungrounded input terminals.

Output Resistance (r_o)

The resistance between the output terminal and ground.

Input Capacitance (C_i)

The capacitance between the input terminals with either input grounded.

Common-Mode Input Impedance (z_{ic})

The parallel sum of the small-signal impedance between each input terminal and ground.

Output Impedance (z_o)

The small-signal impedance between the output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Sensitivity (k_{SVS}, $\Delta V_{IO}/\Delta V_{CC}$)

The absolute value of the ratio of the change in input offset voltage to the change in supply voltages producing it.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage rejection ratio.

Supply Voltage Rejection Ratio (k_{SVR}, $\Delta V_{CC}/\Delta V_{IO}$)

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.
NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

Equivalent Input Noise Voltage (V_n)

The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Equivalent Input Noise Current (I_n)

The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

Average Noise Figure ($\overline{F}$)

The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature, T_O, at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency band.

Short-Circuit Output Current (I_{OS})

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.

Supply Current (I_{CC})

The current into the V_{CC} or V_{CC+} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

Crosstalk Attenuation (V_{o1}/V_{o2})

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

Rise Time (t_r)

The time required for an output voltage step to change from 10% to 90% of its final value.

Total Response Time (Settling Time) (t_{tot})

The time between a step-function change of the input signal level and the instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\epsilon$) containing the final output signal level.

Overshoot Factor

The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal, to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

Slew Rate (SR)

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.

military temperature range

(Values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (uA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
single channel									
Strobe	4–30	0	3	0.1	8	115	LM111	FK,J,JG,U	3-3
Ultra Low Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP111	FK,JG	3-29
Strobe	4–30	0	1.5	0.05	50	150	LT1011M	JG,L	3-37
Strobe	4–30	0	0.5	0.025	50	150	LT1011AM	JG,L	3-37
Ultra-Fast, Precision	5	–5	±2	10	10	10	LT1016M	JG,L	3-61
dual channel									
Low Power, Bipolar	4–30	0	5	0.1	6	300	LM193	FK,JG,L	3-21
Dual TL510M	12	–6	2	15	2	30	TL514M	FK,J,W	3-69
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352M	FK,JG	3-103
High Speed, LinCMOS	4–18	0	10	†	6	200	TLC372M	FK,JG	3-119
Ultra Low Power, Open-Drain Output	4–18	0	5	†	6	1100	TLC393M	FK,JG	3-135
Ultra Low Power, Push-Pull Output	4–18	0	5	†	4	1300	TLC3702M	FK,JG	3-151
quad channel									
Low Power, Bipolar	4–30	0	5	–0.1	6	300	LM139	FK,J	3-17
Precision Input	4–30	0	2	–0.1	6	300	LM139A	FK,J	3-17
Ultra Low Power, Open-Drain Output	4–18	0	5	†	6	1100	TLC339M	FK,J	3-89
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354M	FK,J	3-111
High Speed, LinCMOS	4–18	0	10	†	6	200	TLC374M	FK,J	3-127
Ultra Low Power, Push-Pull Output	4–18	0	5	†	4	1300	TLC3704M	FK,J	3-157

† Typically 5 pA

automotive temperature range

(Values specified at T_A = 25°C)

dual channel

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (uA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
Automotive LM393	4–30	0	7	0.25	6	300	LM2903	D,JG,P	3-21
Ultra-Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352I	D,JG,P	3-103
High Speed, LinCMOS	3–18	0	10	†	6	200	TLC372I	D,JG,P	3-119
Ultra Low Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC393I	D,JG,P	3-135
Ultra Low Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3702I	D,JG,P	3-151

quad channel

Automotive Temp. LM339	4–30	0	7	−0.25	6	300	LM2901	D,J,N	3-17
Low-Cost LM2901	4–26	0	20	0.5	6	300	LM3302	D,J,N	3-25
Ultra Low Power, Automotive LP339, Bipolar	5	0	±5	−0.025	20	8000	LP2901	D,J,N	3-33
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354I	D,J,N	3-111
Open-Drain Output	3–18	0	5	†	6	1100	TLC339I	D,J,N	3-89
High Speed, LinCMOS	3–18	0	10	†	6	200	TLC374I	D,J,N	3-127
Push-Pull Output	3–18	0	5	†	4	1300	TLC3704I	D,J,N	3-157

† Typically 5 pA

industrial temperature range

(Values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (uA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGE	PAGE NO.
single channel									
Strobe	4–30	0	3	0.1	8	115	LM211	D,JG,P	3-3
Ultra Low Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP211	D,JG,P	3-29
Single LM339	4–30	0	5	−0.1	6	300	TL331I	D,JG,P	3-65
dual channel									
Industrial LM393	4–30	0	5	0.25	6	300	LM293	D,JG,P	3-21
Industrial LM393, Low Offset	4–30	0	2	0.25	6	300	LM293A	D,JG,P	3-21
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352I	D,JG,P	3-103
High Speed, LinCMOS	3–18	0	10	†	6	200	TLC372I	D,JG,P	3-119
Ultra Low Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC393I	D,JG,P	3-135
Ultra Low Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3702I	D,JG,P	3-151
quad channel									
Industrial LM339	4–30	0	5	−0.25	6	300	LM239	D,J,N	3-17
Industrial LM339, Low Offset	4–30	0	2	−0.25	6	300	LM239A	D,J,N	3-17
Ultra Low Power, Industrial LP339, Bipolar	4–30	0	±5	−0.025	20	8000	LP239	D,J,N	3-33
Ultra Low Power, Open-Drain Output	3–18	0	5	†	6	1100	TLC339I	D,J,N	3-89
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354I	D,J,N	3-111
High Speed, LinCMOS	3–18	0	10	†	6	200	TLC374I	D,J,N	3-127
Ultra Low Power, Push-Pull Output	3–18	0	5	†	4	1300	TLC3704I	D,J,N	3-157

† Typically 5 pA

commercial temperature range

(Values specified at T_A = 25°C)

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (uA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYP	PACKAGE	PAGE NO.
single channel									
Strobe	4–30	0	7.5	0.25	8	115	LM311	D,JG,P	3-3
Ultra Low Power, Strobe	4–30	0	7.5	0.1	1.6	1200	LP311	D,JG,P	3-29
Strobe	4–30	0	0.5	0.025	50	150	LT1011AC	JG,L,P	3-37
Strobe	4–30	0	1.5	0.05	50	150	LT1011C	JG,L,P	3-37
Ultra-Fast Precision	5	−5	±3	10	10	10	LT1016C	D,JG,L,P	3-61
Single LM339	4–30	0	5	−0.25	6	300	TL331C	D,JG,P	3-65
Output Enable	5	0	±1	–	MAX 16	25	TL712	D,JG,P	3-77
High Speed	5	0	–	–	MAX 16	7	TL714C	D,P	3-81
High Speed	0	−5.2	±1	–	MAX 16	Max 12	TL721	D,JG,P	3-85
dual channel									
Low Power, Bipolar	4–30	0	5	0.25	6	300	LM393	D,JG,P	3-21
Precision Input	4–30	0	2	0.25	6	300	LM393A	D,JG,P	3-21
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC352C	D,JG,P	3-103
High Speed, LinCMOS	3–18	0	10	†	6	200	TLC372C	D,JG,P	3-119
Ultra Low Power, Open Drain Output, CMOS	3–18	0	5	†	6	1100	TLC393C	D,JG,P	3-135
Ultra Low Power, Push-Pull Output, CMOS	3–18	0	5	†	4	1300	TLC3702C	D,JG,P	3-151

† Typically 5 pA

commercial temperature range **(Values specified at T_A = 25°C)**

DESCRIPTION	POWER SUPPLY V_{CC+} NOM (V)	POWER SUPPLY V_{CC-} NOM (V)	V_{IO} MAX (mV)	I_{IB} MAX (uA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYP	PACKAGE	PAGE NO.
quad channel									
Low Power, Bipolar	4–30	0	5	−0.25	6	300	LM339	D,J,N	3-17
Precision Input	4–30	0	2	−0.25	6	300	LM339A	D,J,N	3-17
Ultra Low Power, Bipolar	4–30	0	±5	−0.025	6	8000	LP339	D,J,N	3-33
Ultra Low Power, Open-Drain Output, CMOS	3–18	0	5	†	6	1100	TLC339C	D,J,N	3-89
Ultra Low Supply, LinCMOS	1.4–18	0	10	†	6	200	TLC354C	D,J,N	3-111
High Speed, CMOS	3–18	0	10	†	6	200	TLC374C	D,J,N	3-127
Ultra Low Power, Push-Pull Output, CMOS	3–18	0	5	†	4	1300	TLC3704C	D,J,N	3-157

† Typically 5 pA

Replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained herein.

Manufacturers are arranged in alphabetical order.

LINEAR TECHNOLOGY	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LT1011A	LT1011A		3-37
LT1011	LT1011		3-37
LT1016	LT1016		3-61
LT1017		TLC352, TLC392, or TLC3702	3-103 3-151
LT1018		TLC352, TLC392, or TLC3702	3-103 3-151

NATIONAL	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
LM311	LM311		3-3
LM339	LM339	TLC339	3-17
LM393	LM393	TLC393	3-21
LM2901	LM2901	TLC339	3-17
LM3302	LM3302		3-25
LP339	LP339	TLC339	3-33

PMI	SUGGESTED TI REPLACEMENT	PAGE NO.
CMP04F	LM339 or	3-17
	LM3302 or	3-25
	LM2901 or	3-17
	TLC339	3-89

Input Offset Voltage (V_{IO})

The d-c voltage that must be applied between the input terminals to force the quiescent d-c output voltage to the specified level.

Average Temperature Coefficient of Input Offset Voltage (α_{VIO})

The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{VIO} = \left[\frac{(V_{IO} @ T_{A(1)}) - (V_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Offset Current (I_{IO})

The difference between the currents into the two input terminals with the output at the specified level.

Average Temperature Coefficient of Input Offset Current (α_{IIO})

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \left[\frac{(I_{IO} @ T_{A(1)}) - (I_{IO} @ T_{A(2)})}{T_{A(1)} - T_{A(2)}}\right]$$ where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

Input Bias Current (I_{IB})

The average of the currents into the two input terminals with the output at the specified level.

High-Level Strobe Current ($I_{IH(S)}$)

The current flowing into or out of* the strobe at a high-level voltage.

Low-Level Strobe Current ($I_{IL(S)}$)

The current flowing out of* the strobe at a low-level voltage.

High-Level Strobe Voltage ($V_{IH(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed not to interfere with the operation of the comparator.

Low-Level Strobe Voltage ($V_{IL(S)}$)

For a device having an active-low strobe, a voltage within the range that is guaranteed to force the output high or low, as specified, independently of the differential inputs.

Input Voltage Range (V_I)

The range of voltage that if exceeded at either input terminal will cause the comparator to cease functioning properly.

Common-Mode Input Voltage (V_{IC})

The average of the two input voltages.

*Current out of a terminal is given as a negative value.

Common-Mode Input Voltage Range (V_{ICR})

The range of common-mode input voltage that if exceeded will cause the comparator to cease functioning properly.

Differential Input Voltage (V_{ID})

The voltage at the noninverting input with respect to the inverting input.

Differential Input Voltage Range (V_{ID})

The range of voltage between the two input terminals that if exceeded will cause the comparator to cease functioning properly.

Differential Voltage Amplification (A_{VD})

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant.

High-Level Output Voltage (V_{OH})

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Voltage (V_{OL})

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

High-Level Output Current, (I_{OH})

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-Level Output Current, (I_{OL})

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Output Resistance (r_o)

The resistance between an output terminal and ground.

Common-Mode Rejection Ratio (k_{CMR}, CMRR)

The ratio of differential voltage amplification to common-mode voltage amplification.
NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Current (I_{CC+}, I_{CC-})

The current into* the V_{CC+} or V_{CC-} terminal of an integrated circuit.

Total Power Dissipation (P_D)

The total d-c power supplied to the device less any power delivered from the device to a load.
NOTE: At no load: $P_D = V_{CC+} \cdot I_{CC+} + V_{CC-} \cdot I_{CC-}$.

*Current out of a terminal is given as a negative value.

Response Time

The interval between the application of an input step function and the instant the output crosses the logic threshold voltage.

NOTE: The input step drives the comparator from some initial condition sufficient to saturate the output (or in the case of high-to-low-level response time, to turn the output off) to an input level just barely in excess of that required to bring the output back to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Strobe Release Time

The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from its active logic level to its inactive logic level.

*Current out of a terminal is given as a negative value.

precision timers

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	1 μs	Hours	SE555	FK,JG	4-37
Single Timer, Bipolar	±200 mA	1 μs	Hours	SE555C	FK,JG	4-37
Dual Timer, Bipolar	±200 mA	1 μs	Hours	SE556	FK,J	4-49
Dual Timer, Bipolar	±200 mA	1 μs	Hours	SE556C	FK,J	4-49
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC555M	FK,JG	4-195
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC556M	FK,J	4-203

automotive temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	10 μs	Hours	SA555	D,JG,P	4-37
Dual Timer, Bipolar	±200 mA	10 μs	Hours	SA556	D,J,N	4-49
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC555I	D,JG,P	4-195
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC556I	D,J,N	4-203

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	OUTPUT CURRENT	TIMING		TYPE	PACKAGES	PAGE NO.
		FROM	TO			
Single Timer, Bipolar	±200 mA	10 μs	Hours	NE555	D,JG,P	4-37
Dual Timer, Bipolar	±200 mA	10 μs	Hours	NE556	D,J,N	4-49
LinCMOS, Single High-Speed Timer, 1-Volt Operation	100 mA −10 mA	1 μs	Hours	TLC551C	D,P	4-179
LinCMOS, Dual High-Speed Timer, 1-Volt Operation	100 mA −10 mA	1 μs	Hours	TLC552C	D,N	4-187
LinCMOS, Single High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC555C	D,JG,P	4-195
LinCMOS, Dual High-Speed Timer	100 mA −10 mA	1 μs	Hours	TLC556C	D,J,N	4-203
Programmable Timer/Counter	4 mA	10 μs	Days	uA2240C	N	4-221

current mirrors

(Values specified for T_A = 25°C)

DESCRIPTION	TEMPERATURE RANGE	CURRENT RATIO INPUT TO OUTPUT	INPUT CURRENT RANGE	TYPE	PACKAGES	PAGE NO.
Programmable	0°C to 70°C	3:1 to 1:15	Variable	TL010C	P	4-81
Programmable	−40°C to 85°C	3:1 to 1:15	Variable	TL010I	P	4-81
Fixed	0°C to 70°C	1:1	1 μA to 1 mA	TL011C	LP	4-85
Fixed	−40°C to 85°C	1:1	1 μA to 1 mA	TL011I	LP	4-85
Fixed	0°C to 70°C	1:2	1 μA to 1 mA	TL012C	LP	4-85
Fixed	−40°C to 85°C	1:2	1 μA to 1 mA	TL012I	LP	4-85
Fixed	0°C to 70°C	1:4	1 μA to 1 mA	TL014AC	LP	4-85
Fixed	0°C to 70°C	1:2	2 μA to 2 mA	TL021C	LP	4-85
Fixed	−40°C to 85°C	1:2	2 μA to 2 mA	TL021I	LP	4-85

Hall-Effect switches

(Values specified for T_A = 25°C)

RELEASE POINT (GAUSS) MIN	OPERATING POINT (GAUSS) MAX	MINIMUM HYSTERESIS (GAUSS)	TYPE	PACKAGES	PAGE NO.
−250	250	50	TL170C	LP	4-121
100	600	230	TL172C	LP	4-123
25	450	30	TL3013C	LU	4-165
125	500	50	TL3019C	LU	4-167
50	350	20	TL3020C	LU	4-169
−250	250	50	TL3101	LU	4-171

Hall-Effect linear circuits

(Values specified for T_A = 25°C)

LINEAR RANGE (GAUSS)	SENSITIVITY (mV/GAUSS)	TYPE	PACKAGES	PAGE NO.
±500	1.4	TL173	LP	4-125
±500	1.4	TL3103	LU	4-173

sonar ranging functions

(Values specified for T_A = 25°C)

DESCRIPTION		TYPE	PACKAGES	PAGE NO.
Sonar Ranging Module	Sonar ranging module for measuring distances from a range of 6 inches to 35 feet using the TL851 and TL852	SN28827		4-61
Sonar Ranging Module	Sonar ranging module for measuring distances from a range of 6 inches to 35 feet using the TL852 and TL853	SN28828		4-67
Controller Circuit	Control integrated circuit for use in a sonar ranging module, capable of driving 50-kHz transducers with a simple interface	TL851	N	4-151
Receiver Circuit	Receiver integrated circuit for use in a sonar ranging module	TL852	N	4-155
Control Circuit	Control integrated circuit for use in a sonar ranging module, capable of driving 40-kHz transducers with a simple interface	TL853	N	4-161

floppy-disk control circuits

(Values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
Read-Amplifier System	MC3470 MC3470A	N	4-29
Tape-Read Signal Conditioner	TL041C	DW,NT	4-113
Disk-Memory Read-Chain Data Comparator	TL712	D,JG,P	3-77
Disk-Memory Read-Chain Data Comparator with MECL III and MECL 1000	TL721	D,JG,P	3-85

differential video amplifiers

military temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	BAND-WIDTH (MHz)	GAIN	TYPICAL NOISE, V_n	TYPE	PACKAGES	PAGE NO.
Amplifier with internal frequency compensation and adjustable/selectable gain options	90	600 Max	12 μV	SE592	D,N	4-53
Amplifier with internal frequency compensation	200	10, 100, 400	12 μV	uA733M	J,U	4-213

commercial temperature range

(Values specified for T_A = 25°C)

DESCRIPTION	BAND-WIDTH (MHz)	GAIN	TYPICAL NOISE, V_n	TYPE	PACKAGES	PAGE NO.
Amplifier with 2 multiplexed inputs and wide AGC range	60	100 max	25 μV	MC1445	J,N	4-27
Amplifier with internal frequency compensation and adjustable/selectable gain options	90	600 max	12 μV	NE592	D,N	4-53
Similar to NE592 but with tighter gain distribution	90	600 max	12 μV	NE592A	D,N	4-53
Amplifier with a wide AGC range	50	100	12 μV	TL026C	D,P	4-91
Amplifier with a wide AGC range	50	400 max	12 μV	TL027C	D,J,N	4-99
2-channel multiplexed Video Amp	20	600 max	<5 μV	TL040C	D,N	4-107
Similar to NE592 but in an 8-pin package	90	600 max	12 μV	TL592	D,P	4-143
Similar to NE592A but in an 8-pin package	90	600 max	12 μV	TL592A	D,P	4-143
Low-noise version of NE592 and TL592	90	600 max	3 μV	TL592B	D,N,P	4-147
Amplifier with internal frequency compensation	200	10, 100, 400	12 μV	uA733C	D,N	4-213

logarithmic amplifiers

military temperature range

(Values specified for operating temperature range)

DESCRIPTION	BANDWIDTH	GAIN	TYPE	PACKAGES	PAGE NO.
Logarithmic Amplifier	40 MHz	Logarithmic Curve	TL441AM	J,FK	4-129

programmable tone/noise generators

(Values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
• Complex sound generators designed to provide low-cost digital tones or noise. • Programmable white-noise and attenuation functions, and simultaneous sounds under microprocessor control. • TTL compatible.	SN76494/ SN76494A SN76496/ SN76496A	N	4-73

frequency-to-voltage-converters

(Values specified for T_A = 25°C)

DESCRIPTION	TYPE	PACKAGES	PAGE NO.
• Output swings to ground for zero-frequency input • Only one RC network provides frequency doubling for low ripple. • 8-pin version interfaces directly to variable reluctance magnetic pickups.	LM2907 LM2917	D,N,P	4-21

sample-and-hold amplifiers

military temperature range

(Values specified for operating temperature range)

DESCRIPTION	OFFSET VOLTAGE	GAIN ERROR	TYPE	PACKAGES	PAGE NO.
Precision Sample-and-Hold Amplifier	1 mV	0.002%	LF198	L	4-3
	0.5 mV	0.001%	LF198A		

commercial temperature range

(Values specified for operating temperature range)

DESCRIPTION	OFFSET VOLTAGE	GAIN ERROR	TYPE	PACKAGES	PAGE NO.
Precision Sample-and-Hold Amplifier	2 mV	0.004%	LF398	JG,L	4-3
	1 mV	0.001%	LF398A	L,P	4-3

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

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Manufacturers are arranged in alphabetical order.

INTERSIL		SUGGESTED TI REPLACEMENT	PAGE NO.
ICM7555		TLC555	4-195

MOTOROLA	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
MC1445	MC1445		4-27
MC1733		uA733	4-213
MC3470	MC3470		4-29
NE555	NE555		4-37
NE592	NE592		4-53

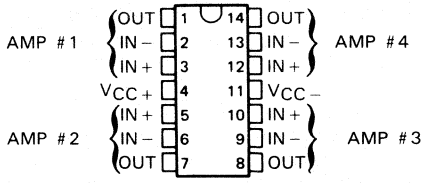
SIGNETICS	DIRECT TI REPLACEMENT	SUGGESTED TI REPLACEMENT	PAGE NO.
NE555	NE555	TLC555	4-195
NE556	NE556	TLC556	4-203
NE592	NE592		4-53
SA555	SA555	TLC555	4-195
SA556	SA556	TLC556	4-203
SE555	SE555	TLC555	4-195
SE555C	SE555C	TLC555	4-37
SE556	SE556	TLC556	4-203
SE556C	SE556C	TLC556	4-49
uA733	uA733	4-203	

SPRAGUE		SUGGESTED TI REPLACEMENT	PAGE NO.
UGN3019		TL3019C	4-167
UGS3019		TL3019I	4-167
UGN3020		TL3020C	4-169
UGS3020		TL3020I	4-169

D2997, MARCH 1987

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Total Harmonic Distortion**
- **Low Supply Current . . . Typically 8 mA**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**
- **Pin Compatible with the LM348**

D, J, OR N PACKAGE
(TOP VIEW)



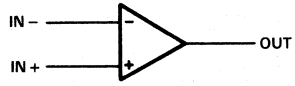
description

These devices are low-cost, high-speed, JFET-input operational amplifiers. They require low supply current yet maintain a large gain-bandwidth product and a fast slew rate. In addition, their matched high-voltage JFET inputs provide very low input bias and offset current.

The LF347 and LF347B can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF347 and LF347B are characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	LF347D	LF347J	LF347N
	5 mV	LF347BD	LF347BJ	LF347BN

D packages are available taped and reeled. Add "R" suffix to the device type. (e.g. LF347DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package . . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	680 mW	7.6 mW/°C	61°C	608 mW
J	680 mW	8.2 mW/°C	67°C	656 mW
N	680 mW	N/A	N/A	680 mW

electrical characteristics over operating free-air temperature range, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		LF347 MIN	LF347 TYP	LF347 MAX	LF347B MIN	LF347B TYP	LF347B MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ	$T_A = 25°C$		5	10		3	5	mV
			Full range			13			7	
αV_{IO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0$, $R_S = 10$ kΩ			18			18		μV/°C
I_{IO}	Input offset current†	$V_{IC} = 0$	$T_J = 25°C$		25	100		25	100	pA
			$T_J = 70°C$			4			4	nA
I_{IB}	Input bias current†	$V_{IC} = 0$	$T_J = 25°C$		50	200		50	200	pA
			$T_J = 70°C$			8			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ kΩ		±12	±13.5		±12	±13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10$ V, $R_L = 2$ kΩ	$T_A = 25°C$	25	100		50	100		V/mV
			Full range	15			25			
r_i	Input resistance	$T_J = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \le 10$ kΩ		70	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		80	100		dB
I_{CC}	Supply current				8	11		8	11	mA

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω		18		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz		0.01		$pA/\sqrt{Hz}$

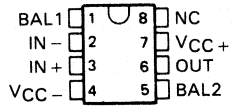
† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

D2997, MARCH 1987

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Voltage**
  Typically 18 nV/$\sqrt{Hz}$
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Supply Current . . . Typically 1.8 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Internally Trimmed Offset Voltage**
  Typically 10 mV
- **High Slew Rate . . . Typically 13 V/μs**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **Pin Compatible with Standard 741**

P, D, OR JG PACKAGE
(TOP VIEW)



NC – No internal connection

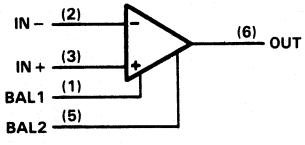
description

This device is a low-cost, high-speed, JFET-input operational amplifier with an internally trimmed input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents. It uses the same offset voltage adjustment circuits as the 741.

The LF351 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF351 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF351	D,JG,P	−0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (ie., LF351DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	T_A = 25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10		μV/°C
I_{IO}	Input offset current†	V_{IC} = 0	T_J = 25°C		25	100	pA
			T_J = 70°C			4	nA
I_{IB}	Input bias current†	V_{IC} = 0	T_J = 25°C		50	200	pA
			T_J = 70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				1.8	3.4	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz		0.01		$pA/\sqrt{Hz}$

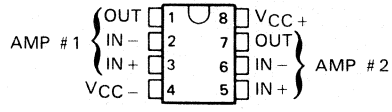
† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2997, MARCH 1987—REVISED MAY 1988

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{\text{Hz}}$
- **Low Input Noise Voltage**
  Typically 18 nV/$\sqrt{\text{Hz}}$
- **Low Supply Current . . . Typically 3.6 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**

D, JG, OR P PACKAGE
(TOP VIEW)



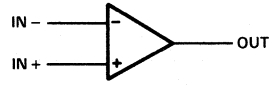
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF353 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF353	D,JG,P	0°C to 70°C	10 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. LP353DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ	T_A = 25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10		μV/°C
I_{IO}	Input offset current†	V_{IC} = 0	T_J = 25°C		25	100	pA
			T_J = 70°C			4	nA
I_{IB}	Input bias current†	V_{IC} = 0	T_J = 25°C		50	200	pA
			T_J = 70°C			8	nA
V_{ICR}	Common-mode input voltage range			±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	100		V/mV
			Full range	15			
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

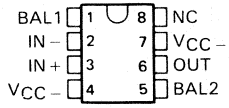
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

D2997, MARCH 1987—REVISED MAY 1988

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Supply Current . . . Typically 2.0 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Low Total Harmonic Distortion**
- **Low 1/f Noise Corner . . . Typically 50 Hz**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

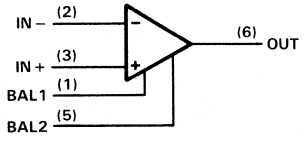
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a maximum input offset voltage drift. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF411C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF411C is characterized for operation from 0°C to 70°C.

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV	LF411CD	LF411CJG	LF411CP

D package is available taped and reeled. Add "R" suffix to device type. (e.g. LF411CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ,	T_A = 25°C		0.8	2	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	V_{IC} = 0	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				2	3.4	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

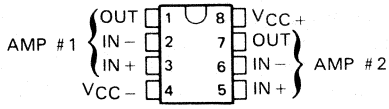
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

D2997, MARCH 1987—REVISED MAY 1988

- **Low Input Bias Current**
  Typically 50 pA
- **Low Input Noise Current**
  Typically 0.01 pA/$\sqrt{Hz}$
- **Low Supply Current . . . Typically 4.5 mA**
- **High Input Impedance**
  Typically 10^{12} Ω
- **Internally Trimmed Offset Voltage**
- **Wide Gain Bandwidth . . . Typically 3 MHz**
- **High Slew Rate . . . Typically 13 V/μs**

D, JG, OR P PACKAGE
(TOP VIEW)



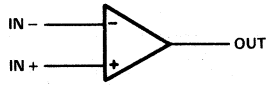
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage and a specified maximum input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF412C can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF412C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LF412C	D,JG,P	0°C to 70°C	3 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. LF412CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} . . . . . 18 V
Supply voltage, V_{CC-} . . . . . −18 V
Differential input voltage, V_{ID} . . . . . ±30 V
Input voltage (see Note 1) . . . . . ±15 V
Duration of output short circuit . . . . . Unlimited
Continuous total power dissipation . . . . . 500 mW
Operating temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

electrical characteristics over operating free-air temperature range, V_{CC+} = 15 V, V_{CC-} = −15 V (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 10 kΩ, T_A = 25°C			1	3	mV
α_{VIO}	Average temperature coefficient of input offset voltage	V_{IC} = 0, R_S = 10 kΩ			10	20†	μV/°C
I_{IO}	Input offset current‡	V_{IC} = 0, See Note 3	T_J = 25°C		25	100	pA
			T_J = 70°C			2	nA
I_{IB}	Input bias current‡	V_{IC} = 0, See Note 3	T_J = 25°C		50	200	pA
			T_J = 70°C			4	nA
V_{ICR}	Common-mode input voltage range			±11	−11.5 to 14.5		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		±12	±13.5		V
A_{VD}	Large-signal differential voltage	V_O = ±10 V, R_L = 2 kΩ	T_A = 25°C	25	200		V/mV
			Full range	15	200		
r_i	Input resistance	T_J = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S ≤ 10 kΩ		70	100		dB
k_{SVR}	Supply voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				4.5	6.8	mA

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	f = 1 kHz		120		dB
SR	Slew rate		8	13		V/μs
B_1	Unity-gain bandwidth		2.7	3		MHz
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		18		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		0.01		pA/√Hz

† At least 90% of the devices meet this limit for α_{VIO}.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.
NOTE 2: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

TEXAS INSTRUMENTS
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D961, OCTOBER 1979–REVISED JUNE 1988

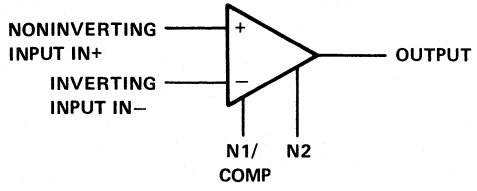
- **Low Input Currents**
- **Low Input Offset Parameters**
- **Frequency and Transient Response Characteristics Adjustable**
- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Same Pin Assignments as uA709**
- **Designed to be Interchangeable with National Semiconductor LM101A and LM301A**

description

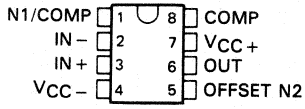
The LM101A, LM201A, and LM301A are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices. The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are protected to withstand short circuits at the output. The external compensation of these amplifiers allows the changing of the frequency response (when the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate. A potentiometer may be connected between the offset-null inputs (N1 and N2), as shown in Figure 7, to null out the offset voltage.

The LM101A is characterized for operation over the full military temperature range of −55°C to 125°C, the LM201A is characterized for operation from −25°C to 85°C, and the LM301A is characterized for operation from 0°C to 70°C.

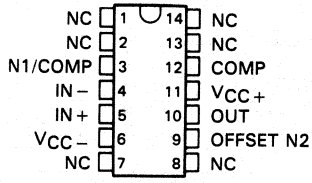
symbol



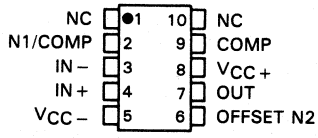
D, JG, OR P PACKAGE
(TOP VIEW)



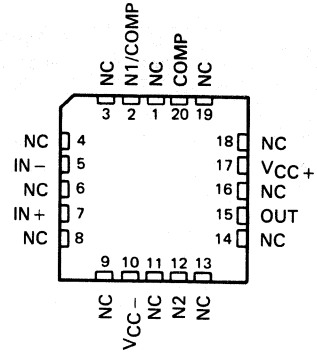
LM101A
W FLAT PACKAGE
(TOP VIEW)



LM101A
U FLAT PACKAGE
(TOP VIEW)



LM101A
FK CHIP-CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM301AD	–	LM301AJG	LM301AP	–	–
−25°C to 85°C	2 mV	LM201AD	–	LM201AJG	LM201AP	–	–
−55°C to 125°C	2 mV	–	LM101AFK	LM101AJG	–	LM101AU	LM101AW

The D package is available taped and reeled. Add the suffix R to the device type. (i.e., LM301ADR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM101A	LM201A	LM301A	UNIT
Supply voltage V_{CC+} (see Note 1)		22	22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−22	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)		±15	±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		−0.5 to 2	−0.5 to 2	−0.5 to 2	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK package		260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM101A only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM201A only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG (LM101A)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (LM201A, LM301A)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, C_C = 30 pF (see Note 5)

PARAMETER		TEST CONDITIONS†		LM101A, LM201A			LM301A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0 V	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage	V_O = 0 V	Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current		25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, V_O = 0, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM101A is −55°C to 125°C, for LM201A is −25°C to 85°C, and for LM301A is 0°C to 70°C.

NOTES: 5. Unless otherwise noted, $V_{CC\pm}$ = ±5 V to ±20 V for LM101A and LM201A, and $V_{CC\pm}$ = ±5 V to ±15 V for LM301A. All typical values are at $V_{CC\pm}$ = ±15 V.

6. For LM101A and LM201A, $V_{CC\pm}$ = ±20 V. For LM301A, $V_{CC\pm}$ = ±15 V.

TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

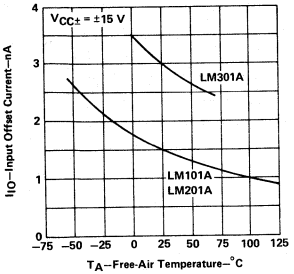


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

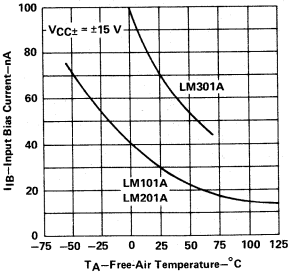


FIGURE 2

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE (WITH
SINGLE-POLE COMPENSATION)
vs FREQUENCY

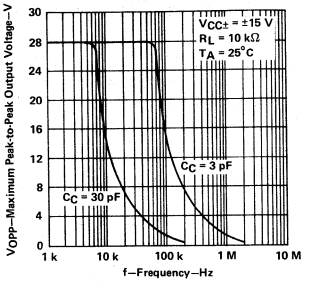


FIGURE 3

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

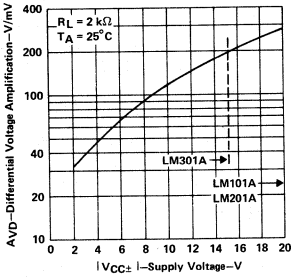


FIGURE 4

OPEN-LOOP LARGE-SIGNAL
DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
FREQUENCY

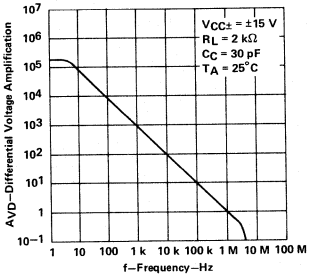


FIGURE 5

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

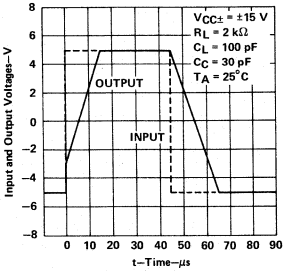
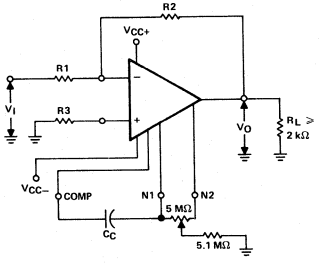


FIGURE 6

TYPICAL APPLICATION DATA



$$\frac{V_O}{V_I} = -\frac{R2}{R1}$$

$$C_C \geq \frac{R1 \cdot 30\ pF}{R1 + R2}$$

$$R3 = \frac{R1 \cdot R2}{R1 + R2}$$

FIGURE 7. INVERTING CIRCUIT WITH ADJUSTABLE GAIN, SINGLE-POLE COMPENSATION, AND OFFSET ADJUSTMENT

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D962, DECEMBER 1970 – REVISED JUNE 1988

- **Low Input Currents**
- **No Frequency Compensation Required**
- **Low Input Offset Parameters**
- **Short-Circuit Protection**
- **No Latch-Up**
- **Wide Common-Mode and Differential Voltage Ranges**

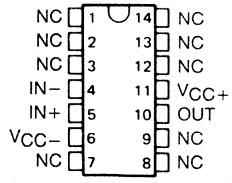
description

The LM107, LM207, and LM307 are high-performance operational amplifiers featuring very low input bias current and input offset voltage and current to improve the accuracy of high-impedance circuits using these devices.

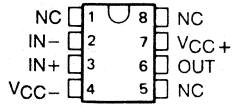
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The LM107 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM207 is characterized for operation from −25°C to 85°C, and the LM307 is characterized for operation from 0°C to 70°C.

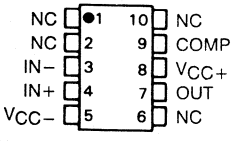
LM107 . . . J OR W PACKAGE
(TOP VIEW)



LM107 . . . JG PACKAGE
LM207, LM307 . . . D, JG, OR P PACKAGE
(TOP VIEW)

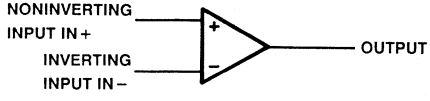


LM107 . . . U FLAT PACKAGE
(TOP VIEW)



NC – No internal connection

symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE					
		SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	LM307D	–	LM307JG	LM307P	–	–
−25°C to 85°C	2 mV	LM207D	–	LM207JG	LM207P	–	–
−55°C to 125°C	2 mV	–	LM107J	LM107JG	–	LM107U	LM107W

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM307DR)

	LM107	LM207	LM307	UNIT
Supply voltage V_{CC+} (see Note 1)	22	22	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−22	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, U, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the LM107 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature. For the LM207 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	–
J (LM107)	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG (LM107)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (LM207, LM307)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	–
P	500 mW	N/A	N/A	500 mW	500 mW	–
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW
W	500 mW	8.0 mW/°C	87°C	500 mW	500 mW	200 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM107, LM207			LM307			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		0.6	2		2	7.5	mV
			Full range			3			10	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_O = 0$	Full range		3	15		6	30	µV/°C
I_{IO}	Input offset current	$V_O = 0$	25°C		1.5	10		3	50	nA
			Full range			20			70	
α_{IIO}	Average temperature coefficient of input offset current	T_A = −55°C to 25°C			0.02	0.2				nA/°C
		T_A = 25°C to MAX			0.01	0.1				
		T_A = 0°C to 25°C						0.02	0.6	
		T_A = 25°C to 70°C						0.01	0.3	
I_{IB}	Input bias current		25°C		30	75		70	250	nA
			Full range			100			300	
V_{ICR}	Common-mode input voltage range	See Note 6	Full range	±15			±12			V
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	25°C	24	28		24	28		V
			Full range	24			24			
		$V_{CC\pm}$ = ±15 V, R_L = 2 kΩ	25°C	20	26		20	26		
			Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50	200		25	200		V/mV
			Full range	25			15			
r_i	Input resistance		25°C	1.5	4		0.5	2		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	80	98		70	90		dB
			Full range	80			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	80	98		70	96		dB
			Full range	80			70			
I_{CC}	Supply current	No load, V_O = 0, See Note 6	25°C		1.8	3		1.8	3	mA
			MAX		1.2	2.5				

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM107 is −55°C to 125°C, for LM207 is −25°C to 85°C, and for LM307 is 0°C to 70°C.

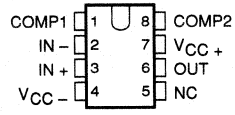
NOTES: 5. Unless otherwise noted $V_{CC\pm}$ = ±5 V to ±20 V for LM107 and LM207, and $V_{CC\pm}$ = ±5 V to ±15 V for LM307. All typical values are at $V_{CC\pm}$ = ±15 V.

6. For LM107 and LM207, $V_{CC\pm}$ = ±20 V. For LM307, $V_{CC\pm}$ = ±15 V.

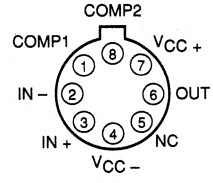
D2808, OCTOBER 1983 – REVISED MARCH 1989

- **Input Offset Current . . . 200 pA Max at 25°C for LM108, LM108A**
- **Input Bias Current . . . 2 nA Max at 25°C for LM108, LM108A**
- **Supply Current . . . 600 μA Max at 25°C for LM108, LM108A**
- **Input Offset Voltage . . . 500 μV Max at 25°C for LM108A, LM308A**
- **Offset Voltage Temperature Coefficient . . . 5 μV/°C Max for LM108A, LM308A**
- **Supply Voltage Range . . . ±2 V to ±18 V**
- **Applications:**
  Integrators
  Transducer Amplifiers
  Analog Memories
  Light Meters
- **Designed To Be Interchangeable with National LM108 Series and Linear Technology LM108 Series**

P PACKAGE
(TOP VIEW)

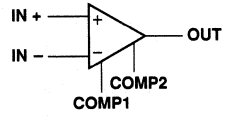


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L package) is in electrical contact with the case.

symbol



description

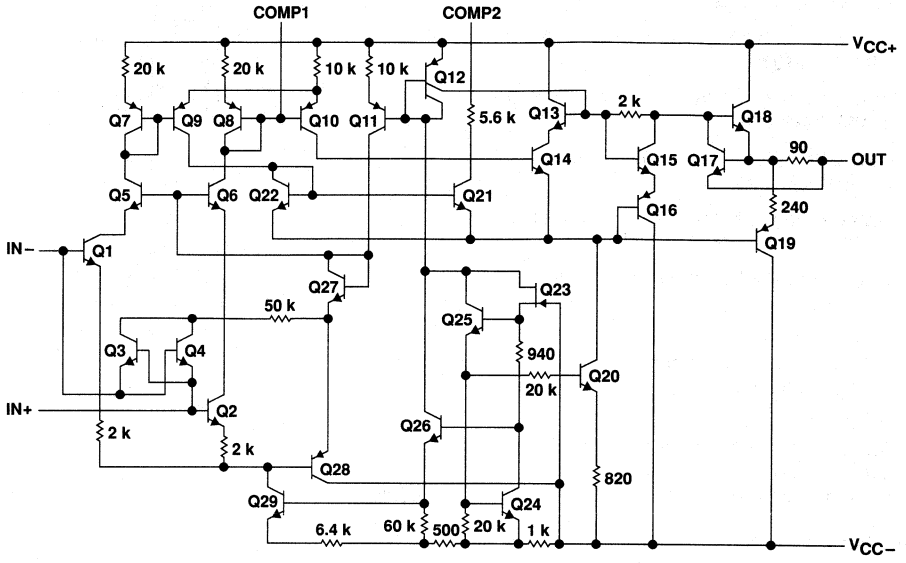
The LM108 series of precision operational amplifiers is particularly well-suited for high-source-impedance applications requiring low input offset and bias currents as well as low power dissipation. Unlike FET input amplifiers, the input offset and bias currents of the LM108 series do not vary significantly with temperature. Advanced design, processing, and testing techniques make this series a superior choice over previous devices. For applications requiring higher performance, see the LT1008 and LT1012.

The LM108 and LM108A are characterized for operation over the full military temperature range of –55°C to 125°C. The LM308 and LM308A are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE	
		METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.5 mV	LM308AL	LM308AP
	7.5 mV	LM308L	LM308P
– 55°C to 125°C	0.5 mV	LM108AL	LM108AP
	2 mV	LM108L	LM108P

schematic



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1): LM108, LM108A . . . . . 20 V
LM308, LM308A . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1): LM108, LM108A . . . . . −20 V
LM308, LM308A . . . . . −18 V
Input voltage range, V_I (see Note 2) . . . . . ±15 V
Differential input current (see Notes 3 and 4) . . . . . ±10 mA
Duration of output short-circuit at (or below) 25°C (see Note 5) . . . . . unlimited
Operating free-air temperature, T_A: LM108, LM108A . . . . . −55°C to 125°C
LM308, LM308A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
5. The output may be shorted to ground or either power supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM108A			LM108			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		0.7	2	mV
			Full range			1			3	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		1	5		3	15	µV/°C
I_{IO}	Input offset current		25°C		0.05	0.2		0.05	0.2	nA
			Full range			0.4			0.4	
α_{IIO}	Temperature coefficient of input offset current		Full range		0.5	2.5		0.5	2.5	pA/°C
I_{IB}	Input bias current		25°C		0.5	2		0.5	2	nA
			Full range			3			3	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±13.5			±13.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		50	300		V/mV
			Full range	40			25			
r_i	Input resistance		25°C	30	70		30	70		MΩ
CMRR	Common-mode rejection ratio		Full range	96			85			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.6		0.3	0.6	mA
			125°C		0.15	0.4		0.15	0.4	

†Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±5 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LM308A			LM308			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω	25°C		0.3	0.5		2	7.5	mV
			Full range			0.73			10	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2	5		6	30	µV/°C
I_{IO}	Input offset current		25°C		0.2	1		0.2	1	nA
			Full range			1.5			1.5	
α_{IIO}	Temperature coefficient of input offset current		Full range		2	10		2	10	pA/°C
I_{IB}	Input bias current		25°C		1.5	7		1.5	7	nA
			Full range			10			10	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V	Full range	±14			±14			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm}$ = ±15 V, R_L = 10 kΩ	Full range	±13			±13			V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V, R_L ≥ 10 kΩ	25°C	80	300		25	300		V/mV
			Full range	60			15			
r_i	Input resistance		25°C	10	40		10	40		MΩ
CMRR	Common-mode rejection ratio		Full range	96			80			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})		Full range	96			80			dB
I_{CC}	Supply current		25°C		0.3	0.8		0.3	0.8	mA

†Full range is 0°C to 70°C.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

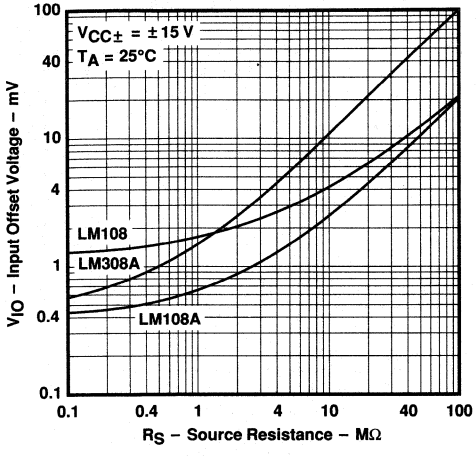


FIGURE 1

TEMPERATURE COEFFICIENT
OF EQUIVALENT INPUT OFFSET VOLTAGE
vs
MATCHED SOURCE RESISTANCE

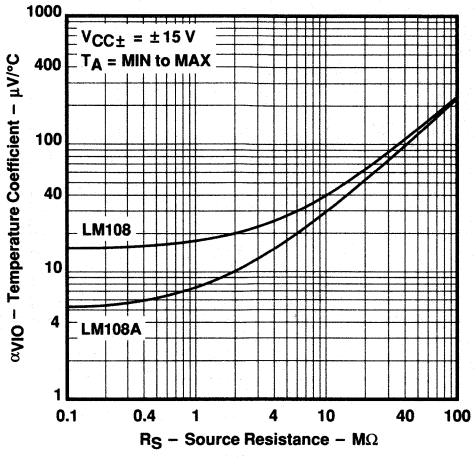


FIGURE 2

LM108, LM108A
INPUT BIAS and OFFSET CURRENTS
vs
FREE-AIR TEMPERATURE

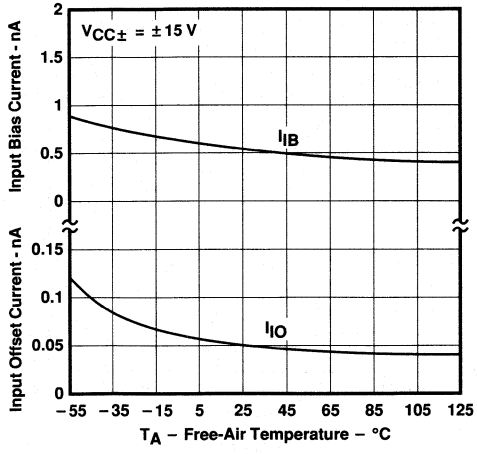


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

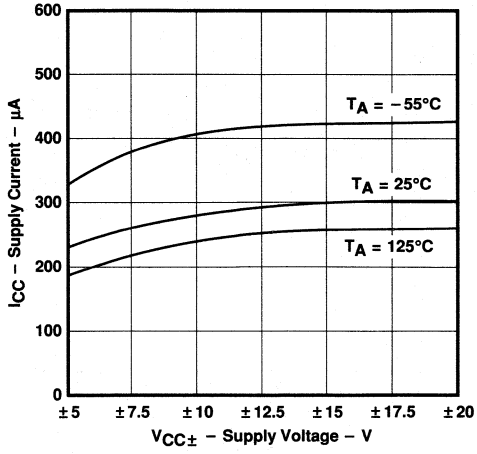


FIGURE 4

†Data above 70°C, below 0°C, or from $V_{CC\pm}$ = ±18 V to ±20 V are applicable to LM108 and LM108A devices only.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

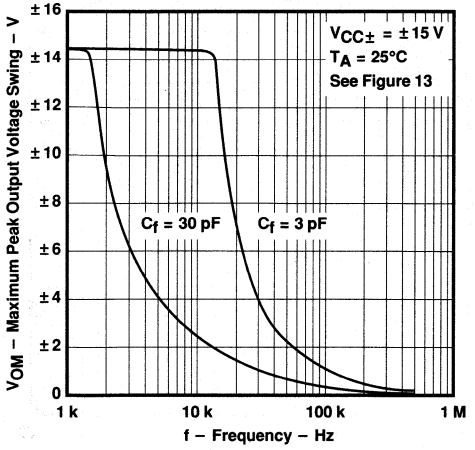


FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE SWING
vs
OUTPUT CURRENT

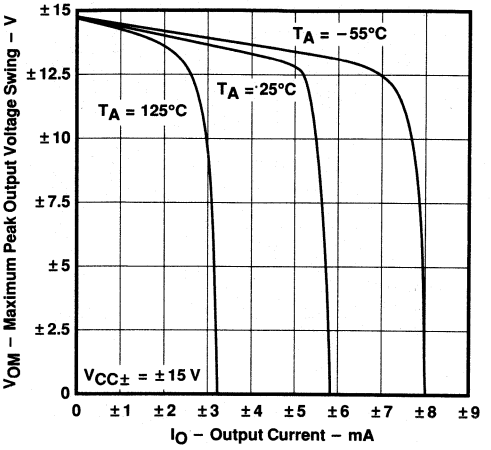


FIGURE 6

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

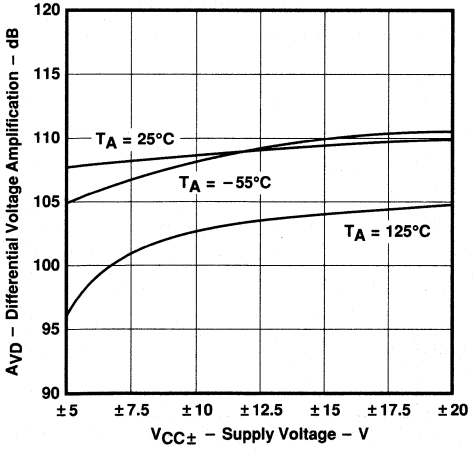


FIGURE 7

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE DELAY
vs
FREQUENCY

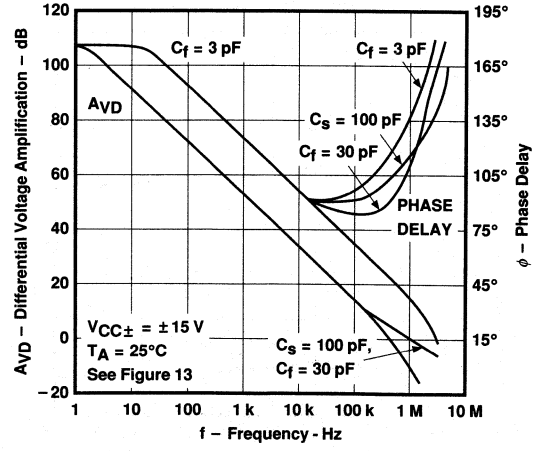


FIGURE 8

†Data above 70°C, below 0°C, or from $V_{CC\pm}$ = ±18 V to ±20 V are applicable to LM108 and LM108A devices only.

TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

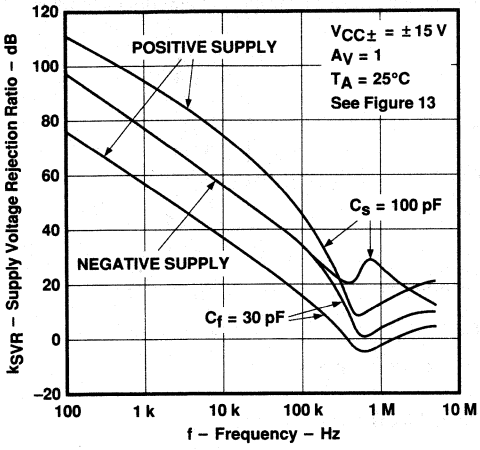


FIGURE 9

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

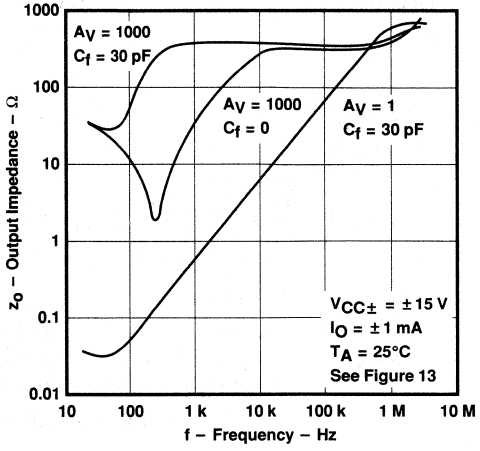


FIGURE 10

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

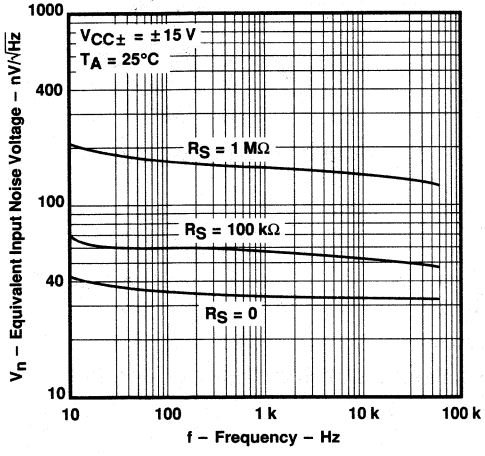


FIGURE 11

VOLTAGE FOLLOWER
PULSE RESPONSE

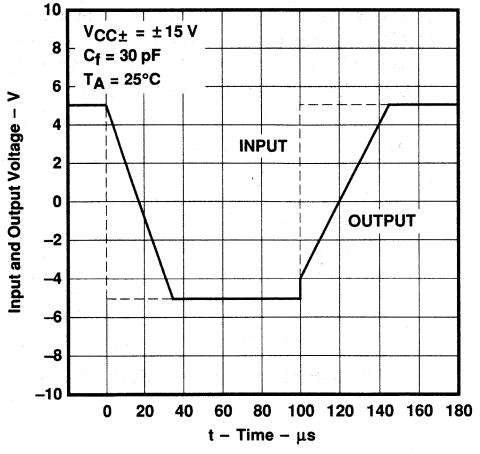
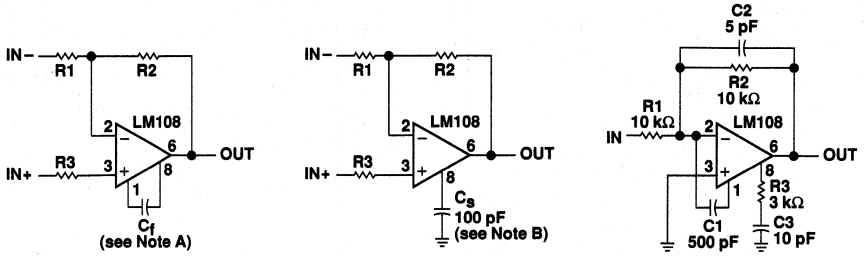


FIGURE 12

TYPICAL APPLICATION DATA

frequency compensation

Figure 13 shows the frequency compensation circuits for standard compensation, alternate compensation, and feed-forward compensation. The alternate compensation circuit improves supply voltage rejection by a factor of ten.



(a) STANDARD (b) ALTERNATE (c) FEED-FORWARD

NOTES: A. $C_f \geq R1C_O/(R1 + R2)$, C_O = 30 pF, bandwidth and slew rate are proportional to $1/C_f$.
B. Bandwidth and slew rate are proportional to $1/C_S$.

FIGURE 13. FREQUENCY COMPENSATION CIRCUITS

input guarding

Input guarding is used to reduce surface leakage (see Figure 14). Both sides of the board must be guarded. Bulk leakage reduction is less than surface leakage reduction and depends on the guard-ring width. The guard ring is connected to a low-impedance point at the same potential as the sensitive input leads. Connections for various op-amp configurations are shown in Figure 15.

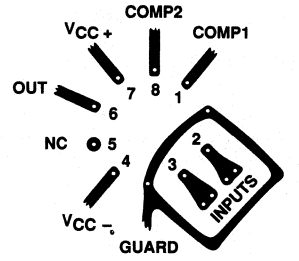
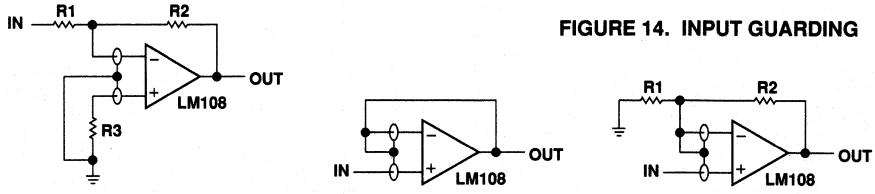


FIGURE 14. INPUT GUARDING



(a) INVERTING (b) FOLLOWER (c) NONINVERTING

FIGURE 15. GUARD RING CONNECTIONS FOR VARIOUS OP AMP CONFIGURATIONS

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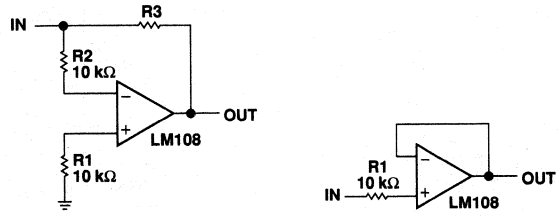
TYPICAL APPLICATION DATA

input protection

Current is limited by R2 even when the input is connected to a voltage source outside the common-mode range [see Figure 16(a)]. If one supply reverses, current is controlled by R1. These resistors do not affect normal operation. The input resistor controls the current when the input exceeds the supply voltages, when the power for the op amp is turned off, or when the output is shorted [see Figure 16(b)].

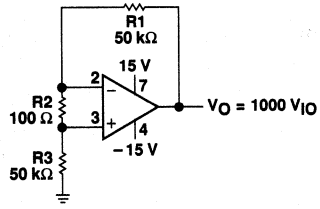


(a) CURRENT LIMITED BY R1 OR R2 (b) CURRENT LIMITED BY R1

FIGURE 16. INPUT PROTECTION

input offset voltage testing

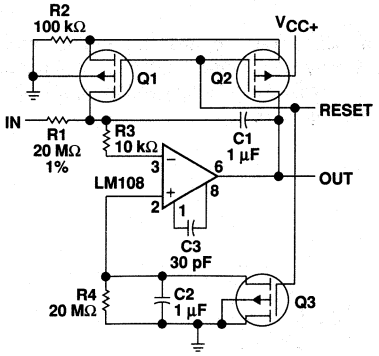
The test circuit for input offset voltage is shown in Figure 17. This circuit is also used as the burn-in configuration with supply voltages equal to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, AV = 100.



NOTE A: Resistors must have low thermoelectric potential.

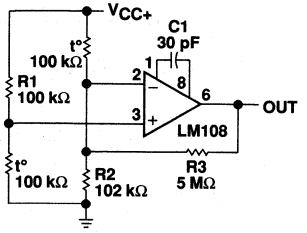
FIGURE 17. TEST CIRCUIT FOR INPUT OFFSET VOLTAGE

TYPICAL APPLICATION DATA



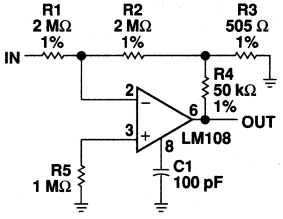
NOTE A: Q1 and Q3 should not have internal gate-protection diodes.

FIGURE 18. LOW-DRIFT INTEGRATOR WITH RESET



NOTE A: R1 = R2R3/(R2 + R3).

FIGURE 19. AMPLIFIER FOR BRIDGE TRANSDUCERS



NOTE A: R2 > R1, R2 >> R3,
A_V = R2(R3 + R4)/R1R3.

FIGURE 20. INVERTING AMPLIFIER WITH HIGH INPUT RESISTANCE

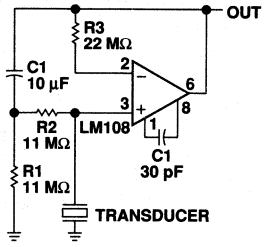
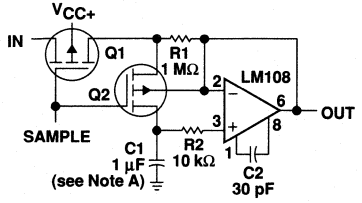
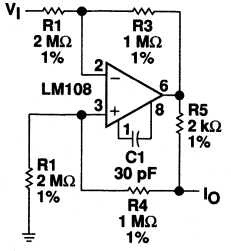


FIGURE 21. AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



NOTES: A. Teflon, polyethylene, or polycarbonate dielectric capacitor.
B. Worst case drift is less than 2.5 mV/s.

FIGURE 22. SAMPLE-AND-HOLD AMPLIFIER



NOTE A: I_O = (R3)V_I/R1R5
R3 = R4 + R5
R1 = R2

FIGURE 23. BILATERAL CURRENT SOURCE

TYPICAL APPLICATION DATA

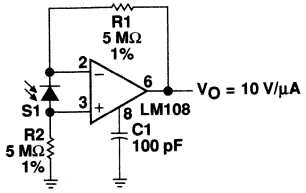
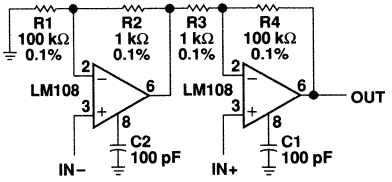
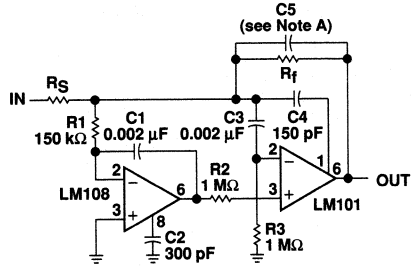


FIGURE 24. AMPLIFIER FOR PHOTODIODE SENSOR



NOTE A: R1 = R4, R2 = R3, A_V = 1 + R1/R2

FIGURE 25. DIFFERENTIAL-INPUT INSTRUMENTATION AMPLIFIER

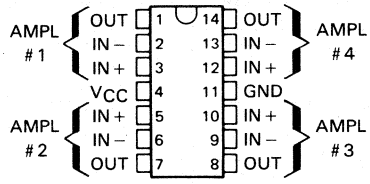


NOTES: A. C5 = $6 \times 10^{-8}/R_f$
B. Power bandwidth = 250 kHz
C. Small-signal bandwidth = 3.5 MHz
D. Slew Rate = 10 V/μs
E. The LM101 increases speed, raises high- and low-frequency gain, increases output drive capability, and eliminates thermal feedback.

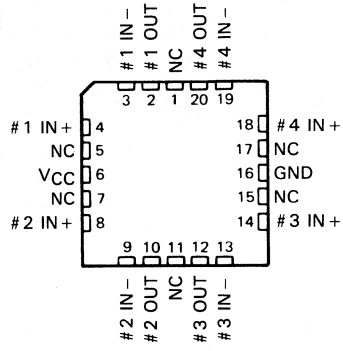
FIGURE 26. FAST SUMMING AMPLIFIER

- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2902 . . . 3 V to 26 V),
  or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . 32 V (26 V for LM2902)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

LM124 . . . J OR W PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGES
(TOP VIEW)

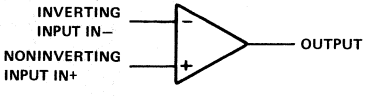


LM124
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each amplifier)



description

These devices consist of four independent, high-gain frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (for the LM2902, 3 V to 26 V), and Pin 4 is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

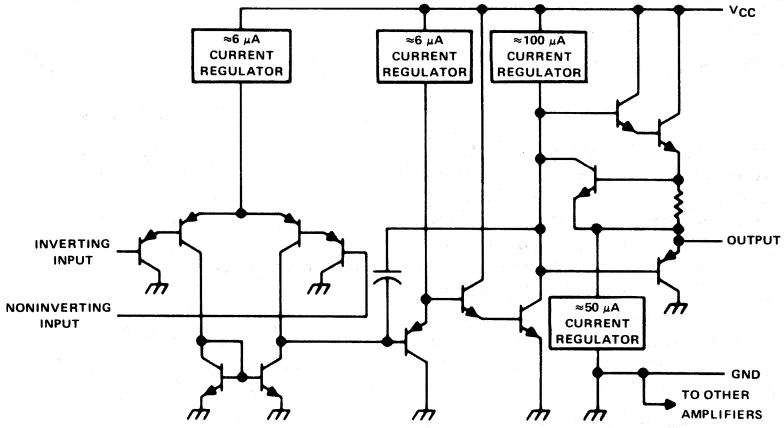
The LM124 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM2902 is characterized for operation from −40°C to 105°C, the LM224 and LM224A from −25°C to 85°C, and the LM324 and LM324A from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)
0°C to 70°C	7 mV	LM324D	—	LM324J	LM324N	—
	3 mV	LM324AD		LM324AJ	LM324AN	
−25°C to 85°C	5 mV	LM224D	—	LM224J	LM224N	—
	3 mV	LM224AD		LM224AJ	LM224AN	
−40°C to 105°C	7 mV	LM2902D	—	LM2902J	LM2902N	—
−55°C to 125°C	5 mV	—	LM124FK	LM124J	—	LM124W

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM324DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			LM124, LM224, LM224A, LM324, LM324A	LM2902	UNIT
Supply voltage, V_{CC} (see Note 1)			32	26	V
Differential voltage (see Note 2)			±32	±26	V
Input voltage range (either input)			−0.3 to 32	−0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)			unlimited	unlimited	
Continuous total dissipation			See Dissipation Rating Table		
Operating free-air temperature range	LM124		−55 to 125		°C
	LM224, LM224A		−25 to 85		
	LM324, LM324A		0 to 70		
	LM2902			−40 to 105	
Storage temperature range			−65 to 150	−65 to 150	°C
Case temperature for 60 seconds		FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		D or N package	260	260	°C

NOTES: 1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	32°C	608 mW	494 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM124)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (all others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	N/A
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A
W	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	200 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM124, LM224			LM324			LM2902			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1.5$			$V_{CC}-1.5$						V
		R_L = 10 kΩ	25°C							$V_{CC}-1.5$			
		V_{CC} = MAX, R_L = 2 kΩ	Full range	26			26			22			
		V_{CC} = MAX, R_L = 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	$R_l \le$ 10 kΩ	Full range		5	20		5	20		5	100	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, $R_L \ge$ 2 kΩ	25°C	50	100		25	100			100		V/mV
			Full range	25			15			15			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	25°C	70	80		65	80		50	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		50	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		10	20		
			Full range	5			5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1.1	3		1.1	3		1.1	3	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2902, 30 V for the others. Full range is −55°C to 125°C for LM124, −25°C to 85°C for LM224, 0°C to 70°C for LM324, and −40°C to 105°C for LM2902.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

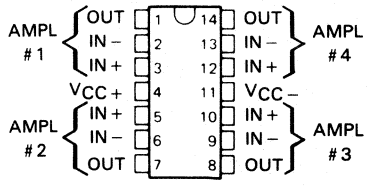
PARAMETER		TEST CONDITIONS†		LM224A			LM324A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
I_O	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−80		−15	−100	nA
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} = 30 V	25°C	0 to $V_{CC}-1.5$			to $V_{CC}-1.5$			V
			Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			
V_{OH}	High-level output voltage	R_L = 2 kΩ	25°C	$V_{CC}-1$			$V_{CC}-1$			V
		V_{CC} 30 V, R_L = 2 kΩ	Full range	26			26			
		V_{CC} = 30 V, R_L = 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	R_l ≤ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30	−60	−20	−30	−60	mA
			Full range	−10			−10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5			5			
		V_{ID} = −1 V, V_O = 200 mV	Full range	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60	mA
I_{CC}	Supply current (four amplifiers)	V_O = 2.5 V, No load	Full range		1.5	2.4		1.5	2.4	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1.1	3		1.1	3	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25°C to 85°C for LM224A and 0°C to 70°C for LM324A.

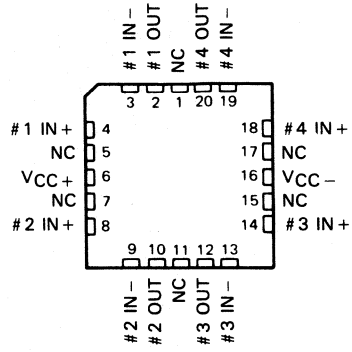
D2551, OCTOBER 1979—REVISED MAY 1988

- **uA741 Operating Characteristics**
- **Low Supply Current Drain . . . 0.6 mA Typ (per amplifier)**
- **Low Input Offset Voltage**
- **Low Input Offset Current**
- **Class AB Output Stage**
- **Input/Output Overload Protection**
- **Designed to be Interchangeable with National LM148, LM248, and LM348.**

LM148 . . . J PACKAGE
LM248, LM348 . . . D, J, OR N PACKAGE
(TOP VIEW)



LM148. . . FK PACKAGE
(TOP VIEW)



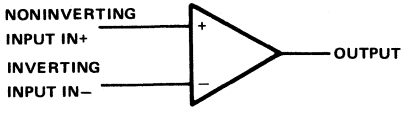
NC—No internal connection

description

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the uA741. These amplifiers exhibit low supply current drain, and input bias and offset currents that are much less than those of the uA741.

The LM148 is characterized for operation over the full military temperature range of −55°C to 125°C, the LM248 is characterized for operation from −25°C to 85°C, and the LM348 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	6 mV	LM348D	—	LM348J	LM348N
−25°C to 85°C	6 mV	LM248D	—	LM248J	LM248N
−55°C to 125°C	5 mV	—	LM148FK	LM148J	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM348DR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM148	LM248	LM348	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		44	36	36	V
Input voltage (either input, see Notes 1 and 3)		±22	±18	±18	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	32°C	608 mW	494 mW	N/A
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM148)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM248, LM348)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	N/A
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	N/A

electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†			LM148			LM248			LM348			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0		25°C		1	5		1	6		1	6	mV
				Full range			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0		25°C		4	25		4	50		4	50	nA
				Full range			75			125			100	
I_{IB}	Input bias current	V_O = 0		25°C		30	100		30	200		30	200	nA
				Full range			325			500			400	
V_{ICR}	Common-mode input voltage range			Full range	±12			±12			±12			V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ		25°C	±12	±13		±12	±13		±12	±13		V
		R_L ≥ 10 kΩ		Full range	±12			±12			±12			
		R_L = 2 kΩ		25°C	±10	±12		±10	±12		±10	±12		
		R_L ≥ 2 kΩ		Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ		25°C	50	160		25	160		25	160		V/mV
				Full range	25			15			15			
r_i	Input resistance			25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
B_1	Unity-gain bandwidth	A_{VD} = 1		25°C		1			1			1		MHz
ϕ_M	Phase margin	A_{VD} = 1		25°C		60°			60°			60°		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0		25°C	70	90		70	90		70	90		dB
				Full range	70			70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C	77	96		77	96		77	96		dB
				Full range	77			77			77			
I_{OS}	Short-circuit output current			25°C		±25			±25			±25		mA
I_{CC}	Supply current (four amplifiers)	No load	V_O = 0	25°C					2.4	4.5		2.4	4.5	mA
			V_O = V_{OM}†			2.4	3.6							
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 Hz to 20 kHz,		25°C		120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for LM148, −25°C to 85°C for LM248, and 0°C to 70°C for LM348.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

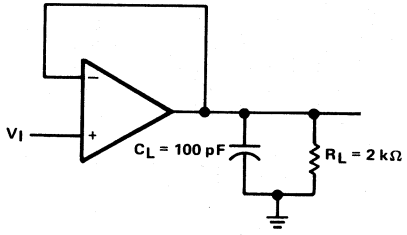
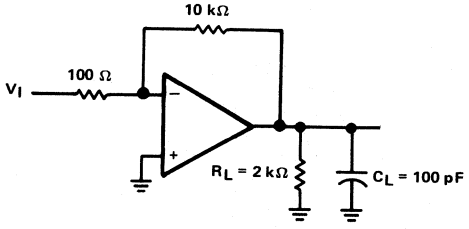


FIGURE 1. UNITY-GAIN AMPLIFIER



A_{VD} = −100

FIGURE 2. INVERTING AMPLIFIER

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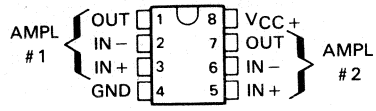
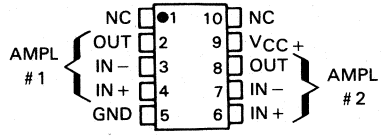
- **Wide Range of Supply Voltages:**
  Single Supply . . . 3 V to 30 V
  (LM2904 . . . 3 V to 26 V),
  or Dual Supplies
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.7 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters:**
  Input Offset Voltage . . . 3 mV Typ
  A Versions . . . 2 mV Typ
  Input Offset Current . . . 2 nA Typ
  Input Bias Current . . . 20 nA Typ
  A Versions . . . 15 nA Typ
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V (±26 V for LM2904)**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

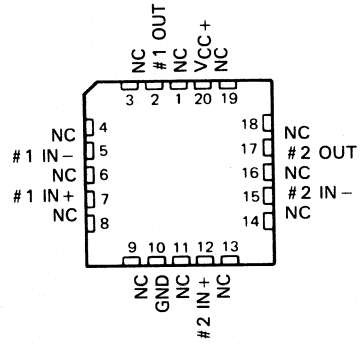
D, JG, OR P PACKAGE
(TOP VIEW)



U FLAT PACKAGE
(TOP VIEW)



LM 158
FK CHIP CARRIER PACKAGE
(TOP VIEW)



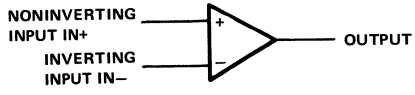
NC–No internal connection

description

These devices consist of two independent, high-gain, frequency-compensated operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible so long as the difference between the two supplies is 3 V to 30 V (3 V to 26 V for the LM2904), and the V_{CC} pin is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, these devices can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

schematic (each amplifier)



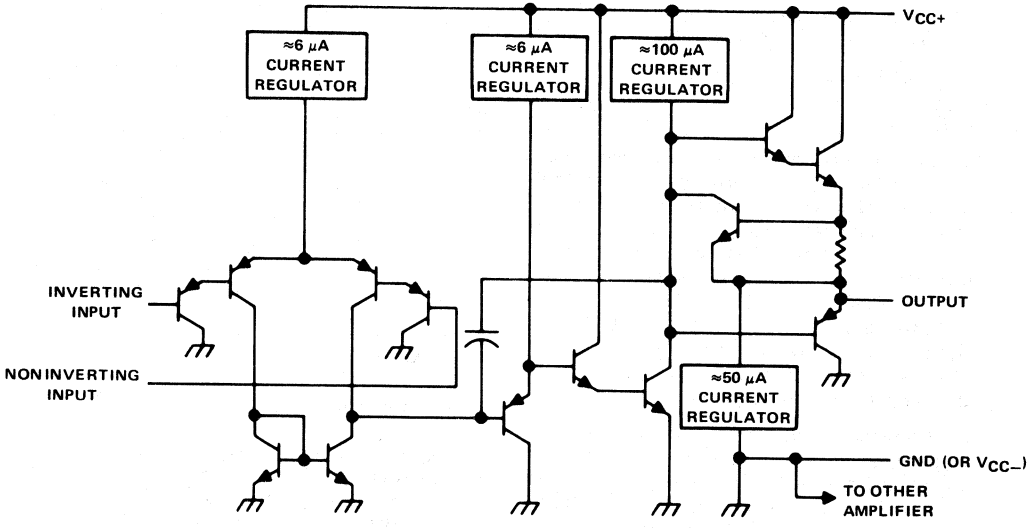
The LM158 is characterized for operation over the full military temperature range of −55°C to 125°C. The LM258 and LM258A are characterized for operation from −25°C to 85°C, the LM358 and LM358A from 0°C to 70°C, and the LM2904 from −40°C to 105°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE				
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)
0°C to 70°C	7 mV	LM358D	—	LM358JG	LM358P	—
	3 mV	LM358AD		LM358AJG	LM358AP	
−25°C to 85°C	5 mV	LM258D	—	LM258JG	LM258P	—
	3 mV	LM258AD		LM258AJG	LM258AP	
−40°C to 105°C	7 mV	LM2904D	—	LM2904JG	LM2904P	—
−55°C to 125°C	5 mV	—	LM158FK	LM158JG	—	LM158U

The D package is available taped and reeled. Add the suffix R to the device type. (e.g., LM358DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

			LM158, LM258, LM258A LM358, LM358A	LM2904	UNIT
Supply voltage, V_{CC} (see Note 1)			32	26	V
Differential voltage (see Note 2)			±32	±26	V
Input voltage range (either input)			0.3 to 32	0.3 to 26	V
Duration of output short-circuit (one amplifier) to ground at (or below) 25°C free-air temperature (V_{CC} ≤ 15 V) (see Note 3)			unlimited	unlimited	
Continuous total dissipation			See Dissipation Rating Table		
Operating free-air temperature range	LM158		−55 to 125		°C
	LM258, LM258A		−25 to 85		
	LM358, LM358A		0 to 70		
	LM2904			−40 to 105	
Storage temperature range			−65 to 150	−65 to 150	°C
Case temperature for 60 seconds		FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds		JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		D or P package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, and V_{CC} specified for measurement of I_{OS}, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (LM158)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (all others)	825 mW	6.6 mW/°C	528 mW	429 mW	—
P	1000 mW	8.0 mW/°C	640 mW	520 mW	—
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM158, LM258			LM358			LM2904			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		3	5		3	7		3	7	mV
			Full range			7			9			10	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7			7			7		μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	30		2	50		2	50	nA
			Full range			100			150			200	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10			10			10		pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−20	−150		−20	−250		−20	−250	nA
			Full range			−300			−500			−500	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to MAX	25°C	0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			V
			Full range	0 to V_{CC} − 2			0 to V_{CC} − 2			0 to V_{CC} − 2			
V_{OH}	High-level output voltage	R_L ≥ 2 kΩ	25°C	V_{CC} − 1.5			V_{CC} − 1.5						V
		R_L ≥ 10 kΩ	25°C							V_{CC} − 1.5			
		V_{CC} = MAX, R_L = 2 kΩ,	Full range	26			26			22			
		V_{CC} = MAX, R_L ≥ 10 kΩ	Full range	27	28		27	28		23	24		
V_{OL}	Low-level output voltage	R_L ≤ 10 kΩ	Full range		5	20		5	20		5	100	mV

A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100		100		V/mV
			Full range	25			15			15		
CMRR	Common-mode rejection ratio	V_{CC} = 5 V to MAX, V_{IC} = V_{ICR} min	25°C	70	80		65	80		50	80	dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	V_{CC} = 5 V to MAX	25°C	65	100		65	100		50	100	dB
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120			120	dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−20	−30		−20	−30		−20	−30	mA
			Full range	−10			−10			−10		
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 5 V	25°C	10	20		10	20		10	20	
			Full range	5			5			5		
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30			30	μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
		V_{CC} = MAX, V_O = 0.5 V_{CC}, No load	Full range		1	2		1	2		1	2	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. "MAX" V_{CC} for testing purposes is 26 V for LM2904, 30 V for the others. Full range is −55°C to 125°C for LM158, −25°C to 85°C for LM258, 0°C to 70°C for LM358, and −40°C to 105°C for LM2904.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM258A			LM358A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 v to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V	25°C		2	3		2	3	mV
			Full range			4			5	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		7	15		7	20	μV/°C
I_{IO}	Input offset current	V_O = 1.4 V	25°C		2	15		2	30	nA
			Full range			30			75	
α_{IIO}	Average temperature coefficient of input offset current		Full range		10	200		10	300	pA/°C
I_{IB}	Input bias current	V_O = 1.4 V	25°C		−15	−80		−15	−100	nA
			Full range			−100			−200	
V_{ICR}	Common-mode input voltage range	V_{CC} 30 V	25°C	0 to V_{CC} − 1.5			0 to V_{CC} − 1.5			V
			Full range	0 to V_{CC} − 2			0 to V_{CC} − 2			
V_{OH}	High-level output voltage	$R_L \geq 2$ kΩ	25°C	V_{CC} − 1.5			V_{CC} − 1.5			V
		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			
		V_{CC} = 30 V, $R_L \geq$ 10 kΩ	Full range	27	28		27	28		
V_{OL}	Low-level output voltage	$R_L \leq$ 10 kΩ	Full range		5	20		5	20	mV

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

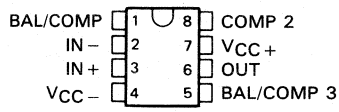
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1 V to 11 V, R_L = ≥ 2 kΩ	25°C	50	100		25	100		V/mV
			Full range	25			15			
CMRR	Common-mode rejection ratio		25°C	70	80		65	80		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		25°C	65	100		65	100		dB
V_{o1}/V_{02}	Crosstalk attenuation	f = 1 kHz to 20 kHz	25°C		120			120		dB
I_O	Output current	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	20	30	60	20	30	60	mA
			Full range	10			10			
		V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
			Full range	5			5			
		V_{ID} = −1 V, V_O = 200 mV	25°C	12	30		12	30		μA
I_{OS}	Short-circuit output current	V_{CC} at 5 V, GND at −5 V, V_O = 0	25°C		±40	±60		±40	±60	mA
I_{CC}	Supply current (two amplifiers)	V_O = 2.5 V, No load	Full range		0.7	1.2		0.7	1.2	mA
		V_{CC} = 30 V, V_O = 15 V, No load	Full range		1	2			2	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −25°C to 85°C for LM258A and 0°C to 70°C to LM358A.

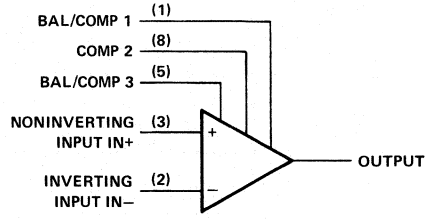
D2219, JUNE 1976 – REVISED OCTOBER 1988

- **Small-Signal Bandwidth . . . 15 MHz Typ**
- **Slew Rate . . . 50 V/ μs Min**
- **Bias Current . . . 250 nA Max (LM218)**
- **Supply Voltage Range . . . ±5 V to ±20 V**
- **Internal Frequency Compensation**
- **Input and Output Overload Protection**
- **Same Pin Assignments as General-Purpose Operational Amplifiers**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



description

The LM218 and LM318 are precision, high-speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor-of-ten increase in speed over general purpose devices without sacrificing dc performance.

These operational amplifiers have internal unity-gain frequency compensation. This considerably simplifies their application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feed-forward compensation will boost the slew rate to over 150 V/μs and almost double the bandwidth. Over compensation may be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor may be added to reduce the settling time for 0.1% error band to under 1 μs.

The high speed and fast settling time of these operational amplifiers make them useful in A/D converters, oscillators, active filters, sample and hold circuits, and general purpose amplifiers.

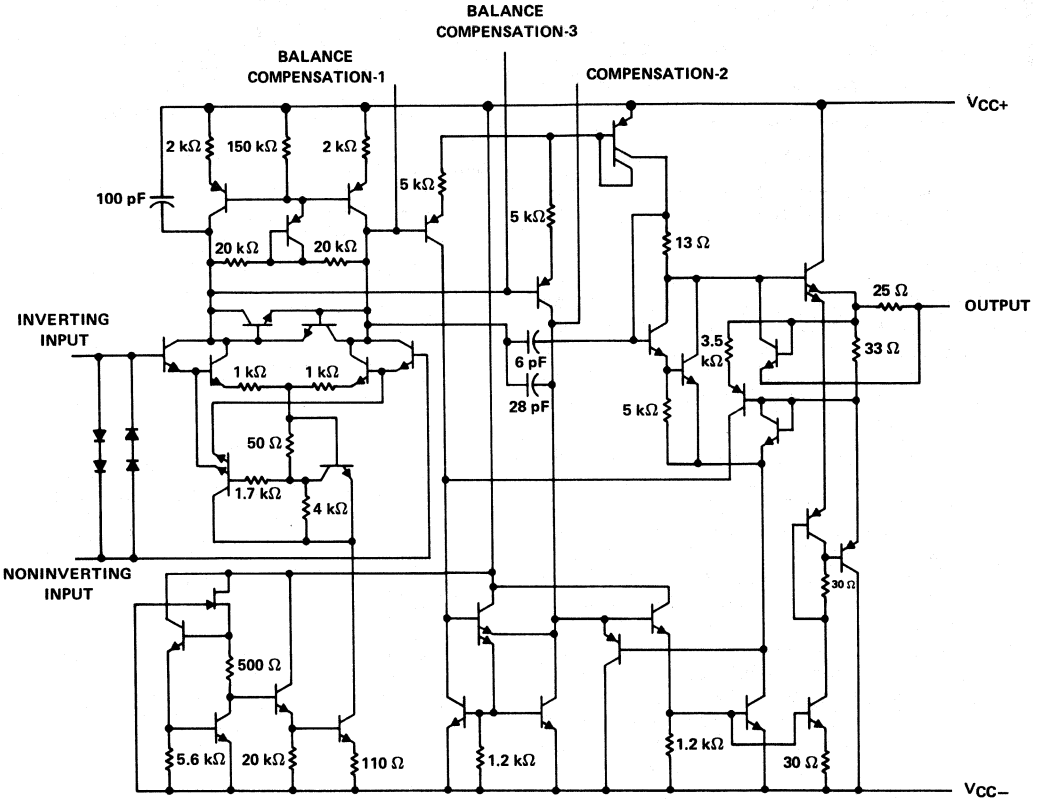
The LM218 is characterized for operation from −25°C to 85°C, and the LM318 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LM318D	LM318JG	LM318P
−25°C to 85°C	4 mV	LM218D	LM218JG	LM218P

The D packages are available taped and reeled. Add the suffix R to the device type (e.g., LM318DR).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM218	LM318	UNIT
Supply voltage, V_{CC+} (see Note 1)		20	20	V
Supply voltage, V_{CC-} (see Note 1)		−20	−20	V
Input voltage (either input, see Notes 1 and 2)		±15	±15	V
Differential input current (see Note 3)		±10	±10	mA
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
3. The inputs are shunted with two opposite-facing base-emitter diodes for over voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of approximately 1 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. For the LM218 only, the unlimited duration of the short-circuit applies at (or below) 85°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW
JG	500 mW	6.6 mW/°C	74°C	500 mW	429 mW
P	500 mW	N/A	N/A	500 mW	500 mW

electrical characteristics at specified free-air temperature (see Note 5)

PARAMETER		TEST CONDITIONS†		LM218			LM318			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		2	4		4	10	mV
			Full range			6			15	
I_{IO}	Input offset current	$V_O = 0$	25°C		6	50		30	200	nA
			Full range			100			300	
I_{IB}	Input bias current	$V_O = 0$	25°C		120	250		150	500	nA
			Full range			500			750	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm} = \pm15$ V	Full range	±11.5			±11.5			V
V_{OM}	Maximum peak output voltage swing	$V_{CC\pm} = \pm15$ V, $R_L = 2$ kΩ	Full range	±12	±13		±12	±13		V
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm15$ V, $V_O = \pm10$ V, $R_L \geq 2$ kΩ	25°C	50	200		25	200		V/mV
			Full range	25			20			
B_1	Unity-gain bandwidth	$V_{CC\pm} = \pm15$ V	25°C		15			15		MHz
r_i	Input resistance		25°C	1	3		0.5	3		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min	Full range	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		Full range	70	80		65	80		dB
I_{CC}	Supply current	No load, $V_O = 0$	25°C		5	8		5	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for LM218 is −25°C to 85°C and for LM318 is 0°C to 70°C.

Note 5: Unless otherwise noted, V_{CC} = ±5 V to ±20 V. All typical values are at $V_{CC\pm} = \pm15$ V, T_A = 25°C.

operating characteristics, $V_{CC+} = 15$ V, $V_{CC-} = 15$ V, $T_A = 25$°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$\Delta V_I = 10$ V,	$C_L = 10$ pF,	See Figure 1	50	70		V/μs

PARAMETER MEASUREMENT INFORMATION

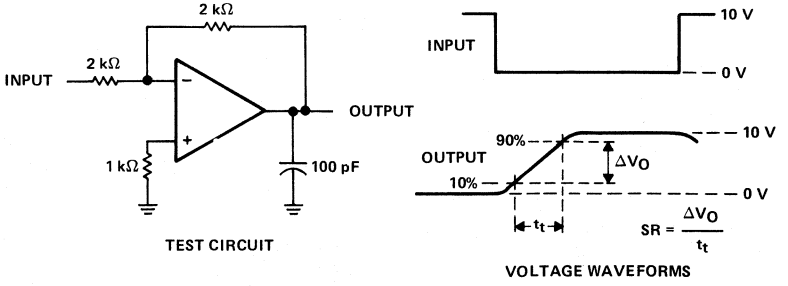
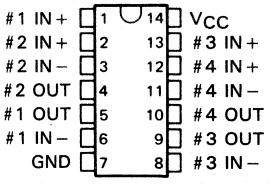


FIGURE 1. SLEW RATE

D2531, JULY 1979 – REVISED AUGUST 1988

- **Wide Range of Supply Voltages, Single or Dual Supplies**
- **Wide Bandwidth**
- **Large Output Voltage Swing**
- **Output Short-Circuit Protection**
- **Internal Frequency Compensation**
- **Low Input Bias Current**
- **Designed to be Interchangeable with National Semiconductor LM2900 and LM3900, Respectively**

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

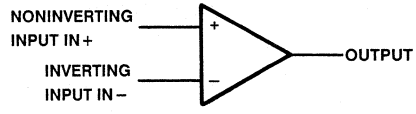
T_A	PACKAGE	
	PLASTIC DIP (N)	CERAMIC DIP (J)
0°C to 70°C	LM3900N	LM3900J
−40°C to 85°C	LM2900N	LM2900J

description

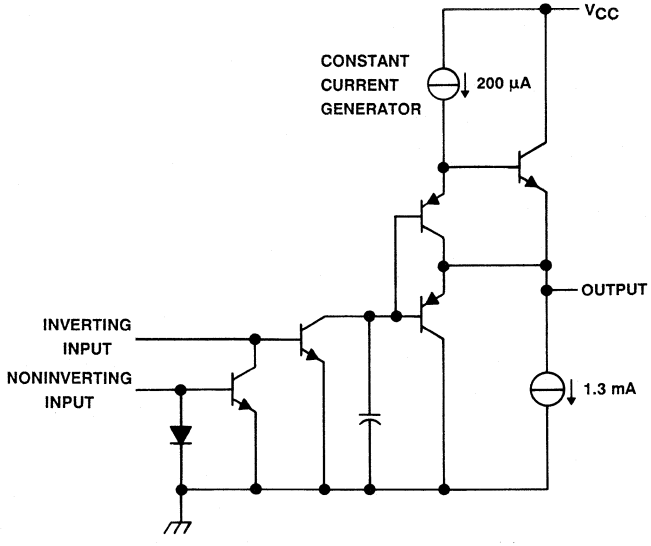
These devices consist of four independent, high-gain frequency-compensated Norton operational amplifiers that were designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible. The low supply current drain is essentially independent of the magnitude of the supply voltage. These devices provide wide bandwidth and large output voltage swing.

The LM2900 is characterized for operation from −40°C to 85°C, and the LM3900 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		LM2900	LM3900	UNIT
Supply voltage, V_{CC} (see Note 1)		36	36	V
Input current		20	20	mA
Duration of output short circuit (one amplifier) to ground at (or below) 25°C free-air temperature (see Note 2)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J Package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N Package	260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	LM2900		LM3900		UNIT
	MIN	MAX	MIN	MAX	
Input current (see Note 3)		−1		−1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

NOTE 3: Clamp transistors are included that prevent the input voltages from swinging below ground more than approximately −0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately −1 mA. Negative input currents in excess of −4 mA will cause the output voltage to drop to a low voltage. These values apply for any one of the input terminals. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common-mode current biasing can be used to prevent negative input voltages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics, V_{CC} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM2900			LM3900			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{IB}	Input bias current (inverting input)	I_{I+} = 0	T_A = 25°C		30	200		30	200	nA
			T_A = Full range		300			300		
$\frac{I_{I-}}{I_{I+}}$	Mirror gain	I_{I+} = 20 µA to 200 µA, T_A = Full range, See Note 4		0.9		1.1	0.9		1.1	µA/µA
	Change in mirror gain				2	5		2	15	%
	Mirror current	$V_{I+} = V_{I-}$, See Note 4	T_A = Full range,		10	500		10	500	µA
A_{VD}	Large-signal differential voltage amplification	V_O = 10 V, f = 100 Hz	R_L = 10 kΩ,	1.2	2.8		1.2	2.8		V/mV
r_i	Input resistance (inverting input)				1			1		MΩ
r_o	Output resistance				8			8		kΩ
B_1	Unity-gain bandwidth (inverting input)				2.5			2.5		MHz
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)				70			70		dB
V_{OH}	High-level output voltage	I_{I+} = 0, I_{I-} = 0	R_L = 2 kΩ	13.5			13.5			V
			V_{CC} = 30 V, No load		29.5			29.5		
V_{OL}	Low-level output voltage	I_{I+} = 0, R_L = 2 kΩ	I_{I-} = 10 µA,		0.09	0.2		0.09	0.2	V
I_{OHS}	Short-circuit output current (output internally high)	I_{I+} = 0, V_O = 0	I_{I-} = 0,	−6	−18		−6	−10		mA
	Pull-down current			0.5	1.3		0.5	1.3		mA
I_{OL}	Low-level output current‡	I_{I-} = 5 µA, V_{OL} = 1 V			5			5		mA
I_{CC}	Supply current (four amplifiers)	No load			6.2	10		6.2	10	mA

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for LM2900, and 0°C to 70°C for LM3900.

‡ The output current-sink capability can be increased for large-signal conditions by overdriving the inverting input.

NOTE 4: These parameters are measured with the output balanced midway between V_{CC} and ground.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	Low-to-high output	V_O = 10 V,	C_L = 100 pF,		0.5		V/µs
		High-to-low output	R_L = 2 kΩ			20		

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT (INVERTING INPUT)
vs
FREE-AIR TEMPERATURE

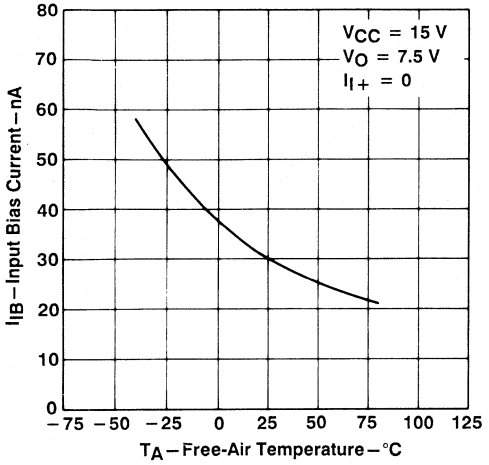


FIGURE 1

MIRROR GAIN
vs
FREE-AIR TEMPERATURE

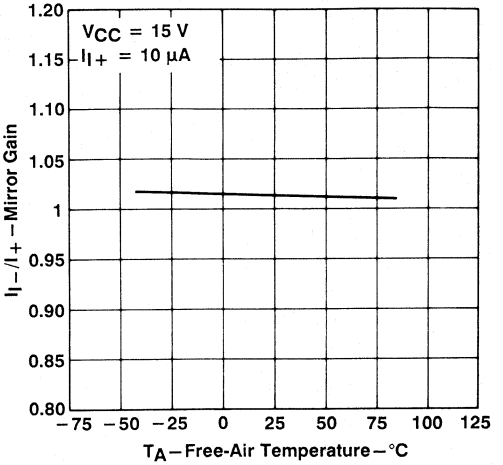


FIGURE 2

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

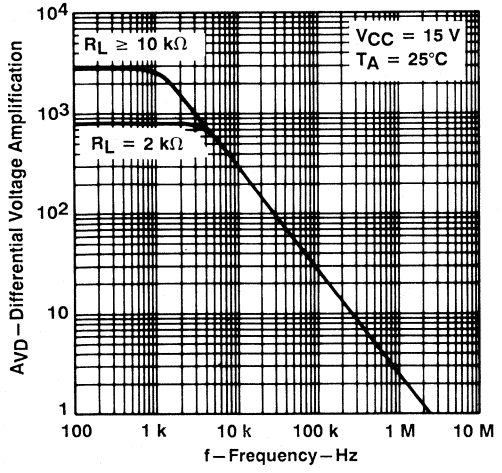


FIGURE 3

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

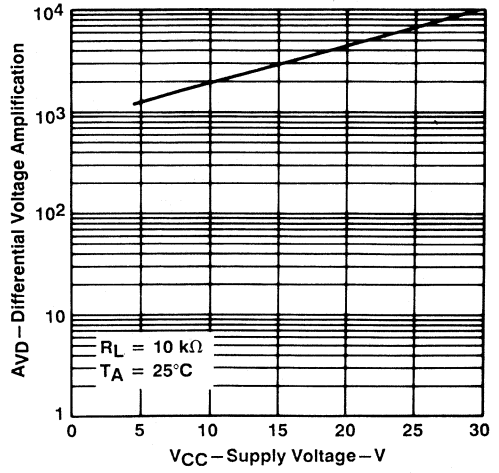


FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

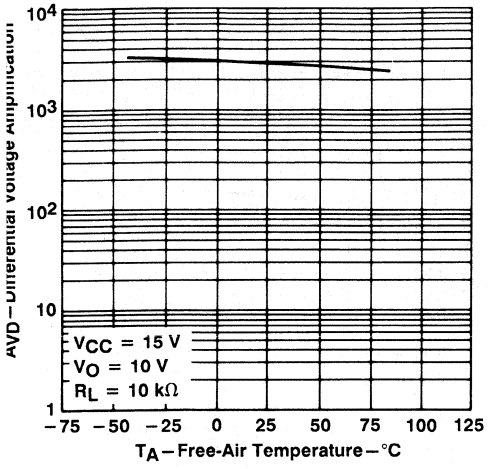


FIGURE 5

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

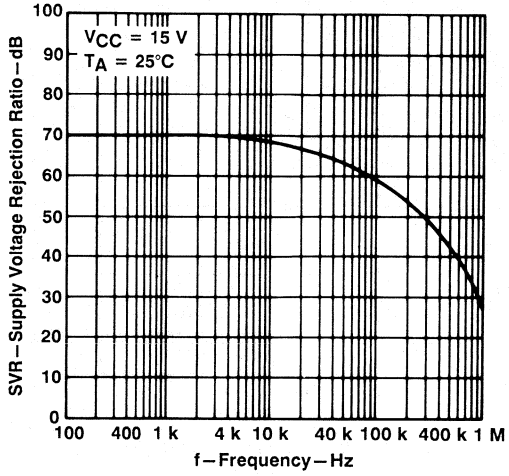


FIGURE 6

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

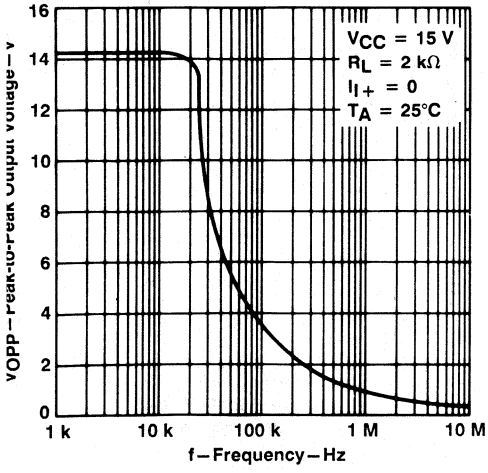


FIGURE 7

LM2900
SHORT-CIRCUIT OUTPUT CURRENT
(OUTPUT INTERNALLY HIGH)
vs
SUPPLY VOLTAGE

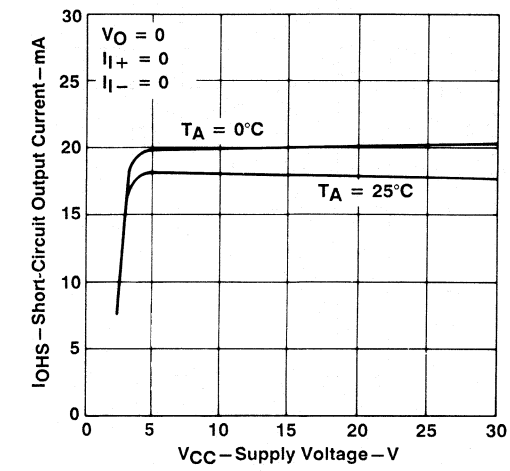


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT CURRENT
vs
SUPPLY VOLTAGE

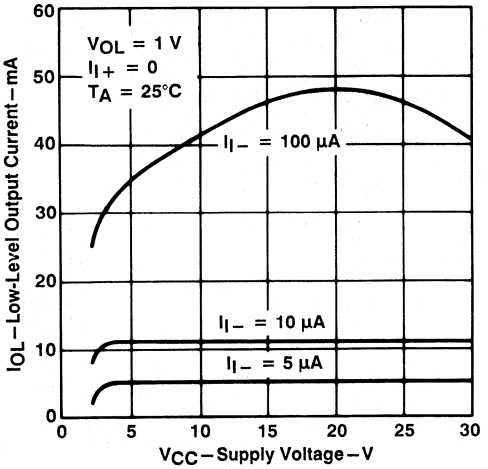


FIGURE 9

PULL-DOWN CURRENT
vs
SUPPLY VOLTAGE

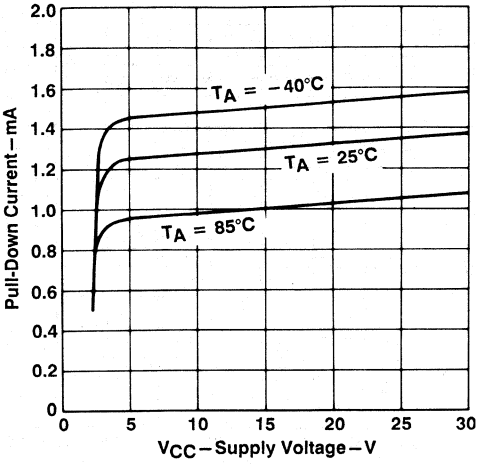


FIGURE 10

PULL-DOWN CURRENT
vs
FREE-AIR TEMPERATURE

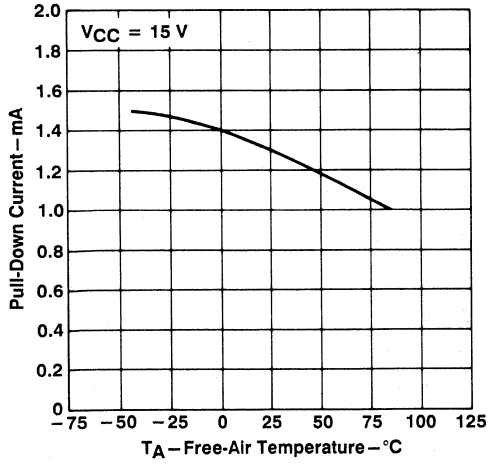


FIGURE 11

TOTAL SUPPLY CURRENT
vs
SUPPLY VOLTAGE

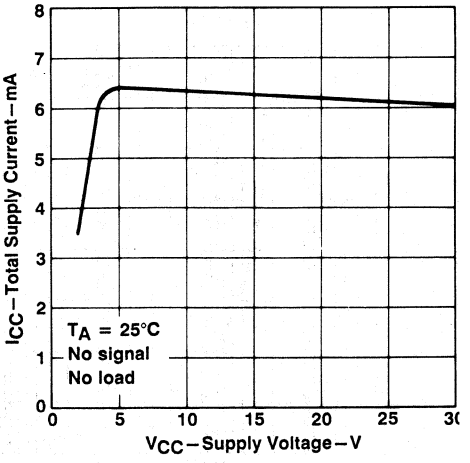


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

Norton (or current-differencing) amplifiers can be used in most standard general-purpose op-amp applications. Performance as a dc amplifier in a single-power-supply mode is not as precise as a standard integrated-circuit operational amplifier operating from dual supplies. Operation of the amplifier can be best be understood by noting that input currents are differenced at the inverting input terminal and this current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near (or even below) ground.

Internal transistors clamp negative input voltages at approximately −0.3 V but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately −100 μA.

Noise immunity of a Norton amplifier is less than that of standard bipolar amplifiers. Circuit layout is more critical since coupling from the output to the noninverting input can cause oscillations. Care must also be exercised when driving either input from a low-impedance source. A limiting resistor should be placed in series with the input lead to limit the peak input current. Current up to 20 mA will not damage the device but the current mirror on the noninverting input will saturate and cause a loss of mirror gain at higher current levels, especially at high operating temperatures.

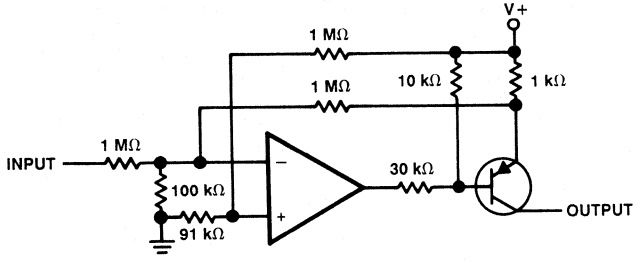


FIGURE 13. VOLTAGE-CONTROLLED CURRENT SOURCE

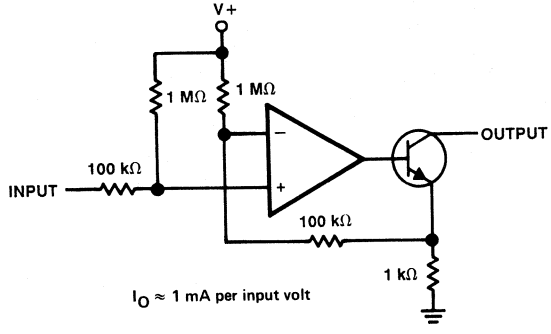
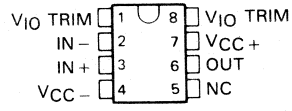


FIGURE 14. VOLTAGE-CONTROLLED CURRENT SINK

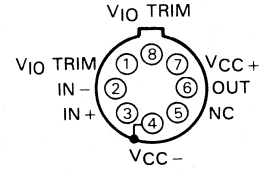
D3192, JANUARY 1989

- **Low Input Offset Voltage:**
  LT1001AM . . . 15 μV Max
  LT1001AC . . . 25 μV Max
  LT1001M, LT1001C . . . 60 μV Max
- **Low Offset Voltage Temperature Coefficient:**
  LT1001AM, LT1001AC . . . 0.6 μV/°C Max
  LT1001M, LT1001C . . . 1 μV/°C Max
- **Low Input Bias Current:**
  LT1001AM, LT1001AC . . . ±2 nA Max
  LT1001M, LT1001C . . . ±4 nA Max
- **Low Common-Mode Rejection Ratio:**
  LT1001AM, LT1001AC . . . 114 dB Min
  LT1001M, LT1001C . . . 110 dB Min
- **Low Supply Voltage Rejection Ratio:**
  LT1001AM, LT1001AC . . . 110 dB Min
  LT1001M, LT1001C . . . 106 dB Min
- **Low Power Dissipation:**
  LT1001AM, LT1001AC . . . 75 mW Max
  LT1001M, LT1001C . . . 80 mW Max
- **Low Peak-to-Peak Equivalent Input Noise Voltage . . . 0.3 μV Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



NC—No internal connection
Pin 4 (L package) is in electrical contact with the case.

description

The LT1001 is a precision operational amplifier suited for applications such as thermocouple amplifiers, strain gauge amplifiers, low-level signal processing, and high-accuracy data acquisition. In the design, processing, and testing of the device, particular attention has been paid to optimizing the entire distribution of several key parameters. The input offset voltage of all units is less than 60 μV, and the LT1001AM is specified at 15 μV maximum. Power dissipation is nearly halved compared to the most popular precision operational amplifiers without adversely affecting noise or speed performance. The output drive capability of the LT1001 is enhanced with voltage gain at a load current of 10 mA.

The specifications of the low-cost commercial-temperature device, the LT1001C, have been significantly improved when compared to equivalent grades of similar precision amplifiers. The input bias current, input offset current, and common-mode and supply voltage rejection ratios of the LT1001C offer performance previously attainable only with high-cost, selected grades of other devices.

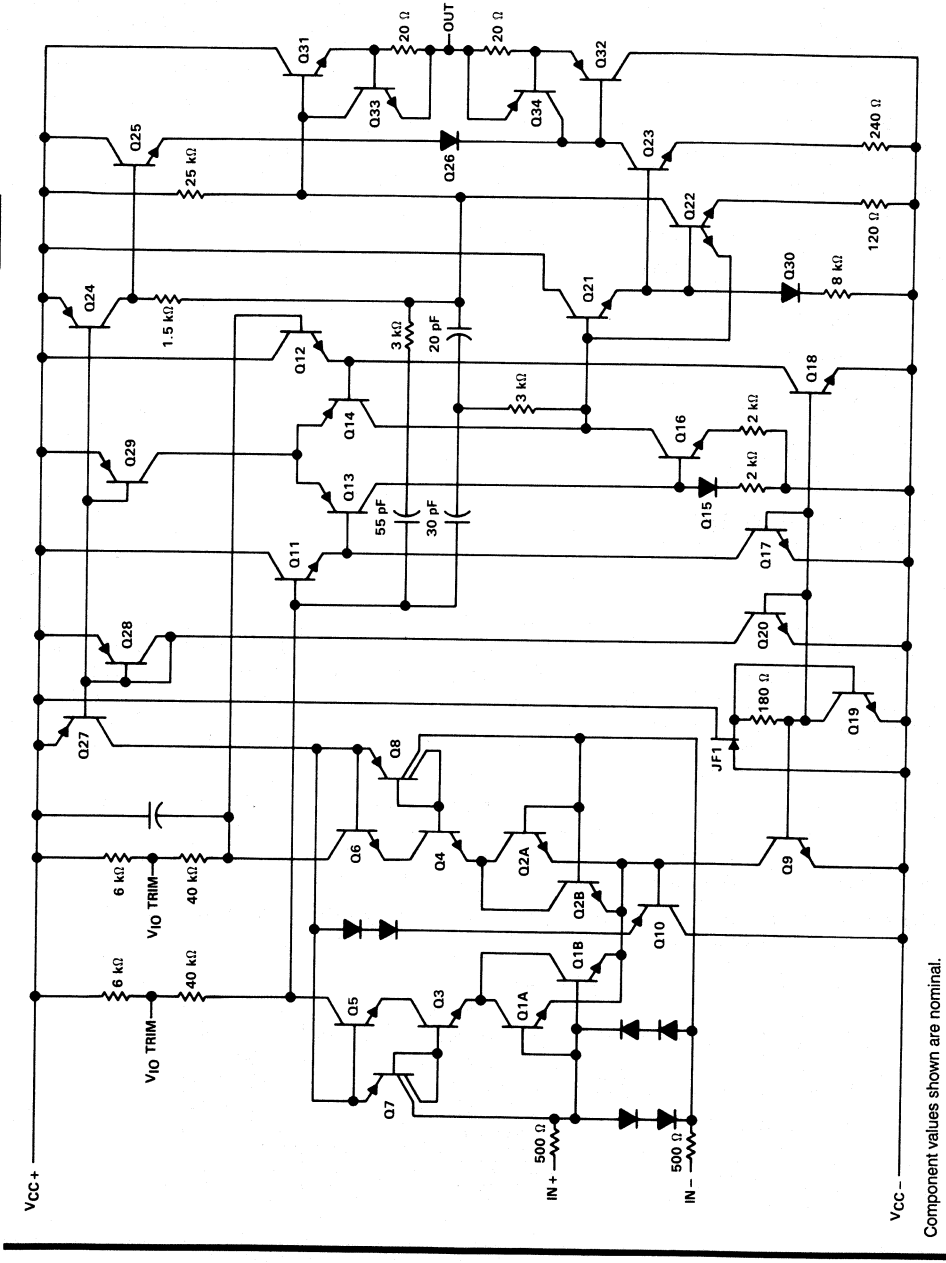
The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	60 μV	LT1001CD	LT1001CJG	LT1001CL	LT1001CP
	25 μV		LT1001ACJG	LT1001ACL	LT1001ACP
−55°C to 125°C	60 μV		LT1001MJG	LT1001ML	
	15 μV		LT1001AMJG	LT1001AML	

The D package is available in tape and reel. Add the suffix R to the device type (e.g., LT1001CDR).

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} . . . . . −22 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage range, V_I . . . . . ±22 V
Duration of short-circuit current at (or below) 25°C . . . . . unlimited
Continuous power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: M-suffix . . . . . −55°C to 125°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	145 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	200 mW

recommended operating conditions

		M-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 15$ V			±13			±13	V
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1001M			LT1001AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		18	60		7	15	µV
			−55°C to 125°C			160			60	
α_{VIO}	Average temperature coefficient of input offset voltage		−55°C to 125°C		0.3	1		0.2	0.6	µV/°C
	Long-term drift of input offset voltage	See Note 4			0.3	1.5		0.2	1	µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		0.4	3.8		0.3	2	nA
			−55°C to 125°C			7.6			4	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±0.7	±4		±0.5	±2	nA
			−55°C to 125°C			±8			±4	
V_{OH}	Maxiumum peak output voltage swing	R_L ≥ 2 kΩ	25°C	±13	±14		±13	±14		V
		R_L ≥ 1 kΩ		±12	±13.5		±12	±13.5		
		R_L ≥ 2 kΩ	−55°C to 125°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	400	800		450	800		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V		250	500		300	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	200			300			
r_{id}	Differential input resistance		25°C	15	80		30	100		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V	25°C	110	126		114	126		dB
			−55°C to 125°C	106			110			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±3 V to ±18 V	25°C	106	123		110	123		dB
			−55°C to 125°C	100			104			
P_D	Total power dissipation	No load	25°C		48	80		46	75	mW
		No load, $V_{CC\pm}$ = ± 3 V			4	8		4	6	
		No load	−55°C to 125°C			100			90	

NOTES: 3. The input offset voltage for all devices is measured with high-speed test equipment approximately 1 second after power is applied. The LT1001AM receives a 168-hour burn-in at 125°C or equivalent.

4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{IO} during the first 30 days is typically 2.5 µV.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1001M			LT1001AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L ≥ 2 kΩ		0.1	0.25		0.1	0.25		V/µs
ϕ_m	Phase margin at unity gain	A_V = 40 dB,	T_A = 25°C		60°			63°		
		R_S = 100 Ω,	T_A = MIN		63°			63°		
		C_L = 10 pF	T_A = MAX		57°			57°		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			0.3	0.6		0.3	0.6	µV
V_n	Equivalent input noise voltage	f = 10 Hz			10.5	18		10.3	18	nV/√Hz
		f = 1 MHz			9.8	11		9.6	11	
GBW	Gain bandwidth product			0.4	0.8		0.4	0.8		MHz

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1001C			LT1001AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 5	25°C		18	60		10	25	µV
			0°C to 70°C			110			60	
α_{VIO}	Average temperature coefficient of input offset voltage		0°C to 70°C		0.3	1		0.2	0.6	µV/°C
	Long-term drift of input offset voltage	See Note 4			0.3	1.5		0.2	1	µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		0.4	3.8		0.3	2	nA
			0°C to 70°C			5.3			3.5	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±0.7	±4		±0.5	±2	nA
			0°C to 70°C			±5.5			±3.5	
V_{OH}	Maximum peak output voltage swing	R_L ≥ 2 kΩ	25°C	±13	±14		±13	±14		V
		R_L ≥ 1 kΩ		±12	±13.5		±12	±13.5		
		R_L ≥ 2 kΩ	0°C to 70°C	±12.5			±12.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±12 V	25°C	400	800		450	800		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V		250	500		300	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	0°C to 70°C	250			350			
r_{id}	Differential input resistance		25°C	15	80		30	100		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V	25°C	110	126		114	126		dB
			0°C to 70°C	106			110			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±3 V to ±18 V	25°C	106	123		110	123		dB
			0°C to 70°C	103			106			
P_D	Total power dissipation	No load	25°C		48	80		46	75	mW
		No load, $V_{CC\pm}$ = ±3 V			4	8		4	6	
		No load	0°C to 70°C			90			85	

Notes: 4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, the change in V_{IO} during the first 30 days is typically 2.5 µV.

5. The input offset voltage for all devices is measured with high-speed test equipment approximately 1 second after power is applied.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		LT1001C			LT1001AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L ≥ 2 kΩ		0.1	0.25		0.1	0.25		V/µs
ϕ_m	Phase margin at unity gain	A_V = 40 dB,	T_A = 25°C		60°			63°		
		R_S = 100 Ω,	T_A = MIN		63°			63°		
		C_L = 10 pF	T_A = MAX		57°			57°		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz			0.3	0.6		0.3	0.6	µV
V_n	Equivalent input noise voltage	f = 10 Hz			10.5	18		10.3	18	nV/√Hz
		f = 1 MHz			9.8	11		9.6	11	
GBW	Gain bandwidth product			0.4	0.8		0.4	0.8		MHz

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

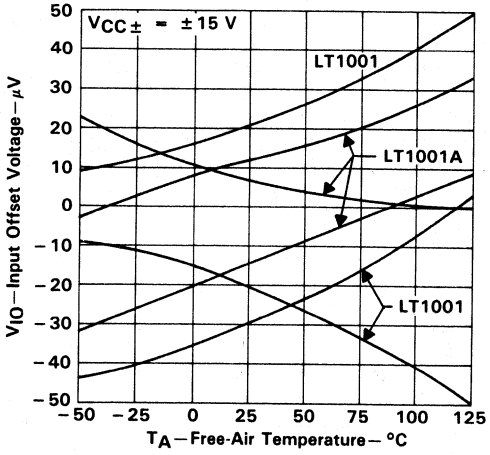


FIGURE 1

WARM-UP CHANGE
IN INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

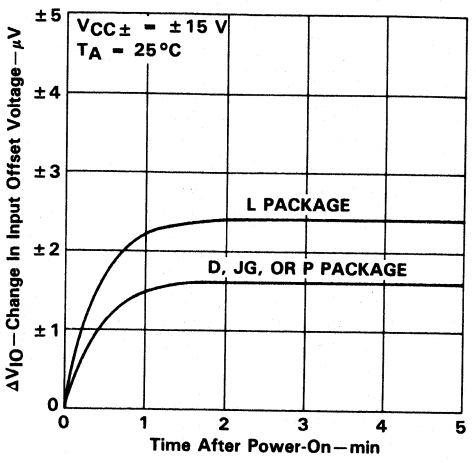


FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

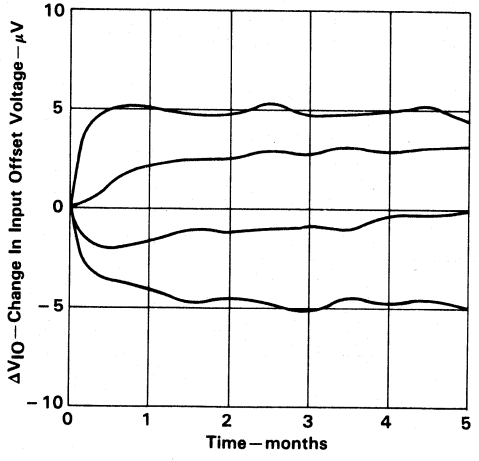


FIGURE 3

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
and INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

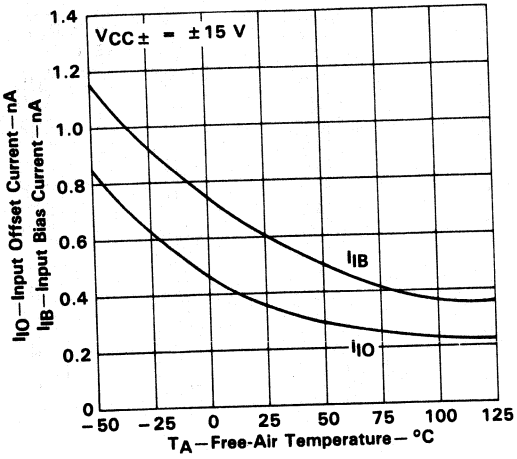


FIGURE 4

INPUT BIAS CURRENT
vs
DIFFERENTIAL INPUT VOLTAGE

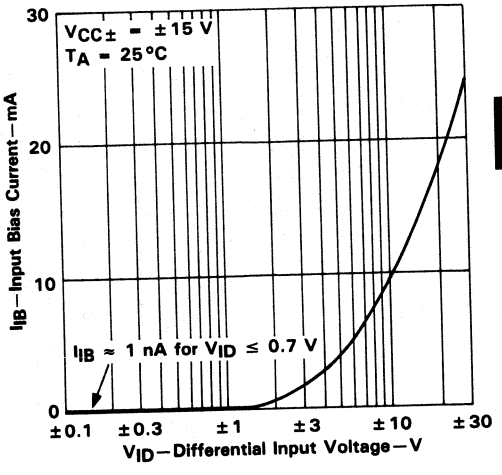


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

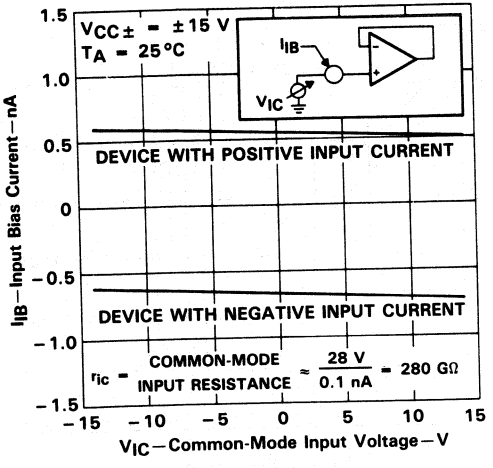


FIGURE 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

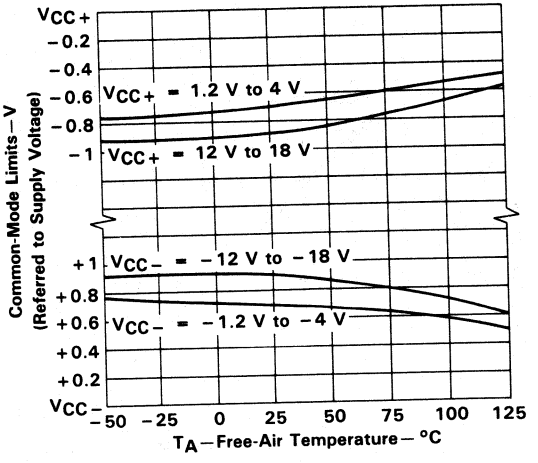


FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK
OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

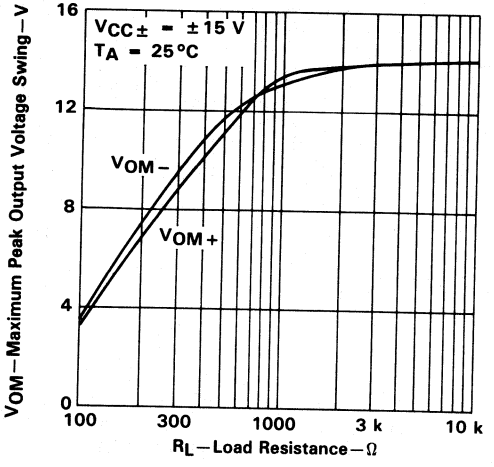


FIGURE 8

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE SWING
vs
FREQUENCY

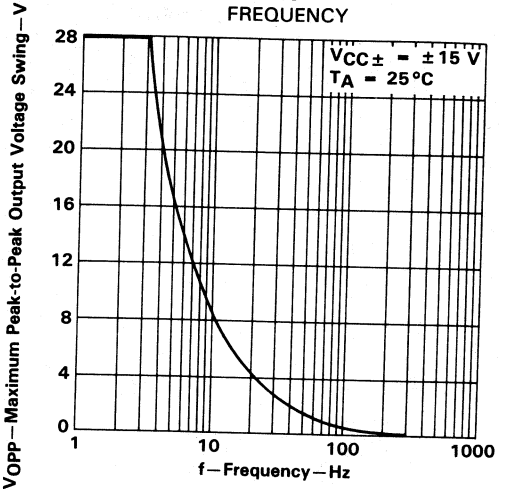


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

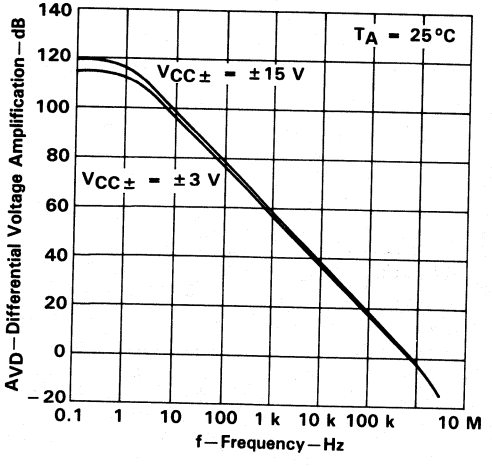


FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

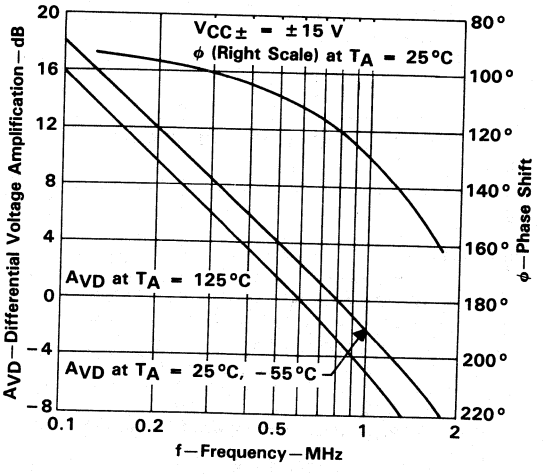


FIGURE 11

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

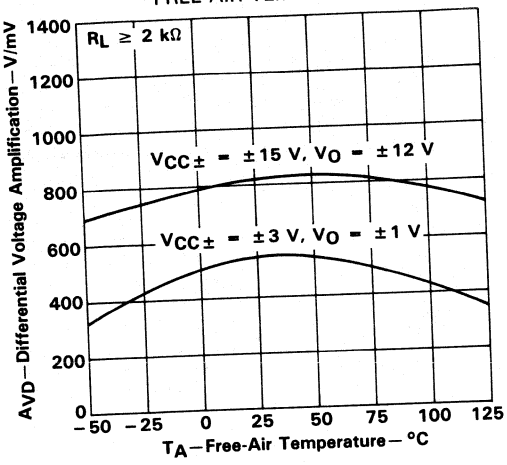


FIGURE 12

OUTPUT IMPEDANCE
vs
FREQUENCY

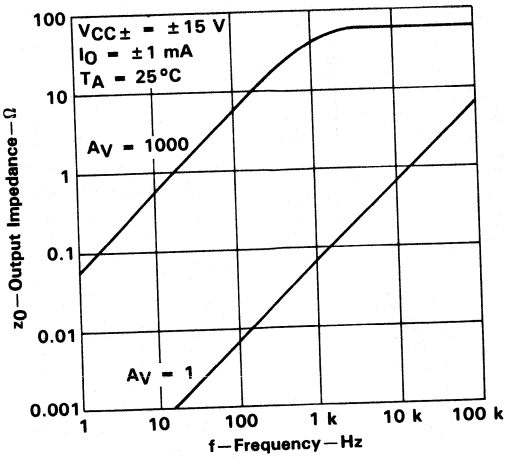


FIGURE 13

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

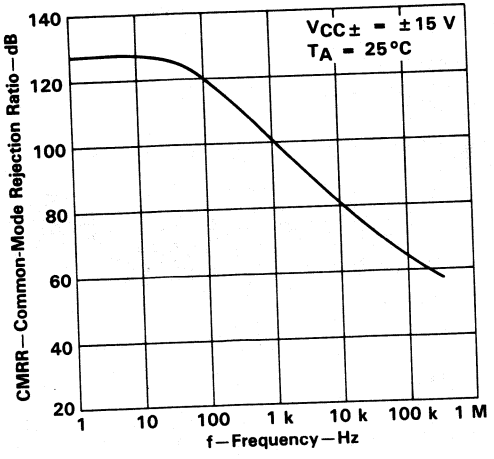


FIGURE 14

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

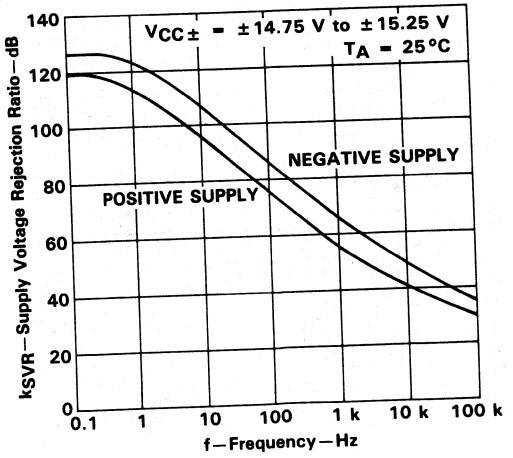


FIGURE 15

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

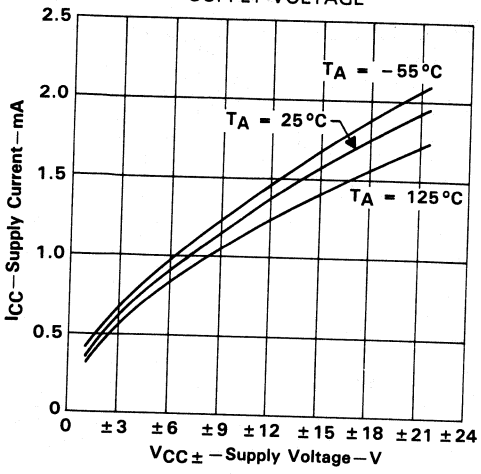


FIGURE 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

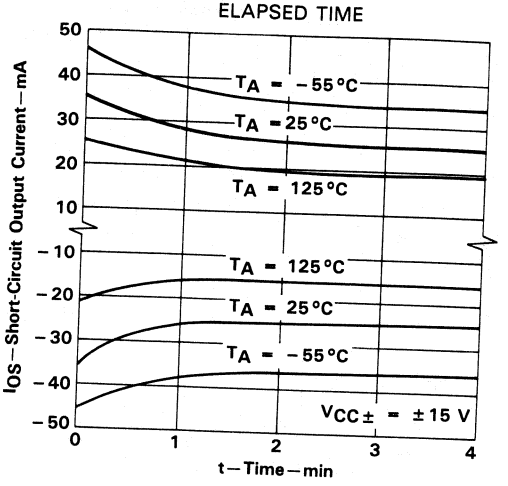


FIGURE 17

EQUIVALENT INPUT NOISE VOLTAGE
and EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

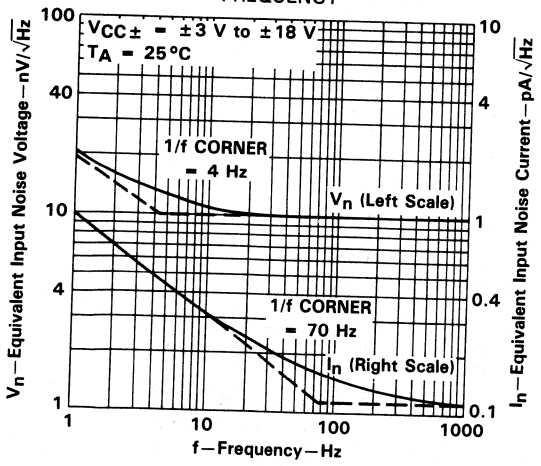


FIGURE 18

OUTPUT NOISE VOLTAGE
OVER A
10-SECOND PERIOD

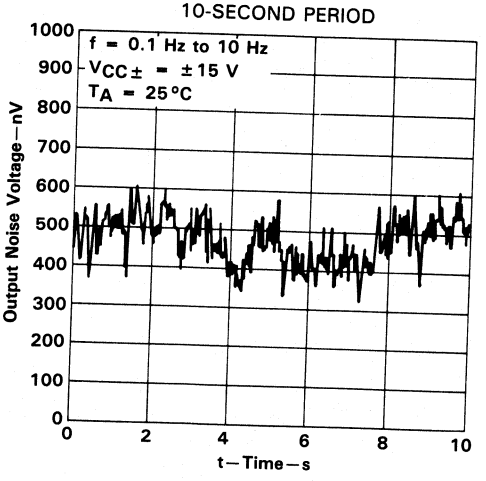


FIGURE 19

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

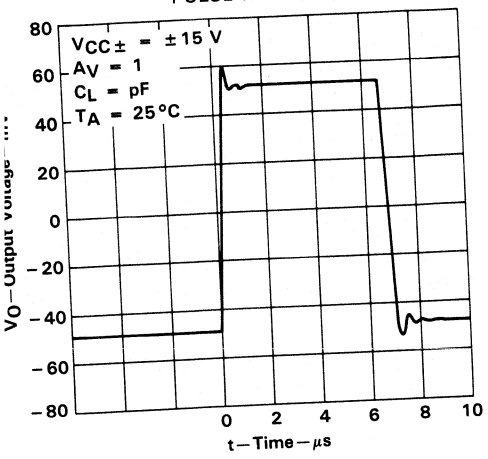


FIGURE 20

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

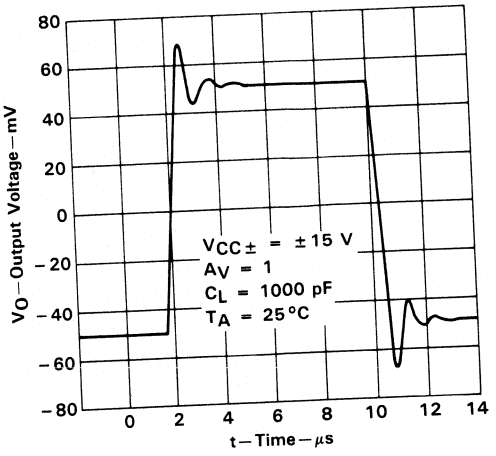


FIGURE 21

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE-RESPONSE

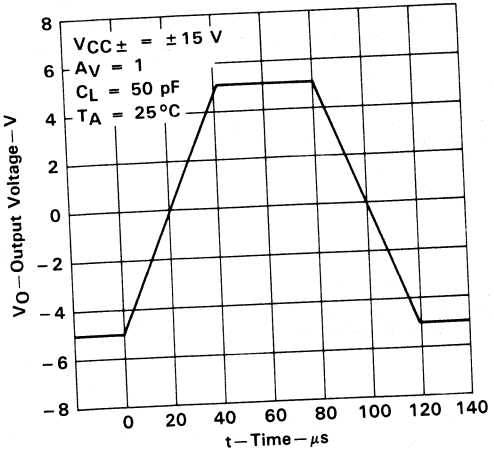


FIGURE 22

VOLTAGE-FOLLOWER OVERSHOOT
vs
LOAD CAPACITANCE

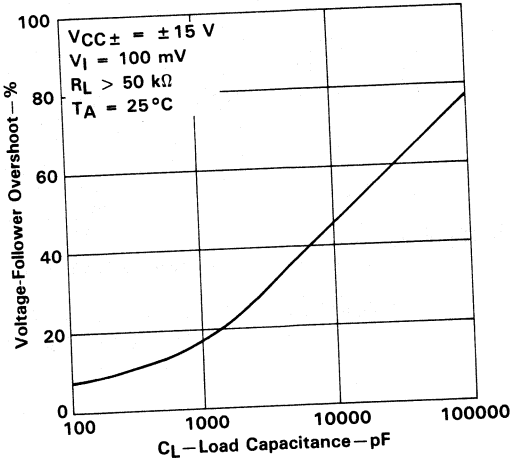
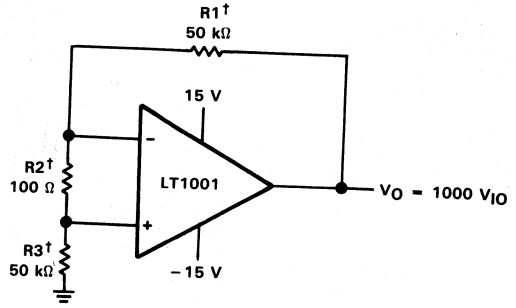


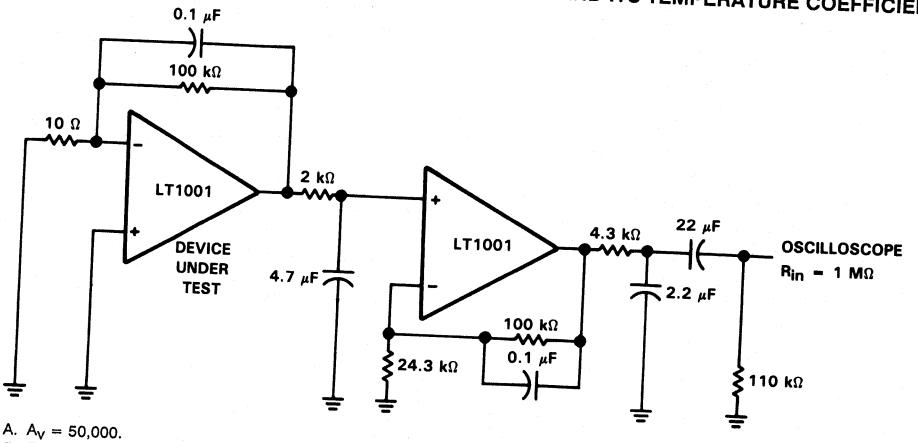
FIGURE 23

PARAMETER MEASUREMENT INFORMATION



†Resistors must have low thermoelectric potential.
NOTE: This circuit is also used as the burn-in configuration for the LT1001 with supply voltages increased to ±20 V, R1 = R3 = 10 kΩ R2 = 200 Ω, and A_V = 100.

FIGURE 24. TEST CIRCUIT FOR INPUT OFFSET VOLTAGE AND ITS TEMPERATURE COEFFICIENT



NOTES: A. A_V = 50,000.
B. The device under test should be warmed up for three minutes and shielded from air currents.

FIGURE 25. TEST CIRCUIT FOR 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE (MEASURED OVER A 10-SECOND INTERVAL)

TYPICAL APPLICATION DATA

plication notes

The LT1001 series units may be inserted directly into OP-07 or LM108A sockets with or without removing external frequency compensation or nulling components.

The LT1001 is specified over a wide range of supply voltages from ±3 V to ±18 V. Operation with lower supply voltages (e.g., two Ni-Cad batteries) is possible down to ±1.2 V. However, with ±1.2-V supplies, the device is stable only in closed-loop gains of 2 or higher (or inverting gains of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent temperature coefficient of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

nput offset voltage adjustment

The input offset voltage and temperature coefficient of the LT1001 are permanently trimmed to a low level at wafer test. However, if further adjustment of V_{IO} is necessary, nulling with a 10-kΩ or 20-kΩ potentiometer will not degrade the temperature coefficient. Trimming to a value other than zero creates a temperature coefficient change of (V_{IO}/300) μV/°C. For example, if V_{IO} is adjusted to 300 μV, the change in the temperature coefficient will be 1 μV/°C. The adjustment range with a 10-kΩ or 20-kΩ potentiometer is approximately ±2.5 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 26 has an approximate null range of ±100 μV.

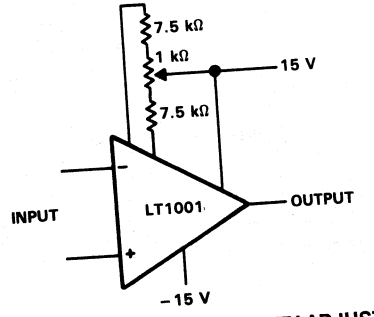
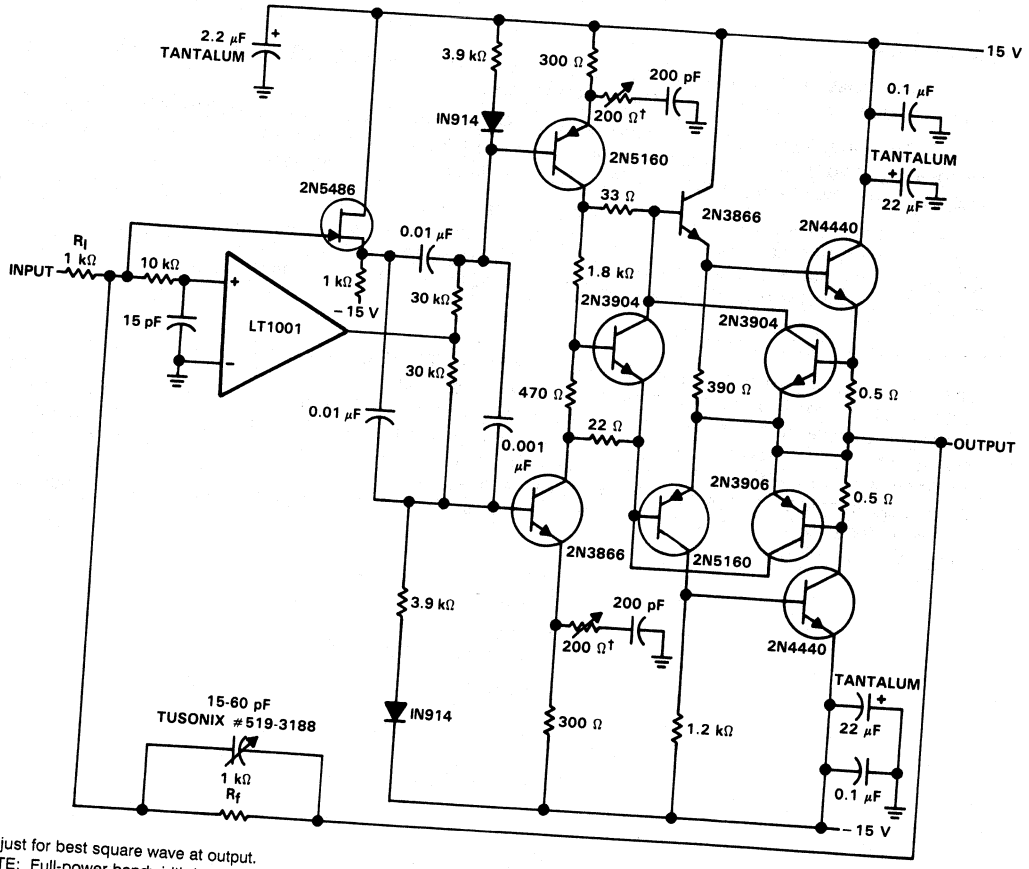


FIGURE 26. IMPROVED SENSITIVITY ADJUSTMENT

TYPICAL APPLICATION DATA



†Adjust for best square wave at output.
NOTE: Full-power bandwidth is 8 MHz.

FIGURE 27. DC-STABILIZED 1000-V/μs OPERATIONAL AMPLIFIER

TYPICAL APPLICATION DATA

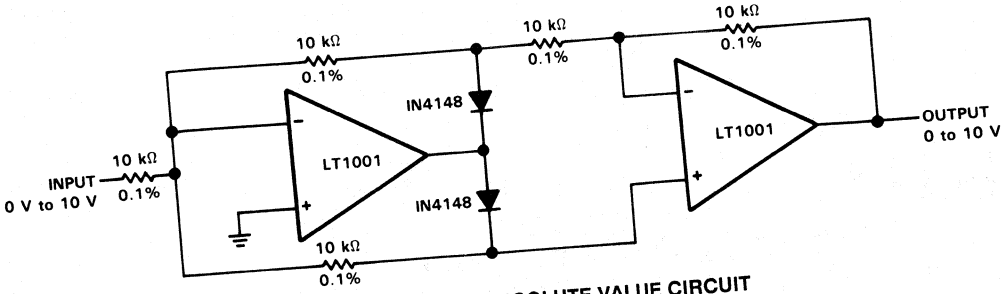


FIGURE 28. PRECISION ABSOLUTE VALUE CIRCUIT

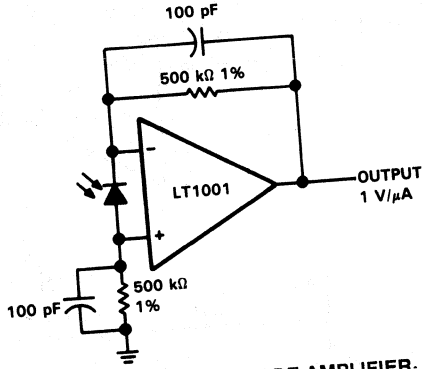


FIGURE 29. PHOTODIODE AMPLIFIER

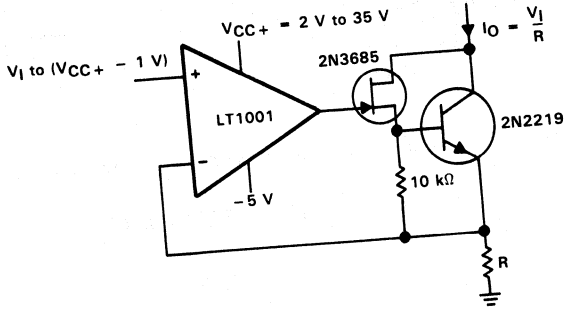
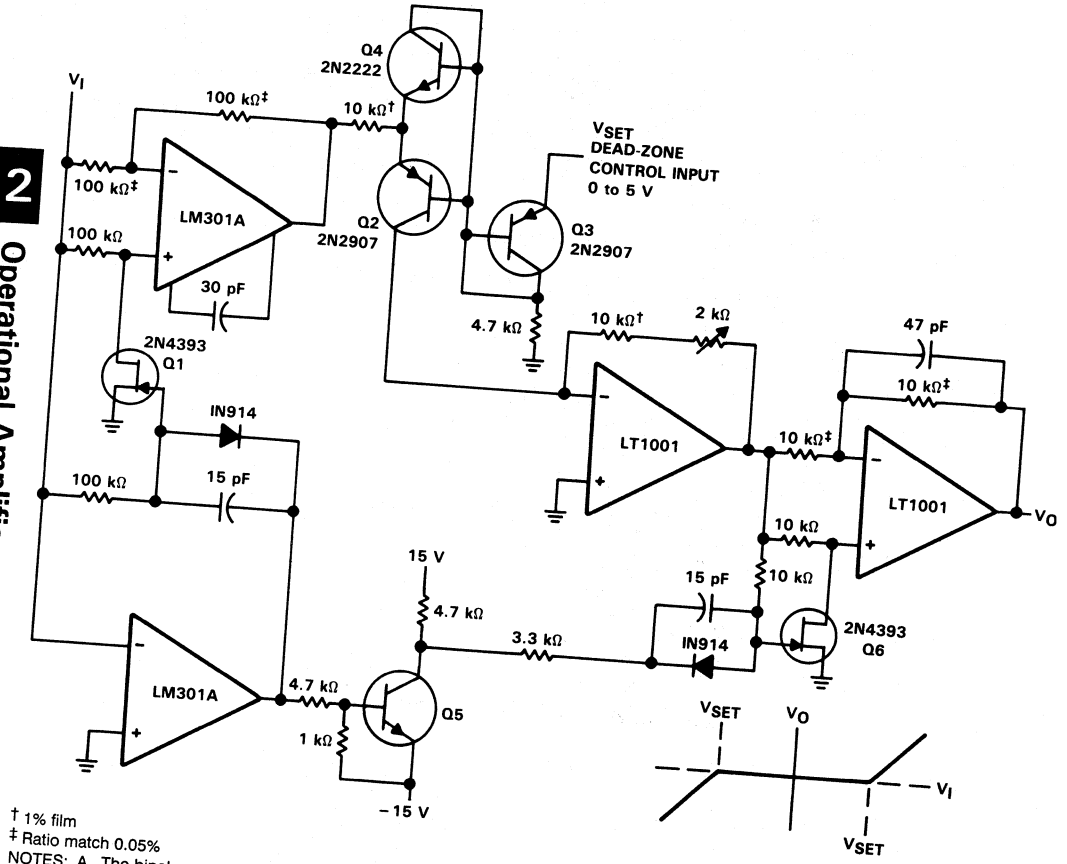


FIGURE 30. PRECISION CURRENT SINK

TYPICAL APPLICATION DATA



† 1% film
‡ Ratio match 0.05%
NOTES: A. The bipolar symmetry for this application is excellent because one device, Q2, sets both limits.
B. Q2-Q5 are a CA 3096 transistor array.

FIGURE 31. DEAD-ZONE GENERATOR

TYPICAL APPLICATION DATA

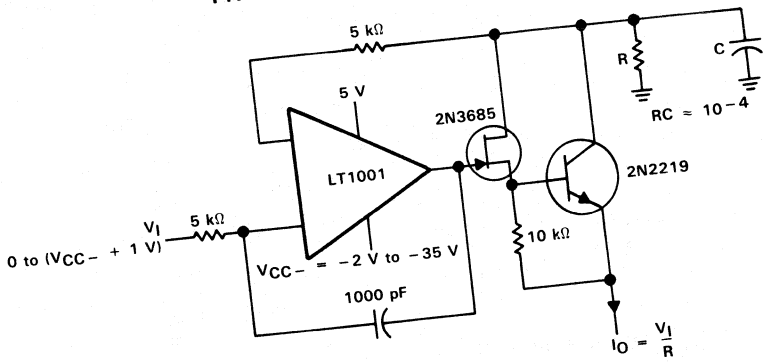
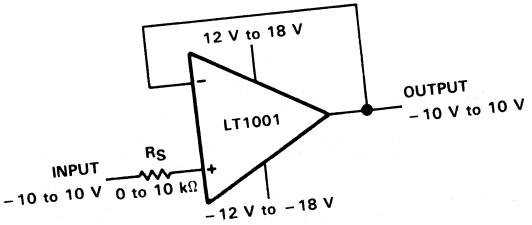


FIGURE 32. PRECISION CURRENT SOURCE

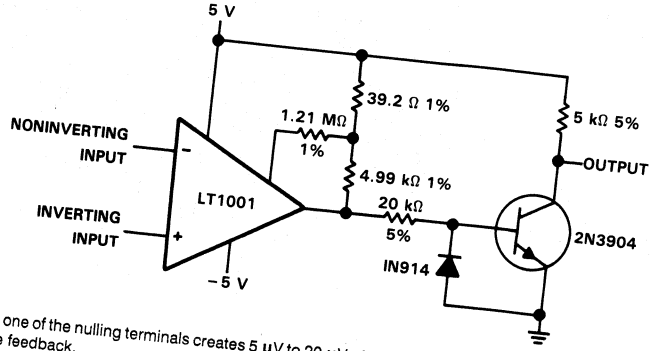


ERROR	OUTPUT ACCURACY			
	LT1001AM T_A = 25°C MAX	LT1001C T_A = 25°C MAX	LT1001AM T_A = −55°C to 125°C MAX	LT1001C T_A = 0°C to 70°C MAX
Input Offset Voltage	15 µV	60 µV	60 µV	110 µV
Input Bias Current	20 µV	40 µV	40 µV	55 µV
Common-Mode Rejection Ratio	20 µV	30 µV	30 µV	50 µV
Supply Voltage Rejection Ratio	18 µV	30 µV	36 µV	42 µV
Differential Voltage Amplification	22 µV	25 µV	33 µV	40 µV
Worst-case Sum	95 µV	185 µV	199 µV	297 µV
Percent of Full Scale (= 20 V)	0.0005%	0.0009%	0.0010%	0.0015%

NOTE: The contributing error terms are due to input offset voltage, input bias current, voltage gain, common-mode rejection ratio, and supply voltage rejection ratio. The worst-case specifications are given in the above table.

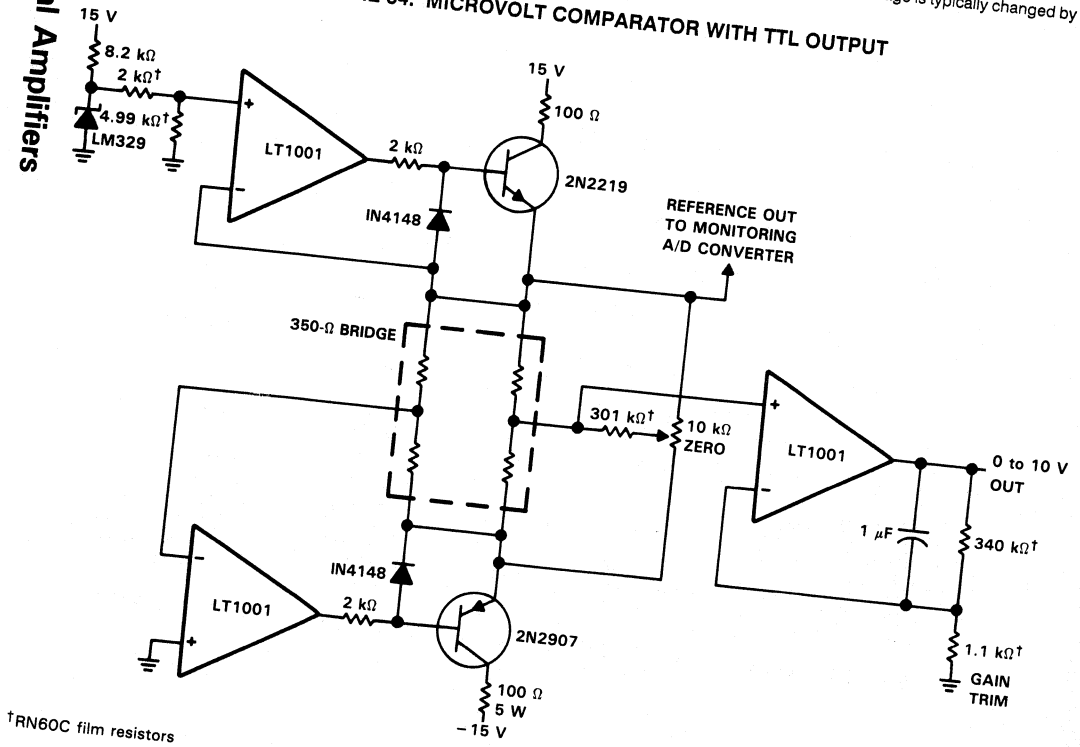
FIGURE 33. LARGE-SIGNAL VOLTAGE FOLLOWER WITH 0.001% WORST-CASE ACCURACY

TYPICAL APPLICATION DATA



NOTE: Positive feedback to one of the nulling terminals creates 5 μV to 20 μV of hysteresis. The input offset voltage is typically changed by les than 5 μV due to the feedback.

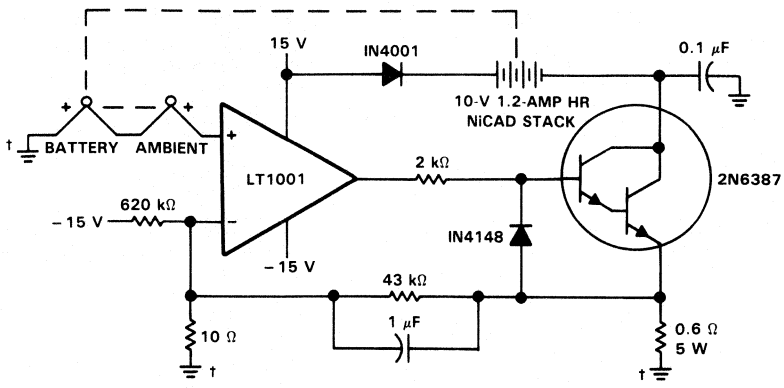
FIGURE 34. MICROVOLT COMPARATOR WITH TTL OUTPUT



†RN60C film resistors

FIGURE 35. STRAIN-GAUGE SIGNAL CONDITIONER WITH BRIDGE EXCITATION

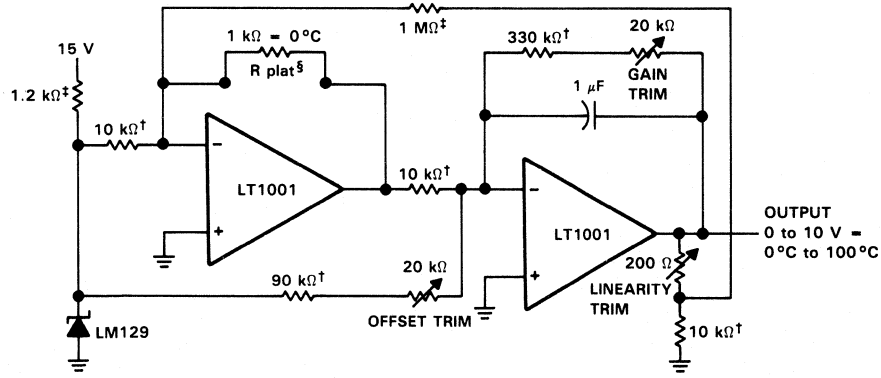
TYPICAL APPLICATION DATA



†Single point ground thermocouples are 40 μV/°C chromel-alumel (type K).

NOTE: This circuit uses the temperature difference between the battery pack mounted thermocouple and the ambient thermocouple to set the battery charge current. The peak charging current is 1 A.

FIGURE 36. THERMALLY CONTROLLED NICAD CHARGER



†ULTRONIX 105A wirewound

‡1% film

§Platinum RTD 118MF (Rosemount, Inc.)

NOTE: Trim sequence: trim offset (0°C = 1000 Ω), trim linearity (35°C = 1138.7 Ω), trim gain (100°C = 1392.6 Ω). Repeat until all three points are fixed with ±0.025°C.

FIGURE 37. LINEARIZED PLATINUM RESISTANCE THERMOMETER WITH ±0.025°C ACCURACY FOR T_A = 0°C TO 100°C

D3195, FEBRUARY 1989

- **Maximum Equivalent Input Noise Voltage:**
  3.8 nV/$\sqrt{Hz}$ at 1 kHz
  4.5 nV/$\sqrt{Hz}$ at 10 Hz
- **Low Peak-to-Peak Equivalent Input Noise Voltage: 60 nV Typ from 0.1 Hz to 10 Hz**
- **Slew Rate (LT1037 and LT1037A): 11 V/μs Min**

LT1007A and LT1037A Specifications:

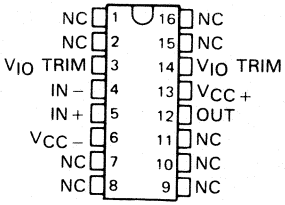
- **High Voltage Amplification:**
  7 V/μV Min, R_L = 2 kΩ
  3 V/μV Min, R_L = 600 Ω
- **Low Input Offset Voltage 25 μV Max**
- **Low Input Offset Voltage Temperature Coefficient: 0.6 μV/°C Max**
- **Common-Mode Rejection Ratio: 117 dB Min**

description

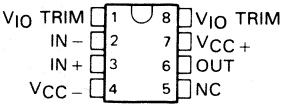
These monolithic operational amplifiers feature extremely low noise performance and outstanding precision and speed specifications. The typical differential voltage amplification (at T_A = 25°C) of these devices is an extremely high 20 V/μV driving a 2-kΩ load to ±12 V and 12 V/μV driving a 600-Ω load to ±10 V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of even the lowest-cost grades (the LT1007C and the LT1037C) have been greatly improved compared to equivalent grades of competing amplifiers.

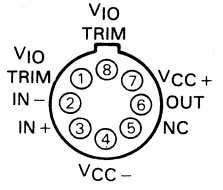
DW SMALL-OUTLINE PACKAGE
(TOP VIEW)



JG AND P
DUAL-IN-LINE PACKAGES
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



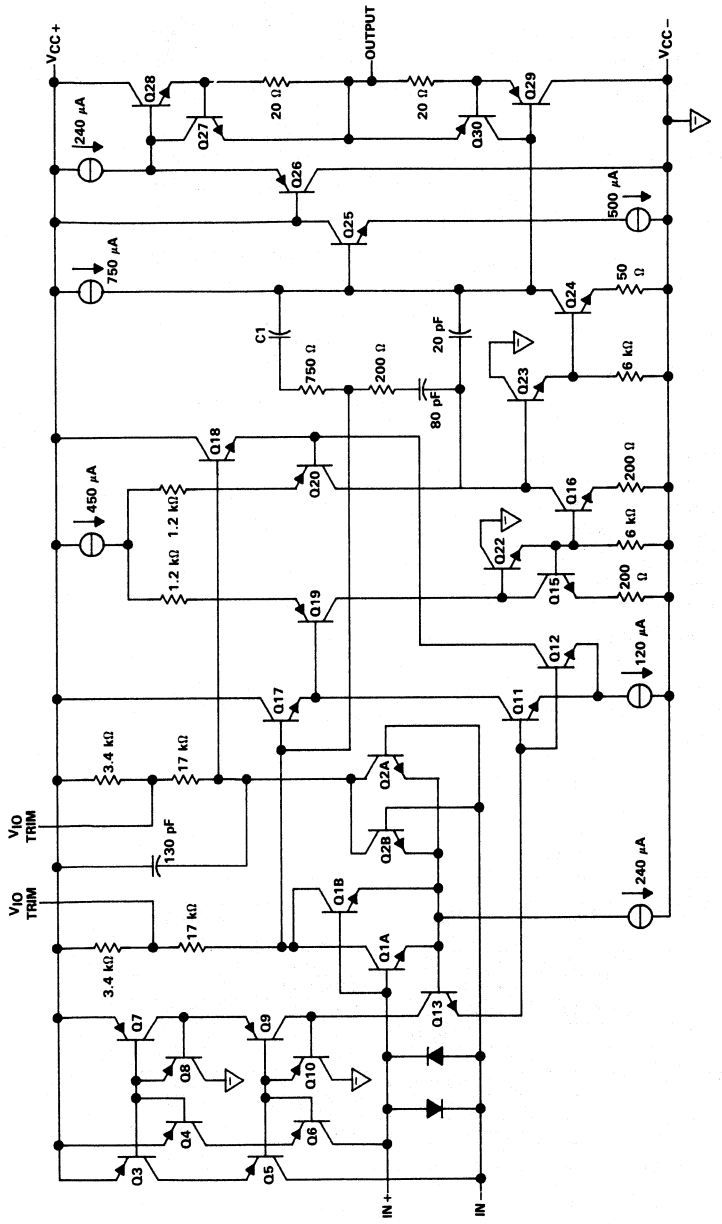
Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (DW)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	60 μV	LT1007CDW	LT1007CJG	LT1007CL	LT1007CP
	25 μV	—	LT1007ACJG	LT1007ACL	LT1007ACP
	60 μV	LT1037CDW	LT1037CJG	LT1037CL	LT1037CP
	25 μV	—	LT1037ACJG	LT1037ACL	LT1037ACP
−55°C to 125°C	60 μV	—	LT1007MJG	LT1007ML	LT1007MP
	25 μV	—	LT1007AMJG	LT1007AML	LT1007AMP
	60 μV	—	LT1037MJG	LT1037ML	LT1037MP
	25 μV	—	LT1037AMJG	LT1037AML	LT1037AMP

The DW packages are available taped and reeled. Add the suffix "R" to the device type. (e.g., LT1007CDWR).

schematic



C1 = 110 pF for LT1007
C1 = 12 pF for LT1037
All component values shown are nominal.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} . . . . . −22 V
Input voltage . . . . . $V_{CC\pm}$
Duration of output short-circuit . . . . . Unlimited
Differential input current (see Note 2) . . . . . ±25 mA
Power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range:
LT1007M, LT1007AM, LT1037M, LT1037AM . . . . . −55°C to 125°C
LT1007C, LT1007AC, LT1037C, LT1037AC . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW and P packages . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG and L packages . . . . . 300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs, unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	N/A	N/A
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	338 mW	N/A
P	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		LT1007M, LT1037M			LT1007C, LT1037C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Input voltage, V_I	T_A = 25°C	±11			±11			V
	T_A = full range	±10.3			±10.5			V
Operating free-air temperatue, T_A		−55		125	0		70	°C

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS	T_A	LT1007, LT1037			LT1007A, LT1037A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	60		10	25	μV
			−55°C to 125°C			160			60	
αV_{IO}	Average temperature coefficient of input offset voltage		−55°C to 125°C			1			0.6	μV/°C
I_{IO}	Input offset current		25°C		12	50		7	30	nA
			−55°C to 125°C			85			50	
I_{IB}	Input bias current		25°C		±15	±55		±10	±35	nA
			−55°C to 125°C			±95			±60	
V_{OM}	Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
		R_L = 600 Ω	25°C	±10.5	±12.5		±11	±12.5		
		R_L = 2 kΩ	−55°C to 125°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/μV
		$R_L \geq$ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
		$R_L \geq$ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	−55°C to 125°C	2			3			
		$R_L \geq$ 1 kΩ, V_O = ±10 V	−55°C to 125°C	1.5			2			
$r_{i(CM)}$	Common-mode input resistance		25°C		5			7		GΩ
r_o	Open-loop output resistance		25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		117	130		dB
		V_{IC} = ±10.3 V	−55°C to 125°C	104			112			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	106	126		110	130		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	−55°C to 125°C	100			104			
P_D	Power dissipation	LT1007M, LT1007AM	25°C		80	140		80	120	mW
		LT1037M, LT1037AM	25°C		85	140		80	130	
			−55°C to 125°C			170			150	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS	T_A	LT1007, LT1037			LT1007A, LT1037A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	60		10	25	μV
			0°C to 70°C			110			50	
αV_{IO}	Average temperature coefficient of input offset voltage		0°C to 70°C			1			0.6	μV/°C
I_{IO}	Input offset current		25°C		12	50		7	30	nA
			0°C to 70°C			70			40	
I_{IB}	Input bias current		25°C		±15	±55		±10	±35	nA
			0°C to 70°C			±75			±45	
V_{OM}	Peak output voltage swing	R_L = 2 kΩ	25°C	±12.5	±13.5		±13	±13.8		V
		R_L = 600 Ω	25°C	±10.5	±12.5		±11	±12.5		
		R_L = 2 kΩ	0°C to 70°C	±12			±12.5			
A_{VD}	Large-signal differential voltage amplification	$R_L \geq$ 2 kΩ, V_O = ±12 V	25°C	5	20		7	20		V/μV
		$R_L \geq$ 1 kΩ, V_O = ±10 V	25°C	3.5	16		5	16		
		$R_L \geq$ 600 Ω, V_O = ±10 V	25°C	2	12		3	12		
		$R_L \geq$ 2 kΩ, V_O = ±10 V	0°C to 70°C	2.5			4			
		$R_L \geq$ 1 kΩ, V_O = ±10 V	0°C to 70°C	2			2.5			
$r_{i(CM)}$	Common-mode input resistance		25°C		5			7		GΩ
r_o	Open-loop output resistance		25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		117	130		dB
		V_{IC} = ±10.5 V	0°C to 70°C	106			114			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	106	126		110	130		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	0°C to 70°C	102			106			
P_D	Power dissipation	LT1007M, LT1007AM	25°C		80	140		80	120	mW
		LT1037M, LT1037AM	25°C		85	140		80	130	
			0°C to 70°C			160			144	

NOTE 3: V_{IO} measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

operating characteristics $V_{CC\pm}$ = ± 15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	LT1007/LT1007A			LT1037/LT1037A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$R_L \geq 2$ kΩ, $A_{VD} \geq 1$ (LT1007, LT1007A)	1.7	2.5		11	15		V/μs
		$R_L \geq 2$ kΩ, $A_{VD} \geq 5$ (LT1037, LT1037A)							
V_{NPP}	Peak-to-peak equivalent input noise voltage	0.1 Hz to 10 Hz, See Note 4		0.06	0.13		0.06	0.13	μV
V_n	Equivalent input noise voltage	10 Hz		2.8	4.5		2.8	4.5	nV/√Hz
		1 kHz		2.5	3.8		2.5	3.8	
I_n	Equivalent input noise current	10 Hz, See Note 5		1.5	4		1.5	4	pA/√Hz
		1 kHz, See Note 5		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	100 kHz	5	8					MHz
		10 kHz, $A_V \geq 15$				45	60		

NOTES: 4. See the test circuit and frequency response curve for 0.1 Hz to 10 Hz noise (Figure 39) in the Applications Information section.
5. See the test circuit for current noise measurement (Figure 40) in the Applications Information section.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power on	2
		vs Time (long-term stability)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
		over common-mode range	6
	Common-mode limit voltage	vs Free-air temperature	7
V_{OM}	Maximum peak output voltage swing	vs Load resistance	8
		vs Frequency	9
A_{VD}	Differential voltage amplification	vs Frequency	10
		vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
		vs Temperature	13
		vs Load resistance	14
		vs Supply voltage	15
		at 2 kΩ and 600 Ω	16
V_{ID}	Differential input voltage	vs Output voltage	16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply voltage rejection ratio	vs Frequency	18
SR	Slew rate	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
ϕ	Phase shift	vs Frequency (LT1007)	11
		vs Frequency (LT1037)	12
ϕ_m	Phase margin	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
V_n	Equivalent input noise voltage	vs Free-air temperature	21
		vs Time (0.01-Hz to 1-Hz noise)	22
		vs Frequency	23
		vs Bandwidth	24
		vs Supply voltage	25
I_n	Equivalent input noise current	vs Frequency	26
	Total noise	vs Source resistance	27
GBW	Gain bandwidth product	vs Free-air temperature (LT1007)	19
		vs Free-air temperature (LT1037)	20
I_{OS}	Short-circuit output current	vs Time (from short to GND)	28
I_{CC}	Supply current	vs Supply voltage	29
z_o	Closed-loop output impedance	vs Frequency	30
	Pulse response (LT1007)	Small-signal (C_{load} = 15 pF)	31
		Large-signal	32
	Pulse response (LT1037)	Small-signal (C_{load} = 15 pF)	33
		Large-signal	34

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

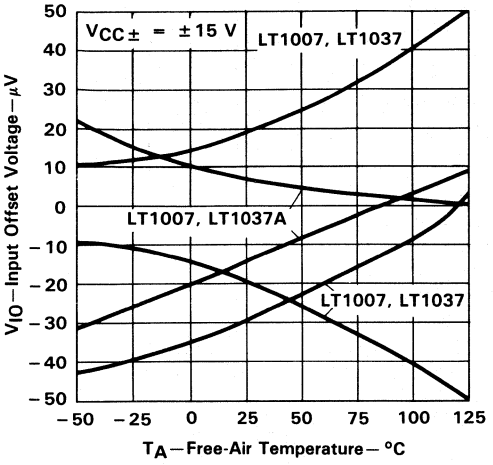


FIGURE 1

INPUT OFFSET VOLTAGE CHANGE
vs
TIME AFTER POWER ON

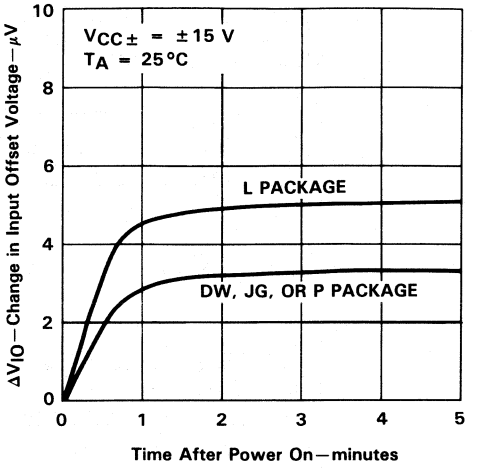


FIGURE 2

LONG TERM STABILITY OF
INPUT OFFSET VOLTAGE
FOR FOUR REPRESENTATIVE UNITS

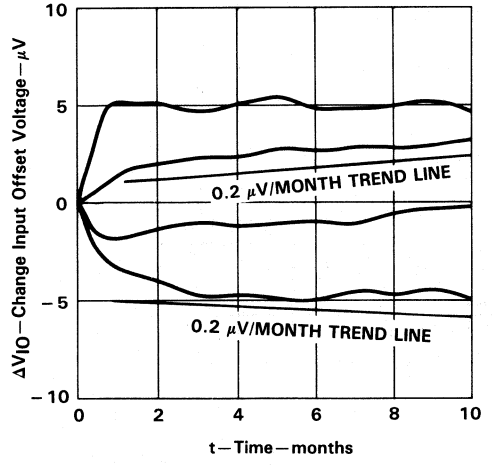


FIGURE 3

INPUT OFFSET CURRENT
vs
TEMPERATURE

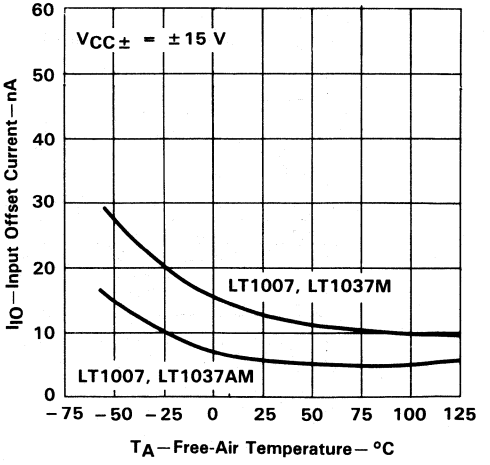


FIGURE 4

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

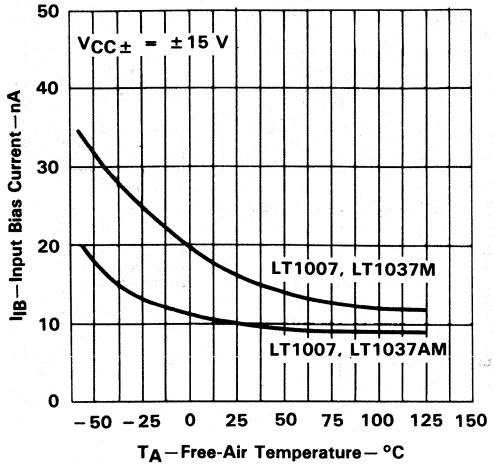


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

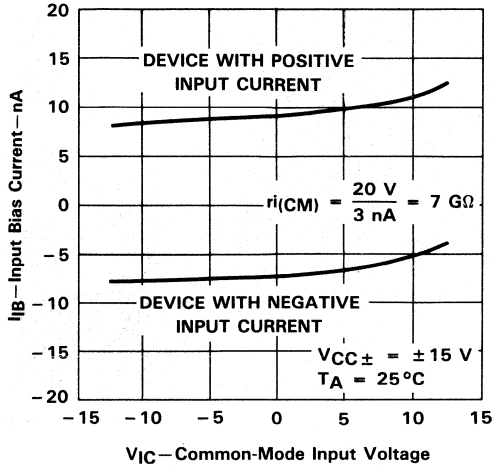


FIGURE 6

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

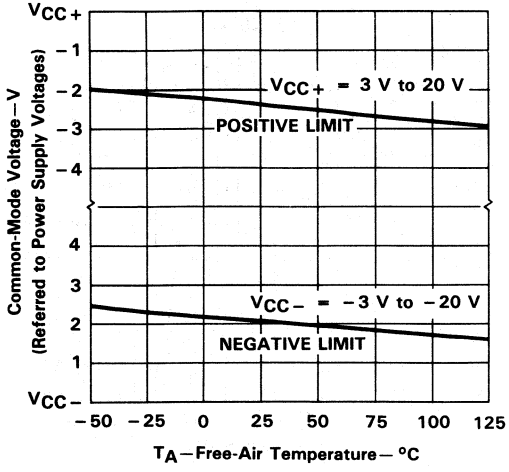


FIGURE 7

PEAK OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

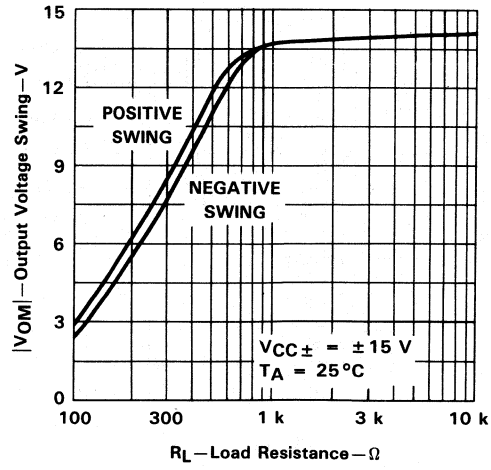


FIGURE 8

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
FREQUENCY

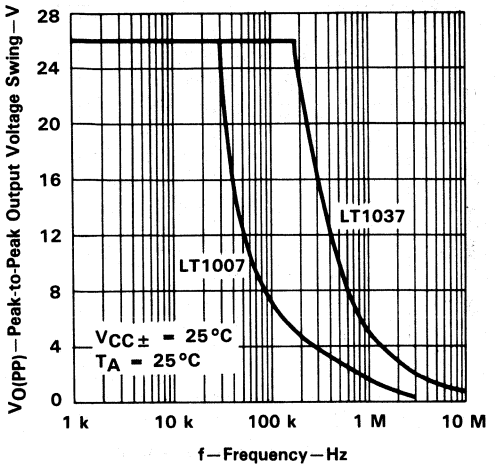


FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

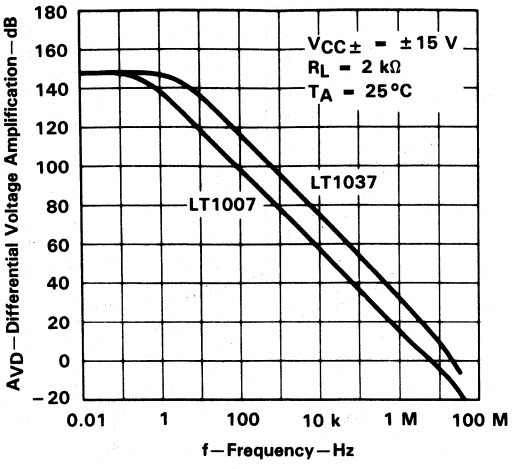


FIGURE 10

LT1007
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

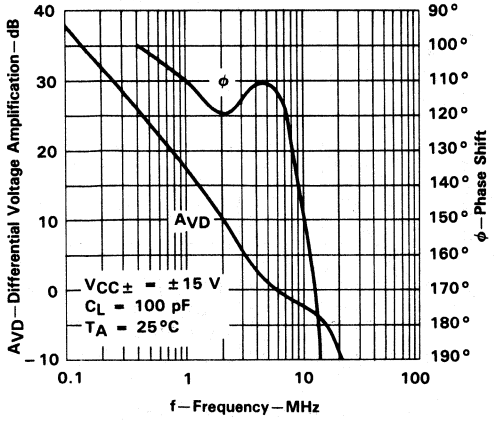


FIGURE 11

LT1037
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

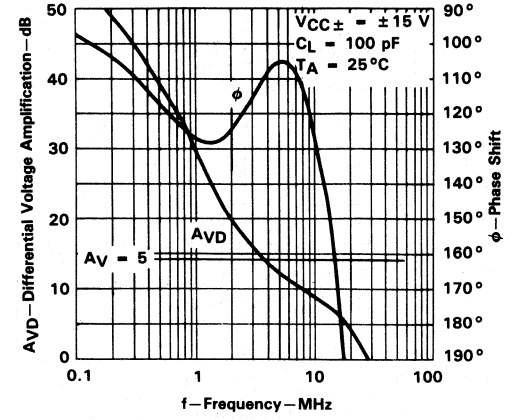


FIGURE 12

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

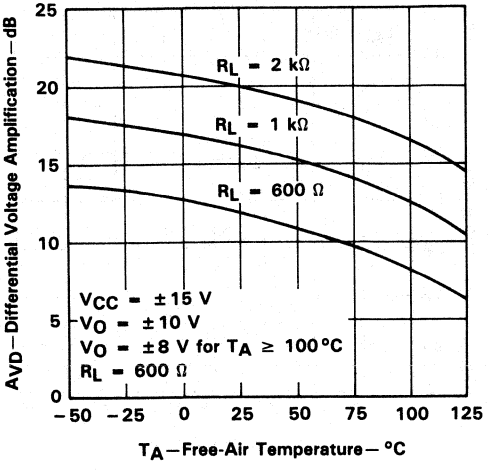

FIGURE 13

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

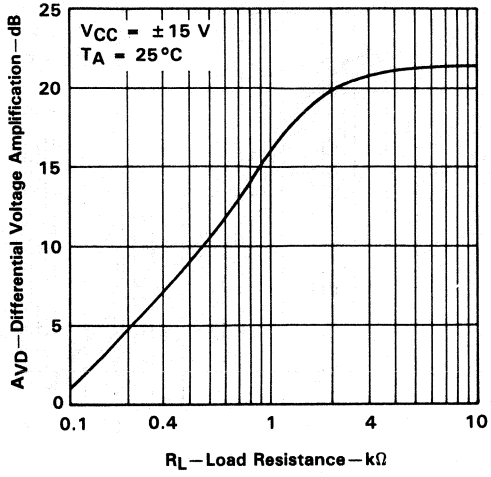

FIGURE 14

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

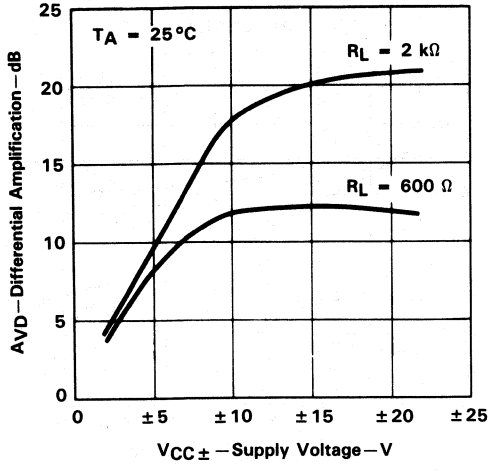

FIGURE 15

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

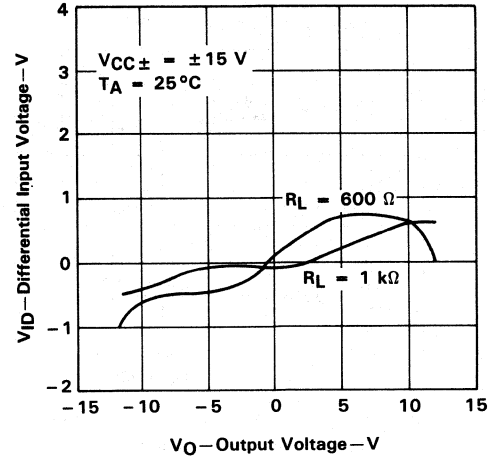

FIGURE 16

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

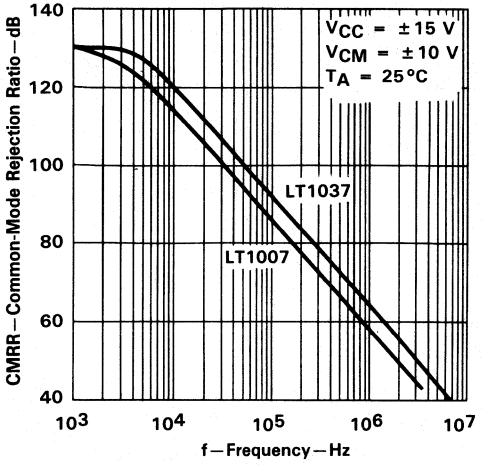

FIGURE 17

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

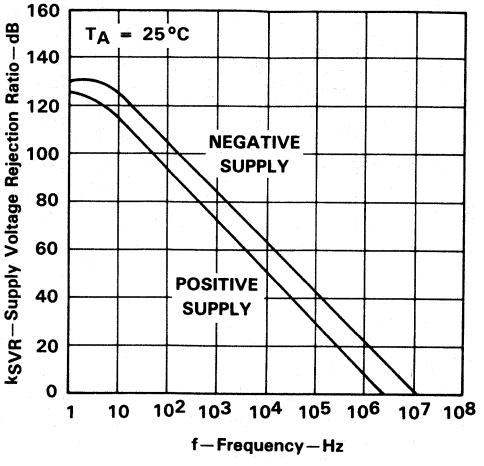

FIGURE 18

LT1007
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

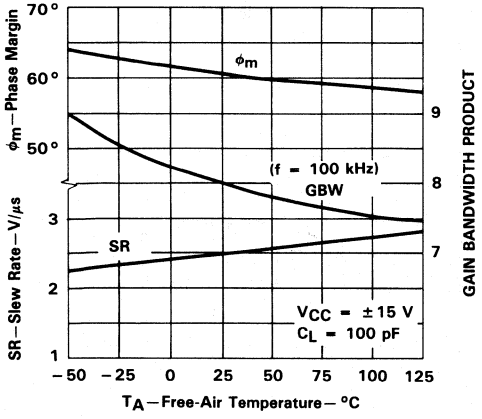

FIGURE 19

LT1037
SLEW RATE, PHASE MARGIN AND
GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

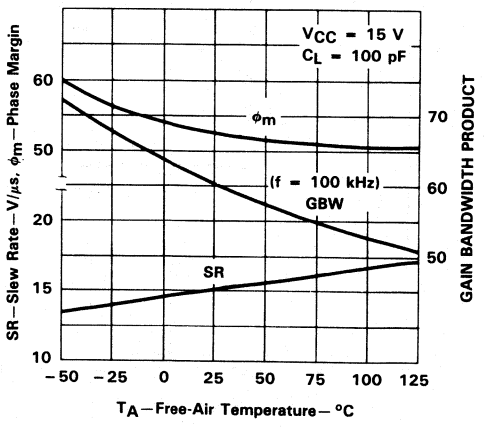

FIGURE 20

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREE-AIR TEMPERATURE

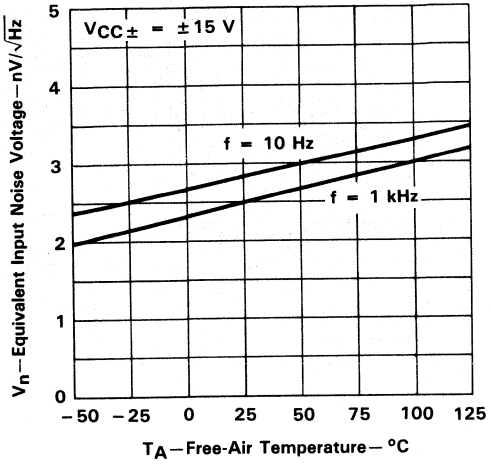


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 100-SECOND TIME PERIOD

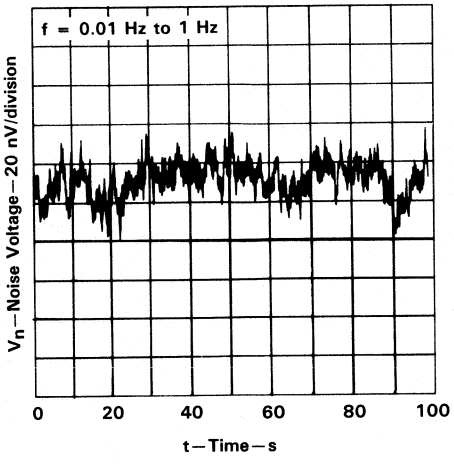


FIGURE 22

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

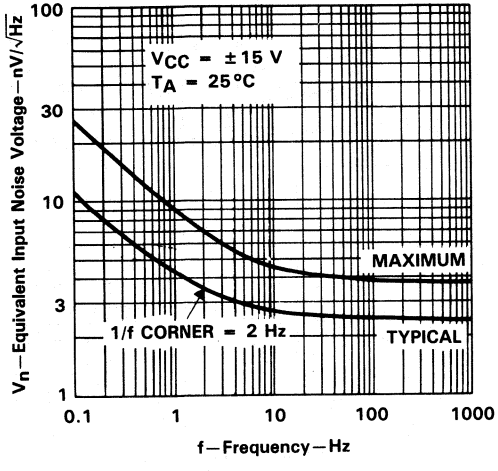


FIGURE 23

BROADBAND NOISE VOLTAGE
0.1 Hz TO INDICATED FREQUENCY

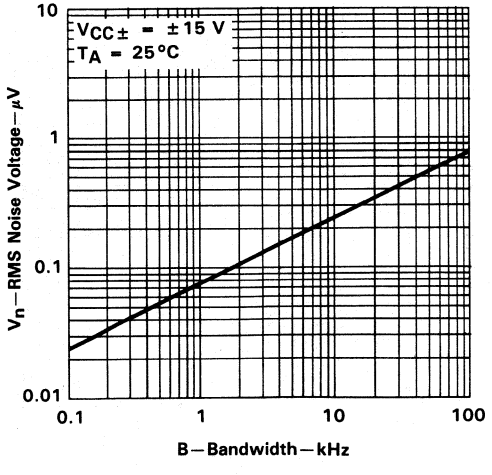


FIGURE 24

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SUPPLY VOLTAGE

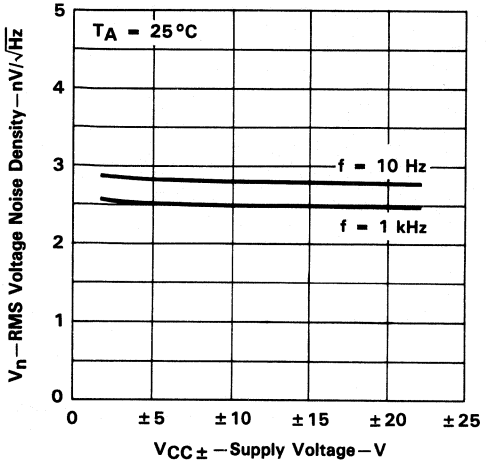


FIGURE 25

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

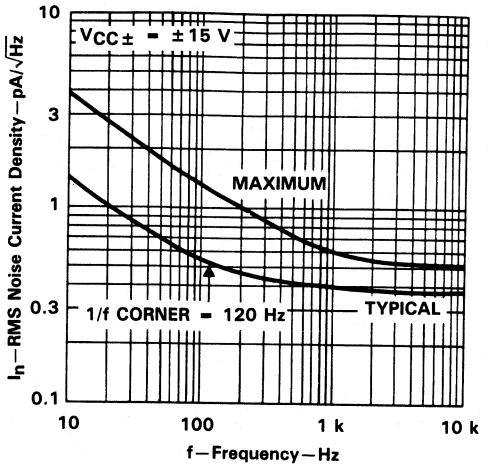


FIGURE 26

TOTAL NOISE VOLTAGE
vs
SOURCE RESISTANCE

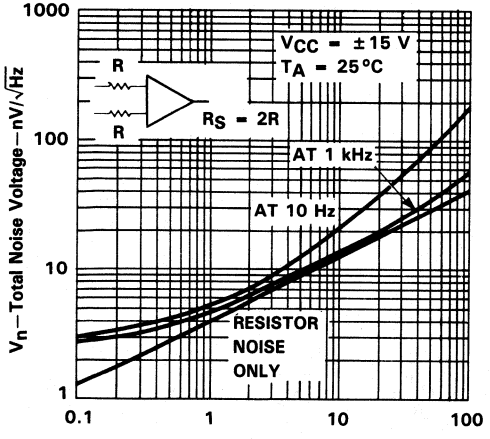


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

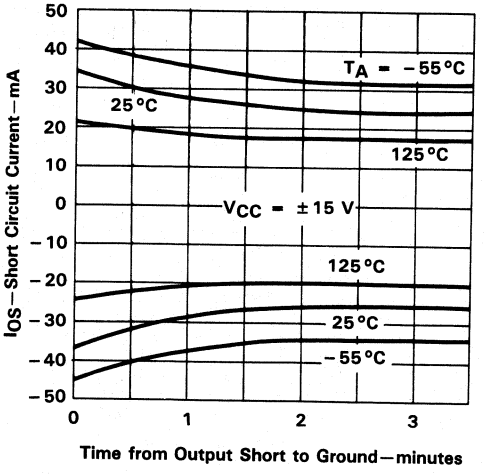


FIGURE 28

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

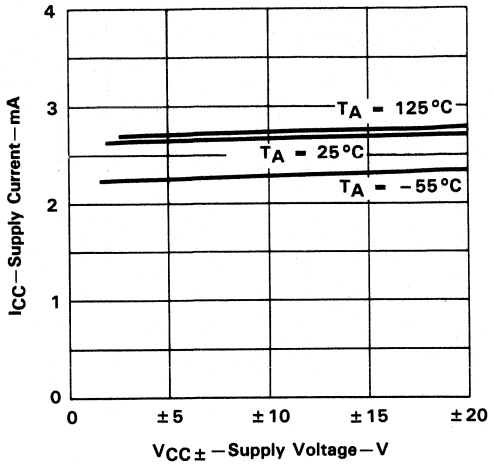


FIGURE 29

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

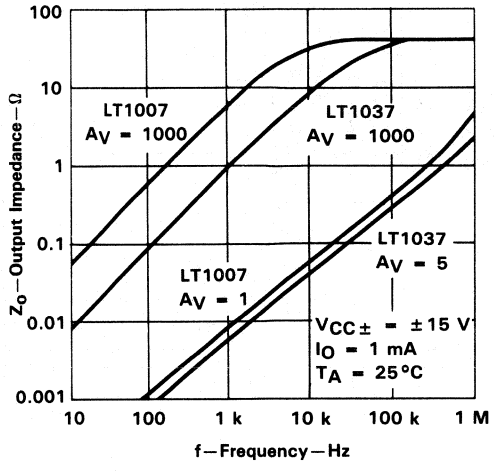


FIGURE 30

LT1037
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

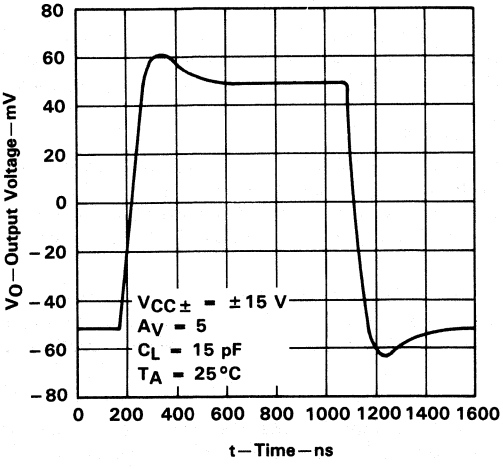


FIGURE 31

LT1037
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

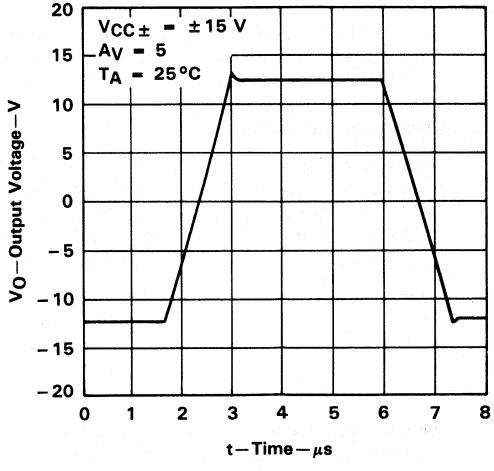


FIGURE 32

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LT1007
VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE

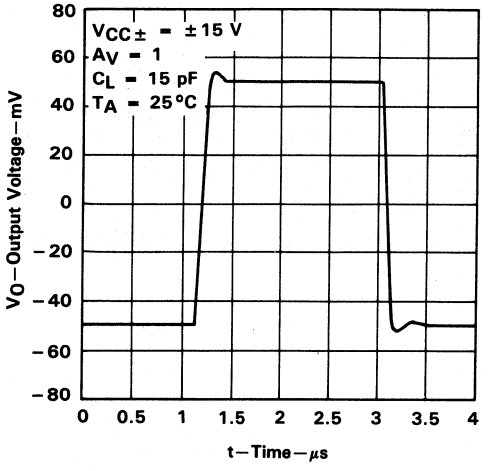


FIGURE 33

LT1007
VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

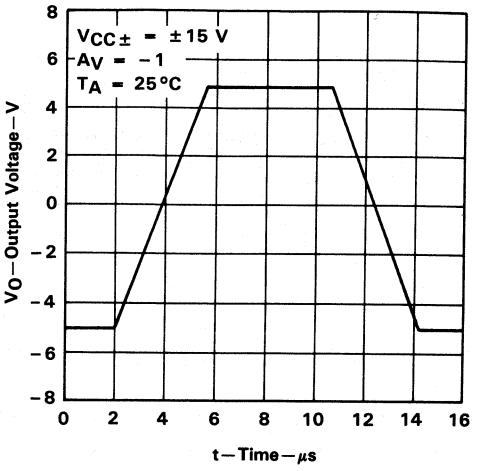


FIGURE 34

TYPICAL APPLICATION DATA

general

The LT1007- and LT1037-series devices may be inserted directly into OP-07, OP-27, OP-37, and 5534 sockets with or without removal of external-compensation or nulling components. In addition, the LT1007 and LT1037 may be fitted to μA741 sockets by removing or modifying external nulling components.

offset voltage adjustment

The input offset voltage and its change with temperature of the LT1007 and LT1037 are permanently trimmed to a low level at wafer testing . However, if further adjustment of V_{IO} is necessary, the use of a 10-kΩ nulling potentiometer, as shown in Figure 35, will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $V_{IO}/300$ μV/°C (e.g., if V_{IO} is adjusted to 300 μV, the change in temperature coefficient will be 1 μV/°C).

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 36 has an approximate null range of ±200 μV.

offset voltage and drift

Unless proper care is exercised, thermocouple effects at the contacts to the input terminals, caused by temperature gradients across dissimilar metals, can exceed the inherent temperature coefficient of the amplifier. Air currents should be minimized, package leads should be short, input leads should be close together, and input leads should be at the same temperature.

TYPICAL APPLICATION DATA

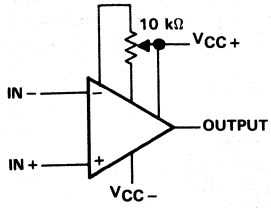


FIGURE 35. STANDARD ADJUSTMENT

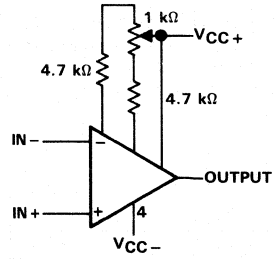


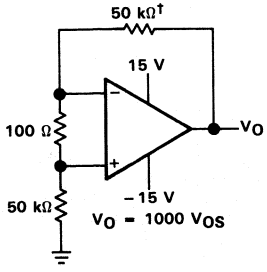
FIGURE 36. IMPROVED SENSITIVITY ADJUSTMENT

The circuit shown in Figure 37 can be used to measure offset voltage. In addition, with the supply voltages increased to ±20 V, it can be used as the burn-in configuration for the LT1007 and LT1037.

When $R_F \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (>1 V), the output waveform will be as shown in Figure 38.

During the fast-feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When R_F is $\geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs.

When R_F is >2 kΩ, a pole will be created with R_F and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_F will eliminate this problem.



†Resistors must have low thermoelectric potential

FIGURE 37. TEST CIRCUIT FOR OFFSET VOLTAGE AND OFFSET VOLTAGE DRIFT WITH TEMPERATURE

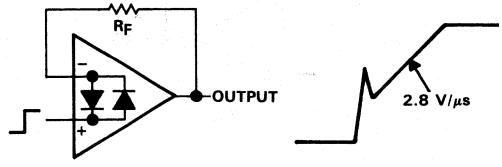
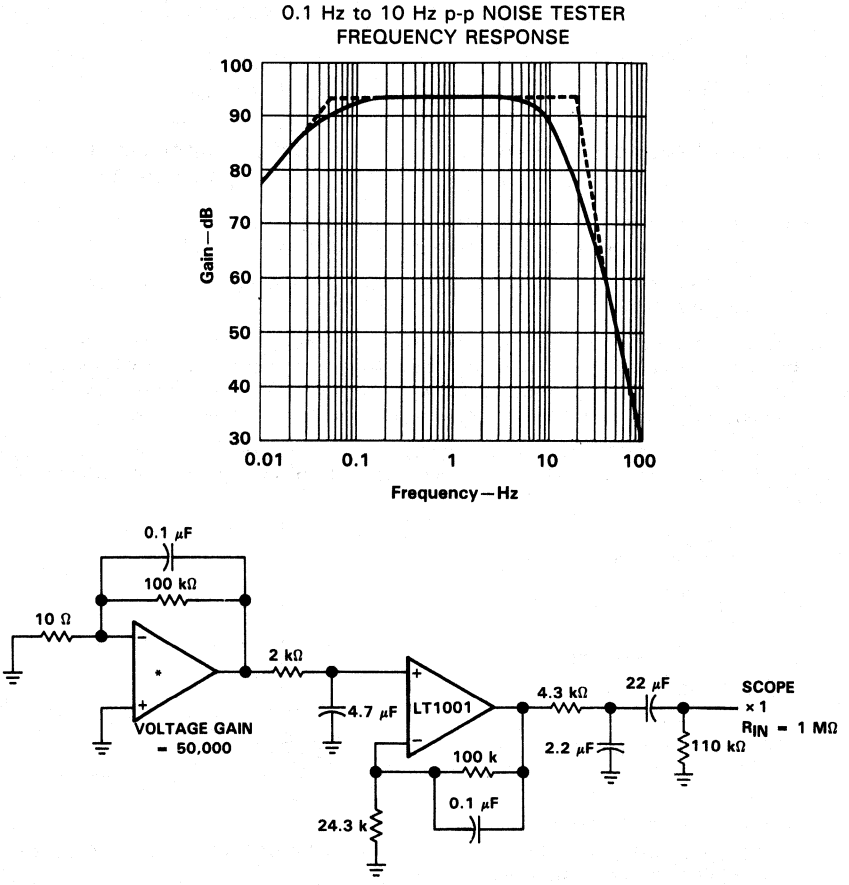


FIGURE 38. PULSE OPERATION

TYPICAL APPLICATION DATA

noise testing

Figure 39 shows a test circuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the LT1007 an LT1037. The frequency response of this noise tester indicates that the 0.1 Hz corner is defined by onl one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequenc band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.



*Device under test
NOTE: All capacitor values are for non-polarized capacitors only.

FIGURE 39. 0.1-Hz TO 10-Hz NOISE TEST CIRCUIT

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

Special test precautions are required to measure the typical 60-nV peak-to-peak noise performance of the LT1007 and LT1037:

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 3 μV, due to the chip temperature increasing 10°C to 20°C from the moment the power supplies are turned on. In the 10-second measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. The device must be well shielded from air currents to eliminate thermoelectric effects. In excess of a few nanovolts, thermoelectric effects would invalidate the measurements.
3. Sudden motion in the vicinity of the device can produce a feedthrough effect that increases observed noise.

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement will correlate well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 40 shows a circuit that measures noise current and presents the formula for calculating noise current.

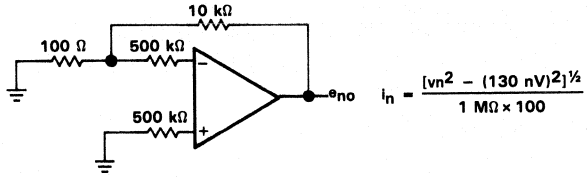


FIGURE 40. NOISE TEST CIRCUIT

The LT1007 and LT1037 achieve low noise, in part, by operating the input stage at 120 μA versus the typical 10 μA for most other operational amplifiers. Voltage noise is directly proportional to the square root of the stage current; therefore, the LT1007 and LT1037 noise current is relatively high. At low frequencies, the low 1/f current-noise corner frequency ($\approx$120 Hz) minimizes noise current to some extent.

In most practical applications, however, noise current will not limit system performance; this is illustrated in Figure 27, where:

$$\text{total noise} = [(\text{noise voltage})^2\ (\text{noise current} \times R_S)^2 + (\text{resistor noise})^2]^{\frac{1}{2}}$$

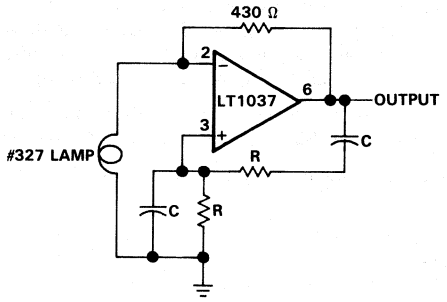
Three regions can be identified as a function of source resistance:

(i)	$R_S \leq 400\ \Omega$	Voltage noise dominates in region (i)
(ii)	$R_S = 400\ \Omega$ to 50 kΩ at 1 kHz	Resistor noise dominates in region (ii)
	$R_S = 400\ \Omega$ to 8 kΩ at 10 Hz	
(iii)	$R_S > 50$ kΩ at 1 kHz	Current noise dominates in region (iii)
	$R_S > 8$ kΩ at 10 Hz	

The LT1007 and LT1037 should not be used in region (iii) where total system noise is at least six times higher than the noise voltage of the operational amplifier (i.e., the low-voltage noise specification is completely wasted).

TYPICAL APPLICATIONS

The sine wave generator application shown below, utilizes the low-noise and low-distortion characteristics of the LT1037.



$f = \frac{1}{2\pi RC}$
R = 1591.5Ω ±0.1%
C = 0.1 μF ±0.1%

TOTAL HARMONIC DISTORTION ≤ 0.0025%
NOISE ≤ 0.001%
AMPLITUDE = ±8 V
OUTPUT FREQUENCY = 1.000 kHz FOR VALUES GIVEN ± 0.4%

FIGURE 41. ULTRA-PURE 1-kHz SINE-WAVE GENERATOR

EQUIVALENT INPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

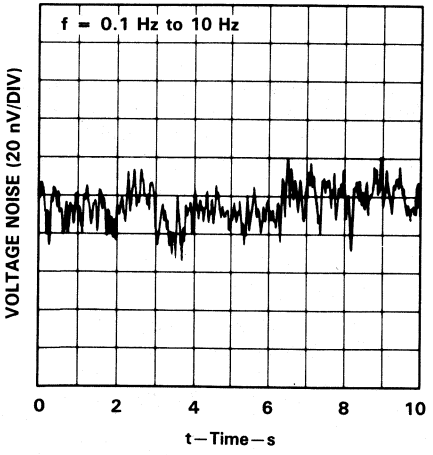
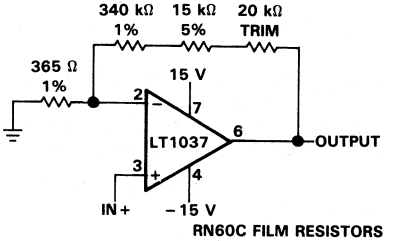


FIGURE 42



RN60C FILM RESISTORS

The high gain and wide bandwidth of the LT1037 and (LT1007) is useful in low-frequency high-closed-loop-gain amplifier applications. A typical precision Op Amp may have an open loop gain of one million with 500 kHz bandwidth. As the gain error plot shows, this device is capable of 0.1% amplifying accuracy up to 0.3 Hz only. Even instrumentation range signals can vary at a faster rate. The LT1037's "gain precision—bandwidth product" is 200 times higher, as shown.

FIGURE 43. GAIN 1000 AMPLIFIER WITH 0.01% ACCURACY, DC to 5 Hz

TYPICAL APPLICATIONS

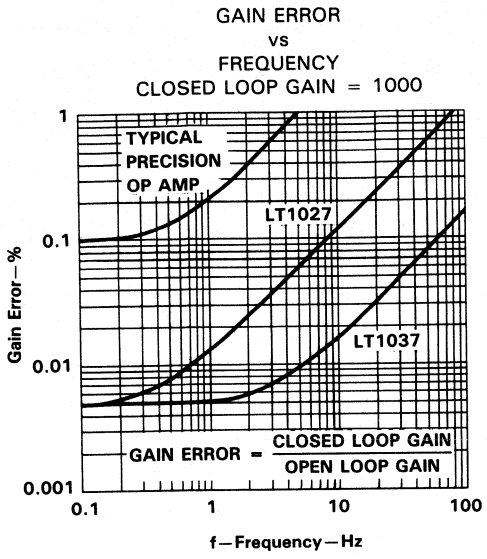
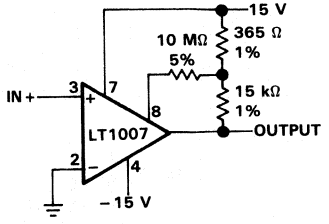


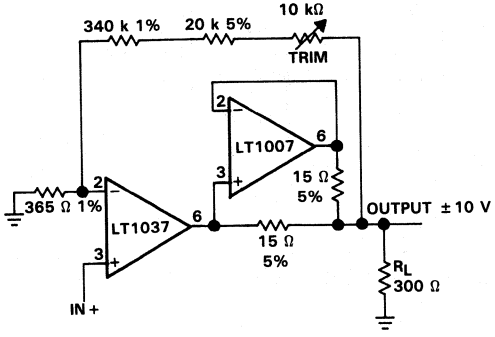
FIGURE 44



Positive feedback to one of the nulling terminals creates approximately 5 μV of hysteresis. Output can sink 16 mA.

Input offset voltage is typically changed less than 5 μV due to the feedback.

FIGURE 45. MICROVOLT COMPARATOR WITH HYSTERESIS



The addition of the LT1007 doubles the amplifier's output drive to ±33 mA. Gain accuracy is 0.02%, slightly degraded compared to above because of self heating of the LT1037 under load.

FIGURE 46. PRECISION AMPLIFIER DRIVES 300-Ω LOAD TO ±10 V

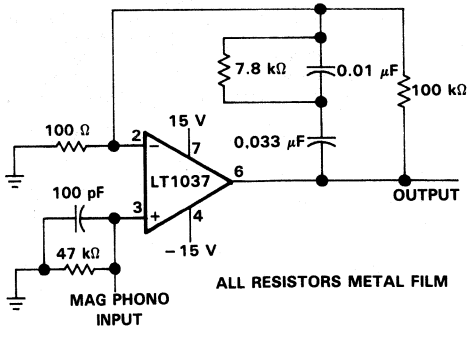


FIGURE 47. PHONO PREAMPLIFIER

TYPICAL APPLICATIONS

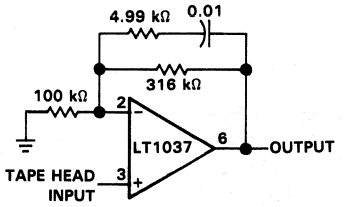


FIGURE 48. TAPE HEAD AMPLIFIER

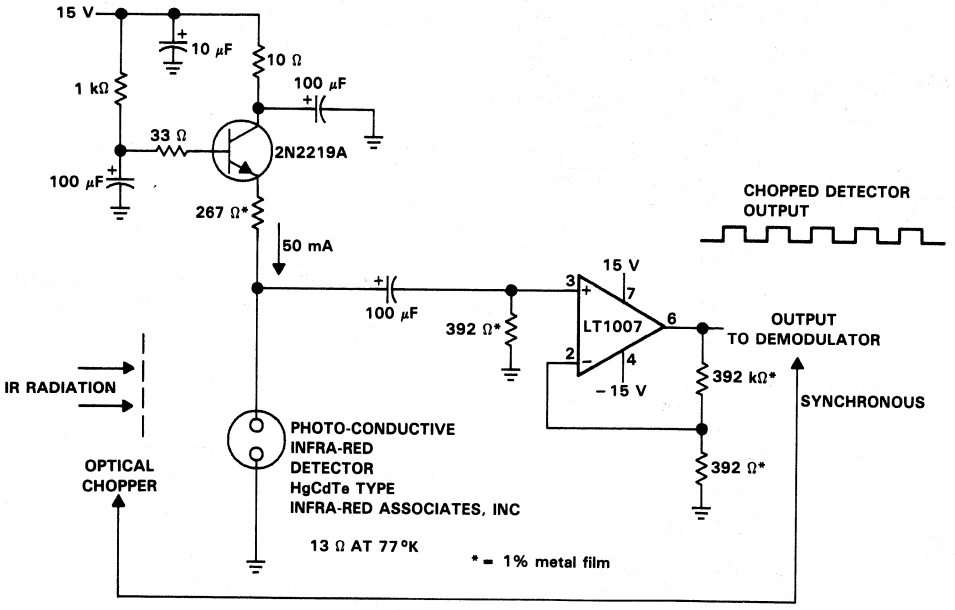
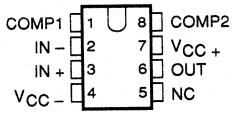


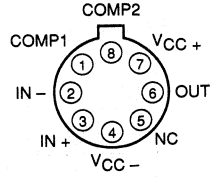
FIGURE 49. INFRA-RED DETECTOR PREAMPLIFIER

- **Input Bias Current . . . ± 30 pA Typ, ± 100 pA Max at 25°C**
- **Input Offset Voltage . . . 30 μV Typ, 120 μV Max at 25°C**
- **Offset Voltage Temperature Coefficient . . . 1.5 μV/°C Max**
- **Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 0.5 μV**
- **Low Supply Current . . . 380 μA Typ, 600 μA Max at 25°C**
- **Supply Voltage Rejection Ratio . . . 114 dB Min at 25°C**
- **Common-Mode Rejection Ratio . . . 114 dB Min at 25°C**
- **High Voltage Amplification with 5-mA Load Current**
- **Applications:**
  - **Precision Instrumentation**
  - **Charge Integrators**
  - **Wide-Dynamic-Range Logarithmic Amplifiers**
  - **Light Meters**
  - **Low-Frequency Active Filters**
  - **Standard Cell Buffers**
  - **Thermocouple Amplifiers**

JG OR P PACKAGE
(TOP VIEW)

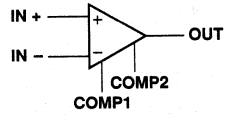


L PACKAGE
(TOP VIEW)



NC – No internal connection
Pin 4 (L Package) is in electrical contact with the case.

symbol



description

The LT1008 is a precision operational amplifier that can be used in practically all precision applications. The LT1008 offers picoampere bias currents (maintained over the full temperature range), microvolt offset voltage, low offset voltage temperature coefficient and long-term drift, low voltage and current noise, and low power dissipation. Additionally, the LT1008's precision specifications include high common-mode and supply voltage rejection ratios. The LT1008 can deliver a 5-mA load current with high voltage amplification.

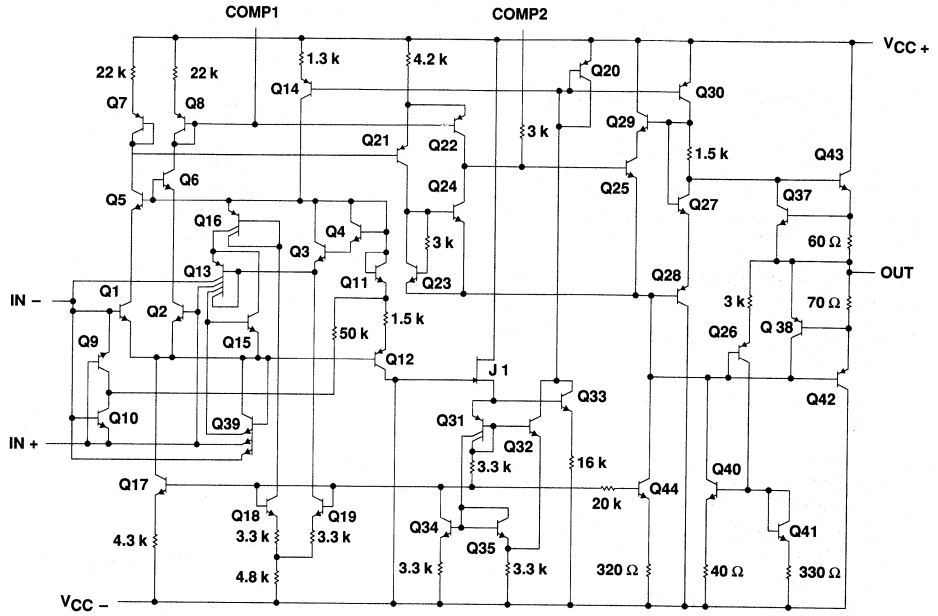
The LT1008 is externally compensated with a single capacitor to add flexibility in shaping the frequency response of the amplifier. The LT1008 is a pin-for-pin replacement for the LM108 series.

The LT1008M is characterized for operation over the full military temperature range of –55°C to 125°C. The LT1008C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	LT1008CJG	LT1008CL	LT1008CP
– 55°C to 125°C	LT1008MJG	LT1008ML	LT1008MP

schematic



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 20 V
Supply voltage, V_{CC-} . . . . . – 20 V
Input voltage range, V_I . . . . . ± 20 V
Differential input current (see Note 2) . . . . . ± 10 mA
Duration of output short-circuit at (or below) 25°C (see Note 3) . . . . . unlimited
Operating free-air temperature, T_A: LT1008M . . . . . – 55°C to 125°C
LT1008C . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages greater than 1 V will cause excessive current to flow through the input protection diodes unless current-limiting resistors are used.
3. The output may be shorted to either supply.

recommended operating conditions

		LT1008M			LT1008C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}				± 20			± 20	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 15 V			± 13.5	– 15		± 13.5	V
Operating free-air temperature, T_A		– 55		125	0		70	°C

electrical characteristics, $V_{CC\pm}$ = ±15V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1008M			LT1008C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		30	120		30	120	μV
			Full range			250			180	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		40	180		40	180	
			Full range			320			250	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		40	180		40	180	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			320			250	
α_{VIO}	Average temperature coefficient of input offset voltage		Full range		0.2	1.5		0.2	1.5	μV/°C
	Long-term drift of input offset voltage		25°C		0.3			0.3		μV/mo
I_{IO}	Input offset current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		30	100		30	100	pA
			Full range			250			180	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		40	150		40	150	
			Full range			350			250	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		40	150		40	150	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			350			250	
α_{IIO}	Average temperature coefficient of input offset current		Full range		0.4	2.5		0.4	2.5	pA/°C
I_{IB}	Input bias current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		±30	±100		±30	±100	pA
			Full range			±600			±180	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		±40	±150		±40	±150	
			Full range			±800			±250	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		±40	±150		±40	±150	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			±800			±250	
α_{IIB}	Average temperature coefficient of input bias current		Full range		0.6	6		0.4	2.5	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13.5	±14		±13.5	±14		V
			Full range	±13.5			±13.5			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±13	±14		±13	±14		V
			Full range	±13			±13			
A_{VD}	Large-signal differential voltage amplification	V_O = ±12 V, R_L ≥ 10 kΩ	25°C	200	2000		200	2000		V/mV
			Full range	100			150			
		V_O = ±10 V, R_L ≥ 2 kΩ	25°C	120	600		120	600		
CMRR	Common-mode rejection ratio	V_{IC} = ±13.5 V	25°C	114	132		114	132		dB
			Full range	108			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±2 V to ±20 V	25°C	114	132		114	132		dB
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range	108			110			
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		380	600		380	600	μA
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		380	600		380	600	
		$V_{CC\pm}$ = ±15 V, V_{IC} = 0	Full range			800			800	

†Full range is −55°C to 125°C for the LT1008M and 0°C to 70°C for the LT1008C.

operating characteristics, $V_{CC\pm}$ = ± 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	C_f = 30 pF, See Figure 29(a)	0.1	0.2		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz		0.5		μV
V_n	Equivalent input noise voltage	f = 10 Hz		17	30	nV/√Hz
		f = 1 kHz		14	22	
I_n	Equivalent input noise current	f = 10 Hz		20		fA/√Hz

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
		vs Source resistance	5
ΔV_{IO}	Change in input offset voltage	vs Time – minutes	2
		vs Time – months	3
α_{VIO}	Temperature coefficient of input offset voltage	vs Source resistance	6
I_{IB}	Input bias current	vs Common-mode input voltage	7
		vs Temperature	8
A_{VD}	Differential voltage amplification	vs Load resistance	9
		vs Frequency	10, 11, 12
CMRR	Common-mode rejection ratio	vs Frequency	13
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	14
I_{OS}	Short-circuit output current	vs Time	15
I_{CC}	Supply current	vs Supply voltage	4
SR	Slew rate	vs Compensation capacitance	16
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Time	17
V_n, I_n	Equivalent input noise voltage and equivalent input noise current	vs Frequency	18
	Total equivalent input noise voltage	vs Source resistance	19
	Phase shift	vs Frequency	11, 12
	Pulse response	Small-signal	20, 21, 22
		Large-signal	23, 24

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TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS
vs
FREE-AIR TEMPERATURE

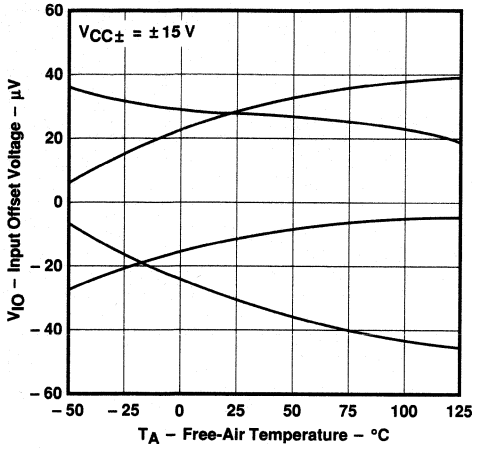


FIGURE 1

WARM-UP CHANGE IN
INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

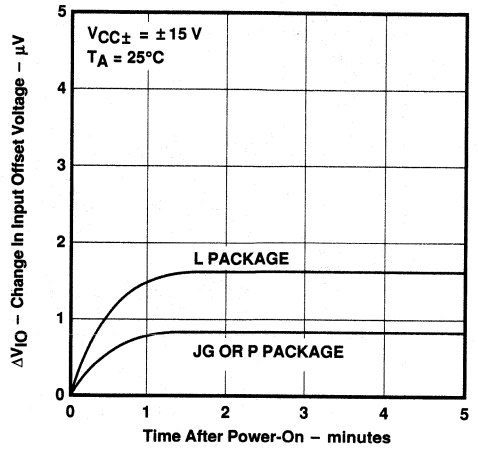


FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

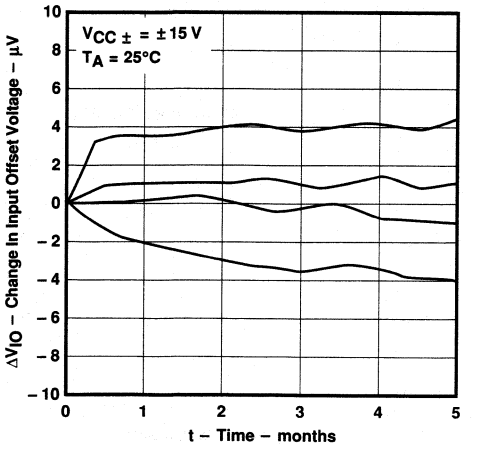


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

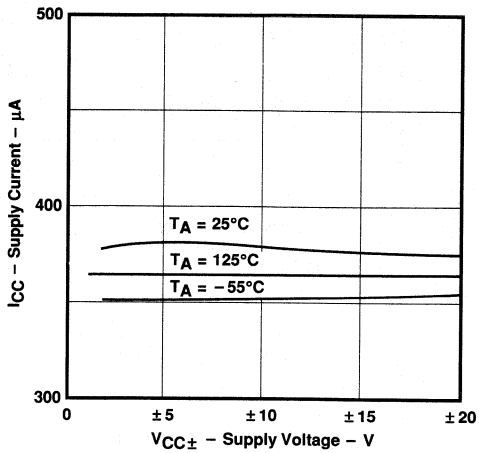


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

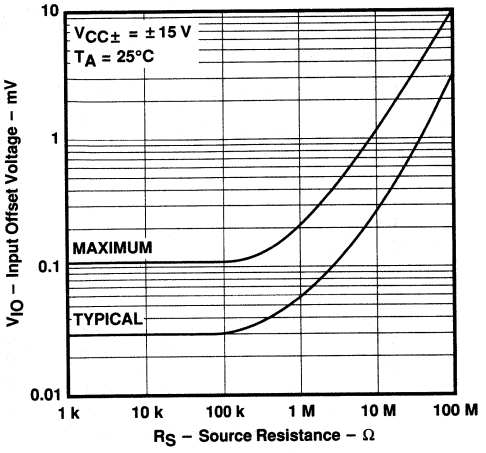


FIGURE 5

AVERAGE TEMPERATURE COEFFICIENT
OF INPUT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

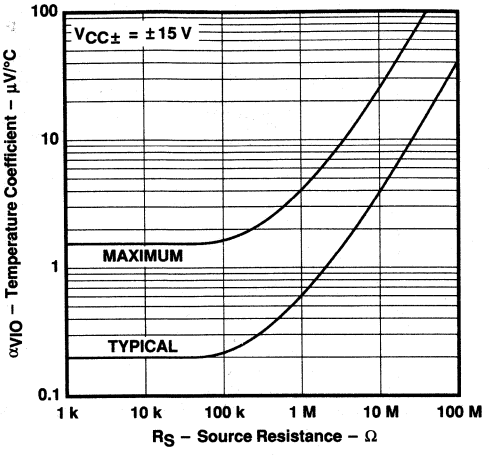


FIGURE 6

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

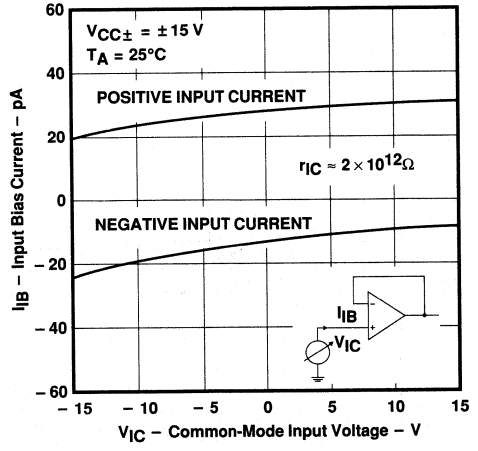


FIGURE 7

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

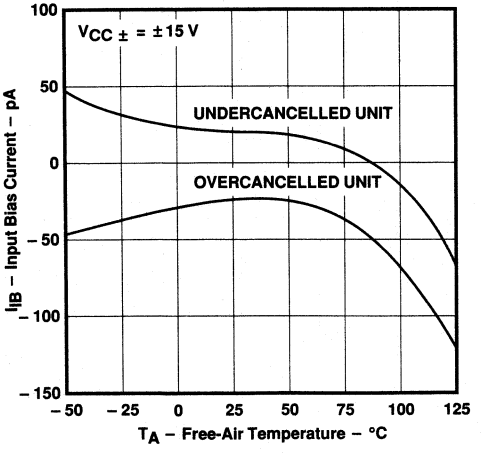


FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

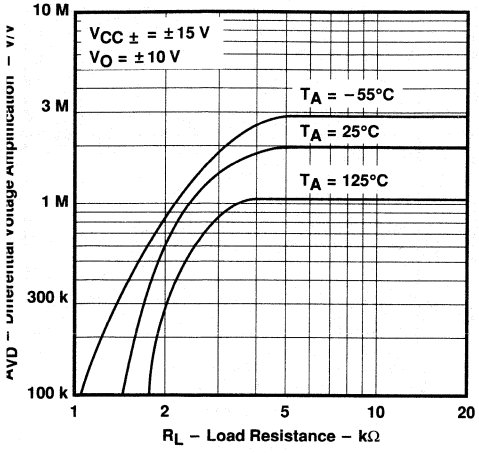


FIGURE 9

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

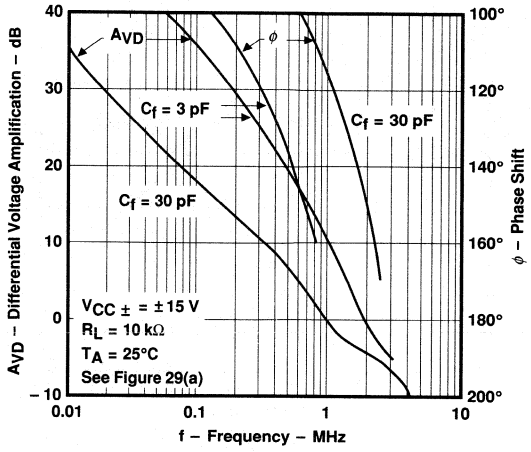


FIGURE 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

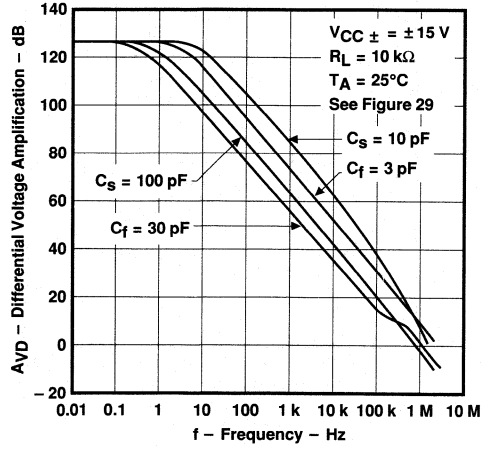


FIGURE 11

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION and PHASE SHIFT
vs
FREQUENCY

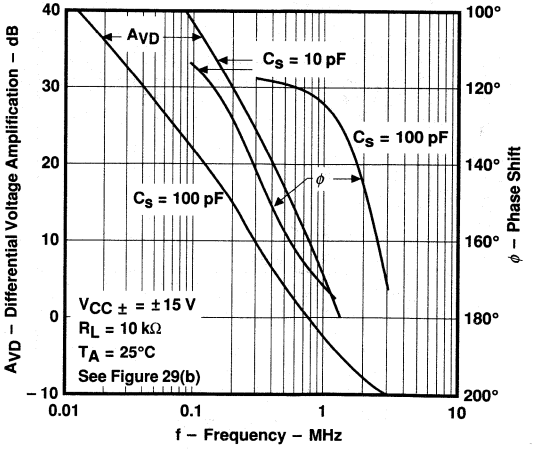


FIGURE 12

Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

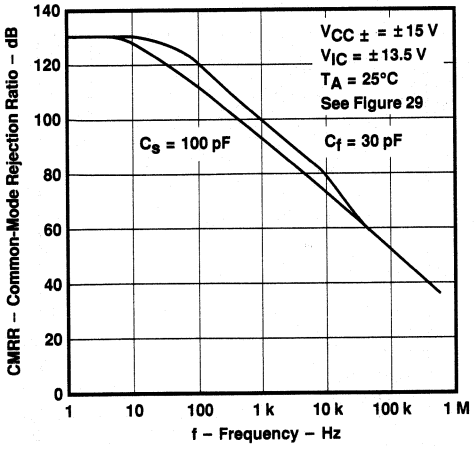


FIGURE 13

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

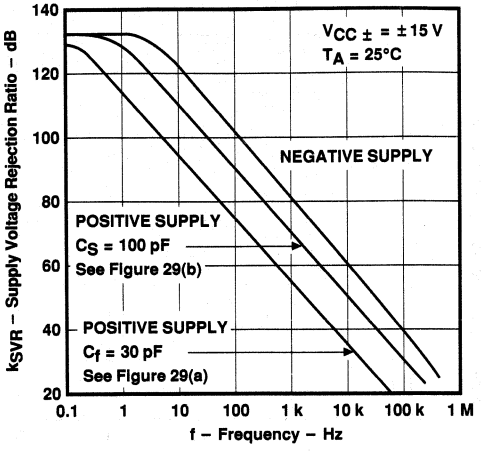


FIGURE 14

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

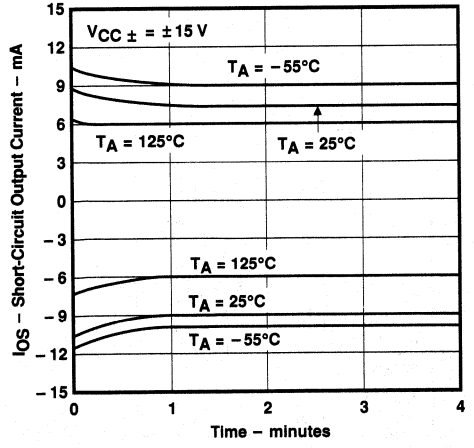


FIGURE 15

SLEW RATE
vs
COMPENSATION CAPACITANCE

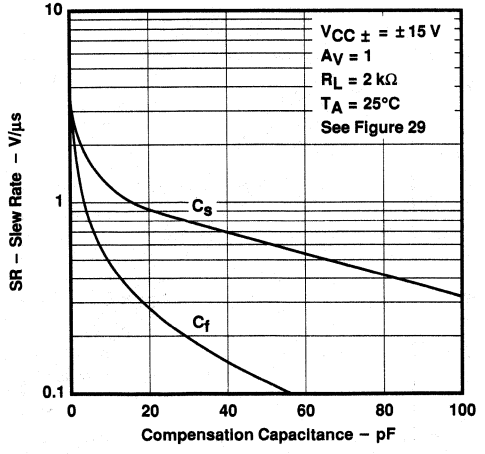


FIGURE 16

†Data for temperatures below 0°C and above 70°C are applicable to the LT1008M only.

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
OVER A 10-SECOND PERIOD

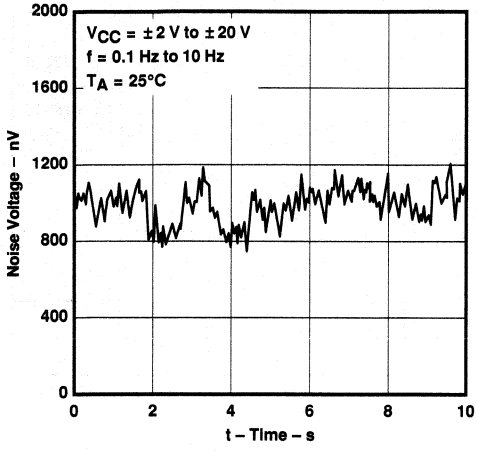


FIGURE 17

EQUIVALENT INPUT NOISE VOLTAGE
and EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

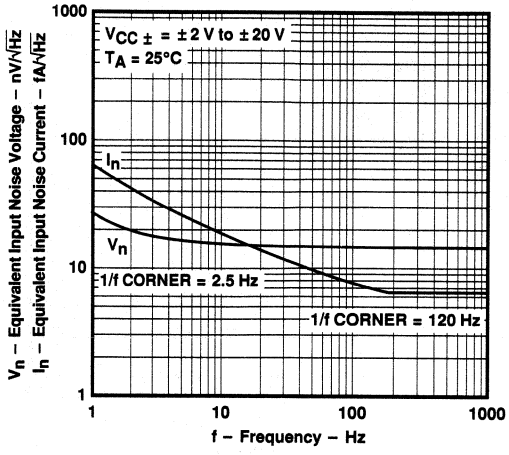


FIGURE 18

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

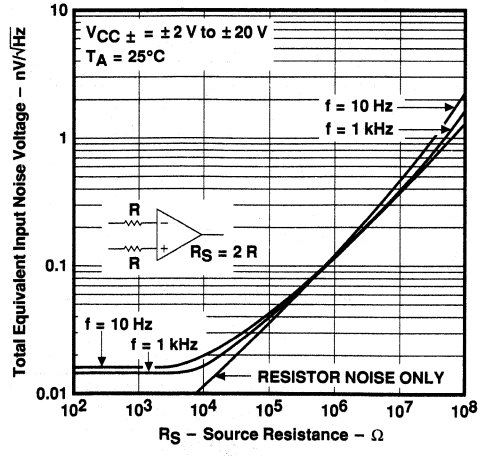


FIGURE 19

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

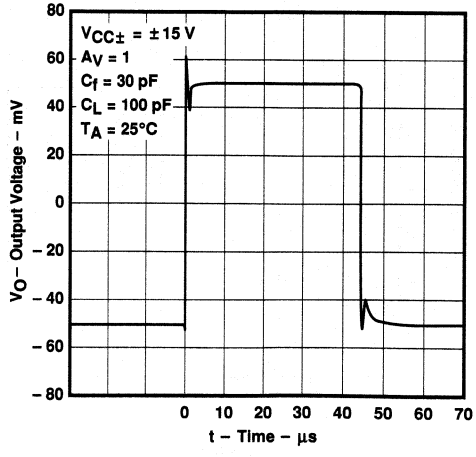


FIGURE 20

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

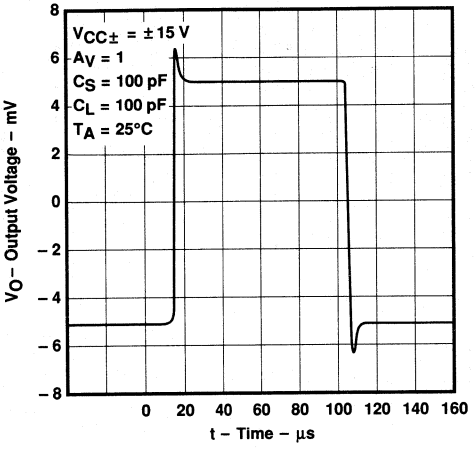


FIGURE 21

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

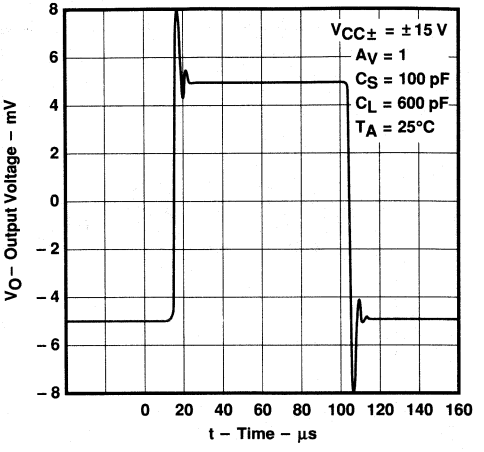


FIGURE 22

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

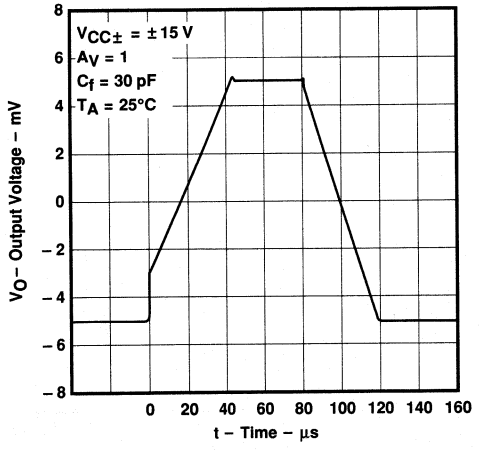


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

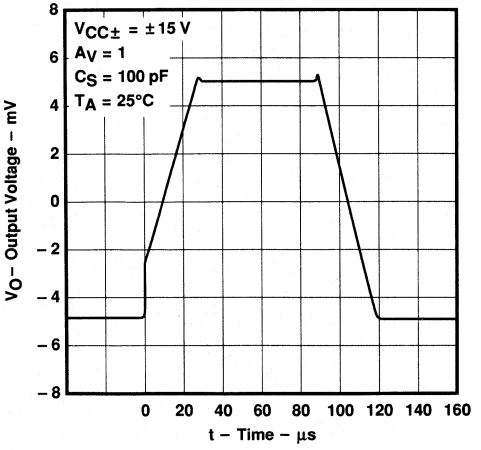


FIGURE 24

TYPICAL APPLICATION DATA

chieving picoampere, microvolt performance

Proper care should be exercised to realize the picoampere, microvolt accuracy of the LT1008. Because leakage currents in external circuitry can significantly degrade performance, high-quality insulation should be used (e. g.,Teflon, Kel-F). All insulating surfaces should be cleaned to remove fluxes and other residues. Surface coating may be necessary to provide a moisture barrier in high-humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs (see Figure 25). In inverting configurations, the guard ring should be tied to ground; in noninverting configurations, the guard ring should be tied to the inverting input (pin 2). Both sides of the printed circuit board should be guarded. Bulk leakage reduction depends on the guard ring width. Nanoampere-level leakage into the compensation terminals can affect input offset voltage and its temperature coefficient (see Figure 26).

Microvolt-level error voltages can also be generated in the external circuitry. Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent temperature coefficient of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature. The LT1008 is specified over a wide range of supply voltages from ±2 V to ±18 V. Operation with lower supplies (down to ±1 V) is possible with two Ni-Cad batteries.

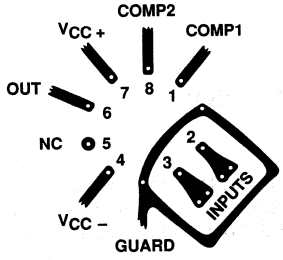
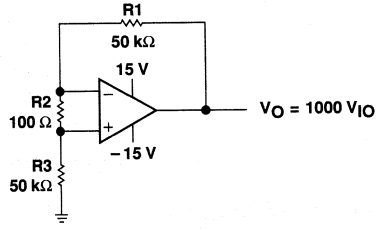


FIGURE 25. GUARD RING



NOTES: A. Resistors must have low thermoelectric potential.
B. This circuit is also used as the burn-in configuration for the LT1008, with supply voltages increased to ± 20 V, R1 = R3 = 20 kΩ, R2 = 200 Ω, and A_V = 100.

FIGURE 26. TEST CIRCUIT FOR V_{IO} AND α_{VIO}

noise testing

The peak-to-peak equivalent input noise voltage of the LT1008 is measured in the test circuit shown in Figure 27. The frequency response of this noise tester indicates that the 0.1-Hz to 10-Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.

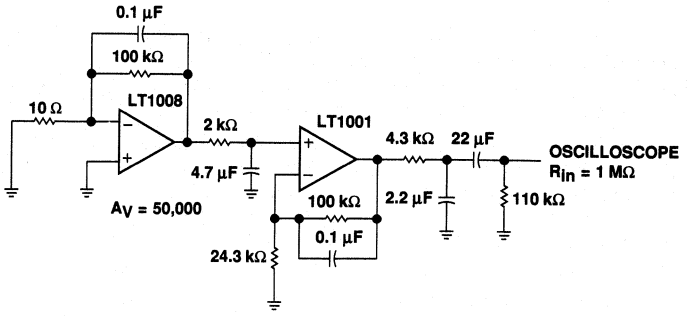
An input noise voltage test is recommended when measuring noise in a large number of units. A 10-Hz input noise voltage measurement correlates well with a 0.1-Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.

Current noise is measured by the current shown in Figure 28 and calculated by the following formula in which the noise of the source resistors is subtracted:

$$I_n = \frac{[V_{no}^2 - (820\ nV)^2]^{1/2}}{40\ M\Omega \times 100}$$

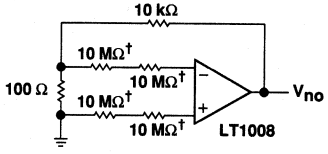
TYPICAL APPLICATION DATA

noise testing (continued)



NOTE A : All capacitor values are for nonpolarized capacitors only.

FIGURE 27. 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE TEST CIRCUIT

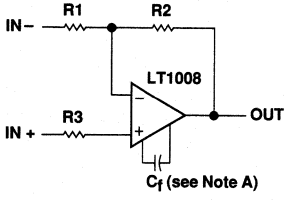


† Metal film.

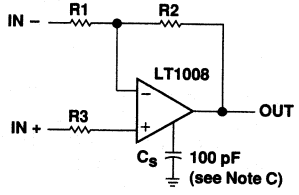
FIGURE 28. NOISE CURRENT TEST CIRCUIT

frequency compensation

The LT1008 is externally frequency compensated with a single capacitor. The two compensation circuits shown in Figure 29 are identical to the frequency compensation circuits for the LM108A series. Therefore, the LT1008 operational amplifiers can be inserted directly into LM108A or LM308A sockets, with similar ac and upgraded dc performance.



(a) STANDARD COMPENSATION



(b) ALTERNATE COMPENSATION (see Note B)

NOTES: A. $C_f \geq (R1 \times C_o) / (R1 + R2)$, C_o = 30 pF. Bandwidth and slew rate are proportional to $1/C_f$.
B. This circuit improves the supply voltage rejection ratio by a factor of 5.
C. Bandwidth and slew rate are proportional to $1/C_S$.
D. For (R2/R1) > 200, no external frequency compensation is necessary.

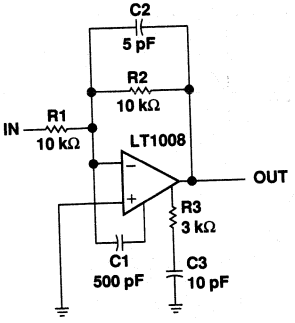
FIGURE 29. FREQUENCY COMPENSATION CIRCUITS (see Note D)

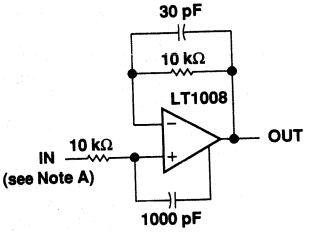
TYPICAL APPLICATION DATA

equency compensation (continued)

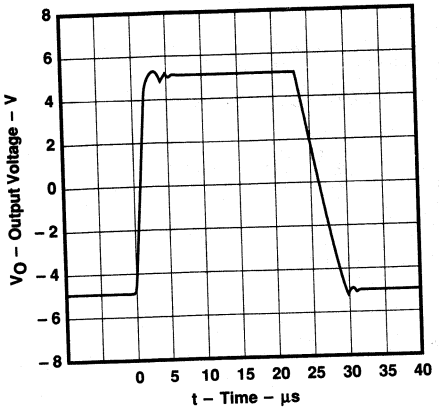
External frequency compensation provides additional flexibility in shaping the frequency response of the amplifier. For example, for a voltage gain of 10 and C_f = 3 pF, a gain-bandwidth product of 5 MHz and slew rate of 1.2 V/μs can be realized. For closed-loop gains greater than 200, no external compensation is necessary, and the slew rate increases to 4 V/μs. The LT1008 can also be overcompensated (e.g., C_f > 30 pF or C_S > 100 pF) to improve capacitive-load-handling capability or to narrow noise bandwidth. In applications in which the feedback loop around the amplifier has gain, overcompensation can stabilize the circuit with a single capacitor.

The availability of the compensation terminals permits the use of feed-forward frequency compensation to enhance slew rate in low closed-loop-gain configurations (see Figure 30). The inverter slew rate is increased to 1.4 V/μs. The voltage-follower feed-forward scheme bypasses the amplifier's gain stages and slews at nearly 10 V/μs.

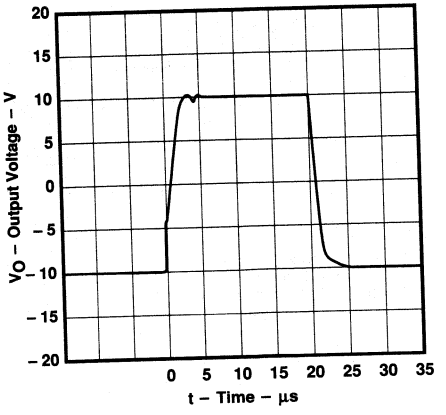




NOTE A: $R_S \leq 15$ kΩ for stability.



(a) INVERTER FEED-FORWARD



(b) VOLTAGE-FOLLOWER FEED-FORWARD

FIGURE 30. FREQUENCY COMPENSATION CIRCUITS and VOLTAGE-FOLLOWER PULSE RESPONSES

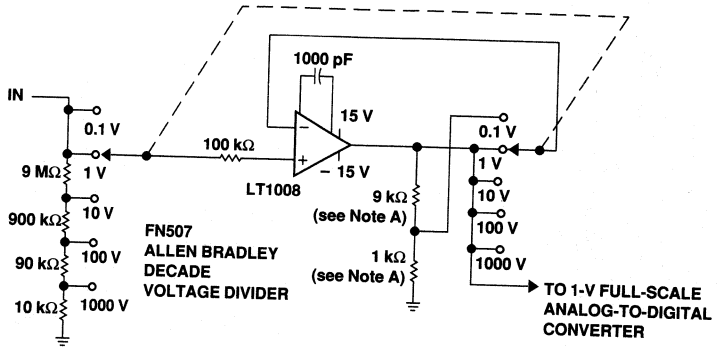
TYPICAL APPLICATION DATA

other considerations

The inputs of the LT1008 are protected by back-to-back diodes. Current-limiting resistors are not usec because the leakage of these resistors would prevent the realization of picoampere-level bias currents at elevated temperatures. In the voltage-follower configuration, when the input is driven by a fast, large-signal pulse (> 1 V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short-circuit protection, flows through the diodes.

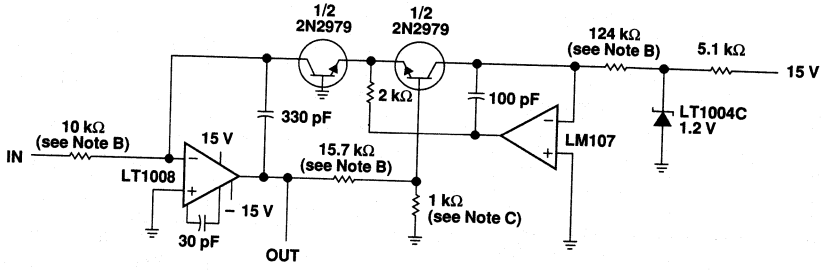
The use of a feedback resistor, as shown in the voltage-follower feed-forward diagram, is recommended because this resistor keeps the current below the short-circuit limit, resulting in faster recovery and settling of the output.

typical applications



NOTES: A. Ratio match ± 0.01 %.
B. This application requires low bias current, low offset voltage and offset voltage temperature coefficient, low noise, and low long-term offset voltage drift.

FIGURE 31. INPUT AMPLIFIER FOR 4 1/2-DIGIT VOLTMETER

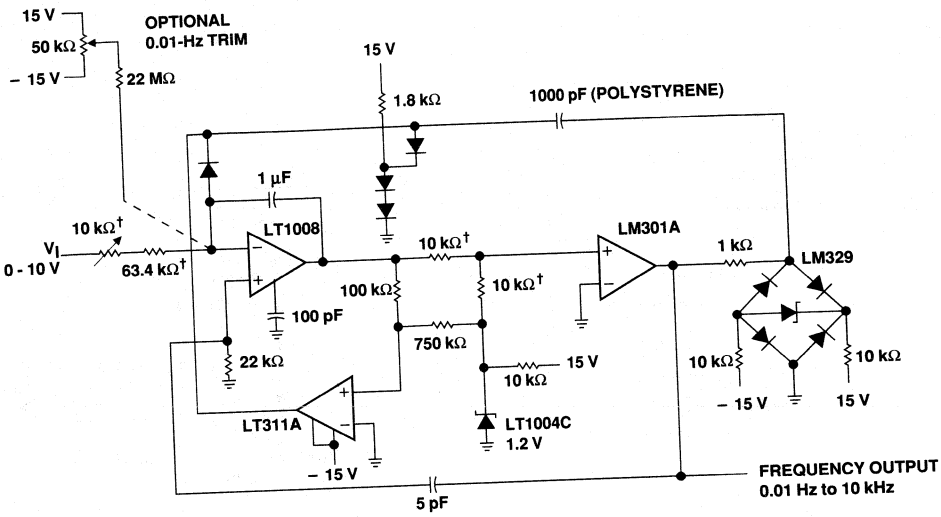


NOTES: A. The low bias current and offset voltage of the LT1008 allow 4 1/2 decades of voltage input logging.
B. 1% film resistor.
C. Tel. Labs, Type Q81.

FIGURE 32. LOGARITHMIC AMPLIFIER

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA



†1% metal film resistor

NOTES: A. The LT1008 integrator extends the low frequency range. The total dynamic range is 0.01 Hz to 10 kHz (or 120 dB) with 0.01% linearity.
B. All diodes 1N4148.

FIGURE 33. EXTENDED RANGE CHARGE PUMP VOLTAGE-TO-FREQUENCY CONVERTER

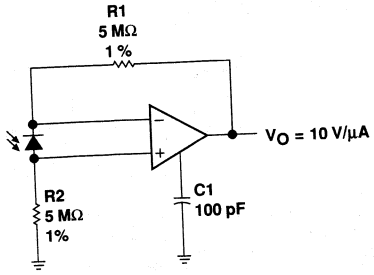
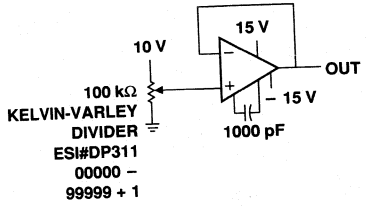


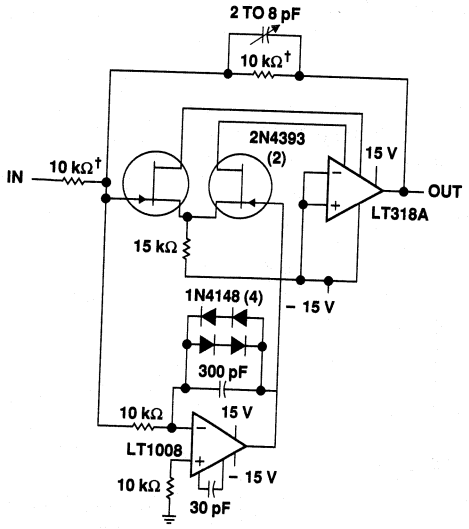
FIGURE 34. AMPLIFIER FOR PHOTODIODE SENSOR



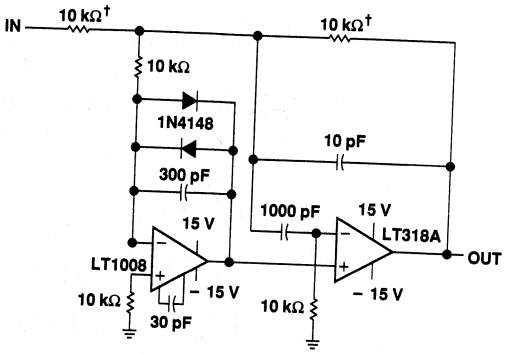
NOTE A : Approximate error due to noise, bias current, common-mode rejection, and voltage gain of the amplifier is 1/5 of a least significant bit.

FIGURE 35. FIVE-DECADE KELVIN-VARLEY DIVIDER BUFFERED BY THE LT1008

TYPICAL APPLICATION DATA



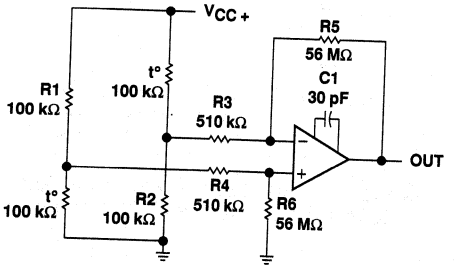
(a) SR = 100 V/μs
I_{IB} = 30 pA
V_{IO} = 30 μV
Settling = 5 μs to 0.01%/10-V step



(b) SR = 50 V/μs
I_{IB} = 30 pA
V_{IO} = 30 μV
α_{VIO} = 0.3 μV/°C
BW = 2 MHz
Settling = 12 μs to 0.01%/10-V step

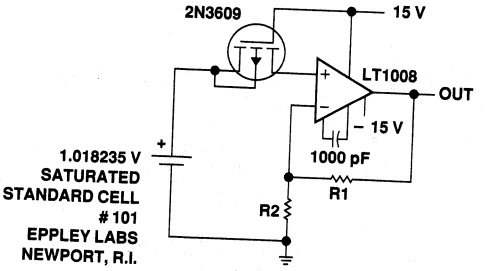
†1% metal film resistor.

FIGURE 36. FAST PRECISION INVERTERS



NOTE A : A_{VD} = 100.

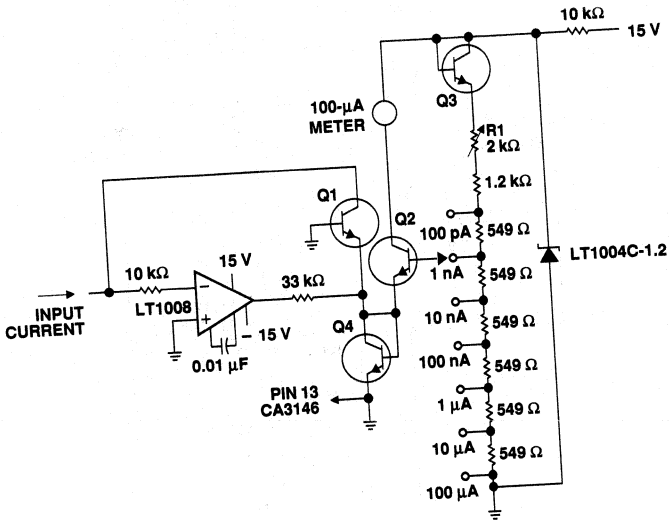
FIGURE 37. AMPLIFIER FOR BRIDGE TRANSDUCERS



NOTE A : The typical 30-pA input bias current of the LT1008 will degrade the standard cell by only 1 ppm/year. Noise is a fraction of a ppm. Unprotected gate MOSFET isolates standard cell on power down.

FIGURE 38. SATURATED STANDARD-CELL AMPLIFIER

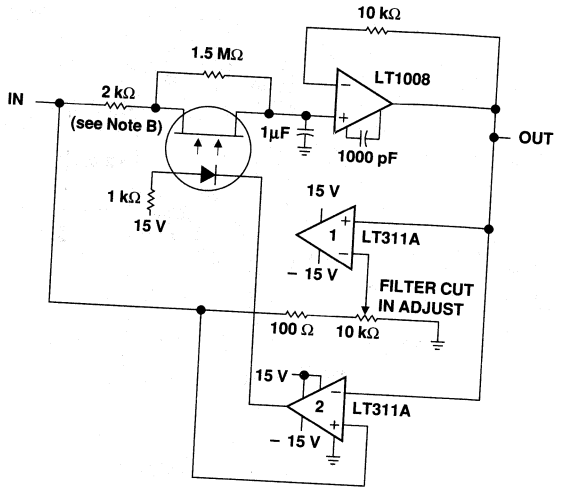
TYPICAL APPLICATION DATA



NOTES: A. This ammeter measures currents from 100 pA to 100 μA without the use of expensive high-value resistors. Accuracy at 100 μA is limited by the offset voltage between Q1 and Q2 and, at 100 pA, by the inverting bias current of the LT1008.
B. Q1-Q4 RCA CA3146 transistor array.
C. Adjust R1 for full-scale deflection with 1-μA input current.

FIGURE 39. AMMETER WITH 6-DECADE RANGE

TYPICAL APPLICATION DATA



NOTES: A. This circuit is useful where fast signal acquisition and high precision are required, as in electronic scales. The filter's time constant is set by the 2-kΩ resistor and the 1-μF capacitor until COMP1 switches. The time constant is then set by the 1.5-MΩ resistor and the 1-μF capacitor. COMP2 provides a quick reset. The circuit settles to a final value three times as fast as a simple 1.5-MΩ, 1-μF filter with almost no dc error.
B. OPTO-MOS switch, Type OFMIA, Theta-J Corp.

FIGURE 40. PRECISION, FAST-SETTLING, LOW-PASS FILTER.

nternally Compensated

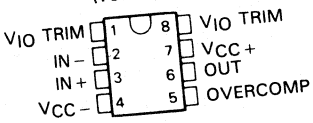
nput Offset Voltage:
LT1012M . . . 35 µV Max
LT1012C . . . 50 µV Max

Input Bias Current (LT1012M):
100 pA Max at 25°C
600 pA Max from −55°C to 125°C

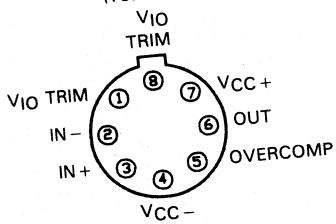
αVIO . . . 1.5 µV/°C Max

- Typical Peak-To-Peak Noise Voltage . . . 0.5 µV at f = 0.1 Hz to 10 Hz
- Low Supply Current . . . 600 µA Max
- CMRR . . . 114 dB Min (LT1012M)
- kSVR . . . 114 dB Min (LT1012M)
- 5-mA Load Current with Voltage Gain of 200,000 Min (LT1012M)

P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



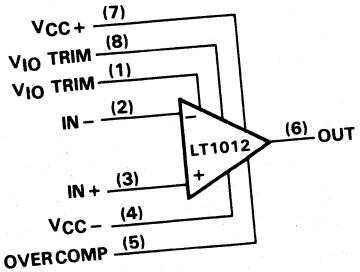
Pin 4 (L package) is in electrical contact with the case.

escription

The LT1012 is an internally compensated operational amplifier that can be used in practically all precision applications. The LT1012 combines picoampere bias currents (maintained over the full temperature range), microvolt offset voltage, low offset voltage temperature coefficient and long-term drift, low voltage and current noise, and low power dissipation. High common-mode and supply voltage rejection ratios, low warm-up drift, and the capability to deliver 5-mA load current with a voltage gain of 200,000 complete the LT1012's precision specifications.

The LT1012M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1012C is characterized for operation from 0°C to 70°C.

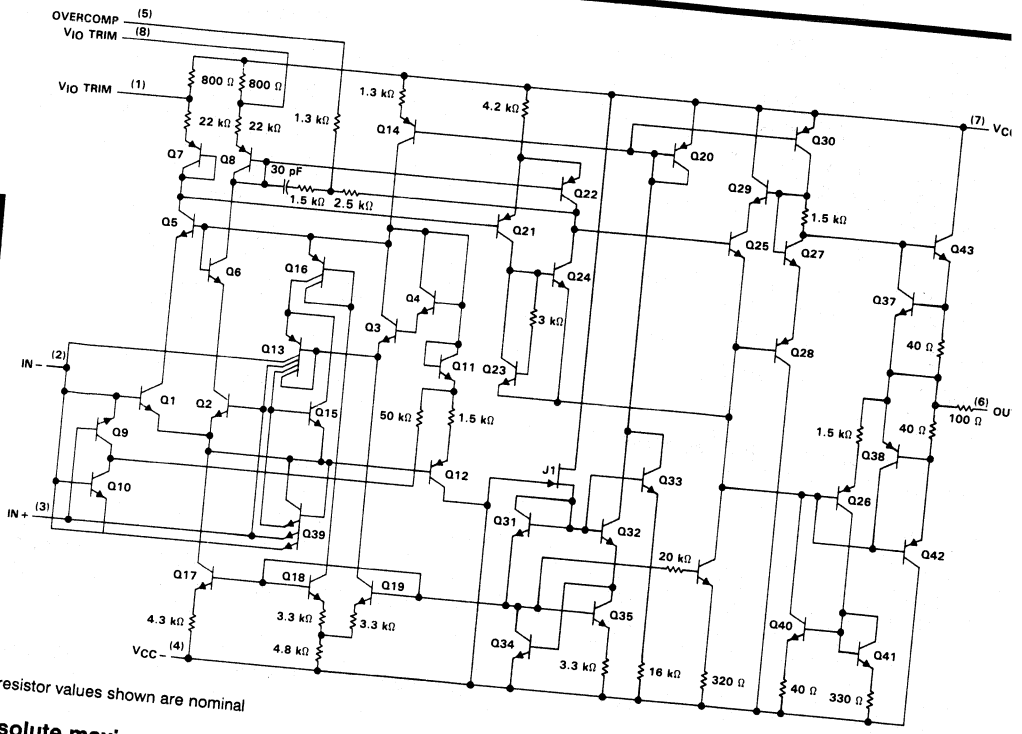
symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE	
		METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	50 µV	LT1012CL	LT1012CP
−55°C to 125°C	35 µV	LT1012ML	–

schematic



All resistor values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	+20 V
Supply voltage, V_{CC-} (see Note 1)	−20 V
Input voltage	$V_{CC\pm}$
Differential input current (see Note 2)	±10 mA
Duration of output short-circuit at or below 25°C	unlimited
Operating free-air temperature range: LT1012M	−55°C to 125°C
LT1012C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: L package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages greater than 1 V cause excessive current to flow through the input protection diodes unless limiting resistance is used.

al characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1012M			LT1012C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
	Input offset voltage	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		8	35		10	50	µV
			Full range			180			120	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		20	90		25	120	
			Full range			250			200	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		20	90		25	120	
			Full range			250			200	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range		0.2	1.5		0.2	1.5	µV/°C
	Average temperature coefficient of input offset voltage		Full range		0.3			0.3		µV/mo
O	Long-term drift of input offset voltage		25°C		0.3					
I_{IO}	Input offset current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		15	100		20	150	pA
			Full range			250			230	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		25	150		30	200	
			Full range			350			300	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		25	150		30	200	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			350			300	
α_{IIO}	Average temperature coefficient of input offset current		Full range		0.3	2.5		0.3	2.5	pA/°C
I_{IB}	Input bias current	$V_{CC\pm}$ = ±15 V, V_{IC} = 0	25°C		±25	±100		±30	±150	pA
			Full range			±600			±230	
		$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		±35	±150		±40	±200	
			Full range			±800			±300	
		$V_{CC\pm}$ = ±2 V to ±20 V	25°C		±35	±150		±40	±200	
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range			±800			±300	
α_{IIB}	Average temperature coefficient of input bias current		Full range		0.6	6		0.3	2.5	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13.5	±14		±13.5	±14		V
			Full range	±13.5			±13.5			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±13	±14		±13	±14		V
			Full range	±13			±13			
A_{VD}	Large-signal differential voltage amplification	V_O = ±12 V, R_L ≥ 10 kΩ	25°C	300	2000		200	2000		V/mV
			Full range	100			100			
		V_O = ±10 V, R_L ≥ 2 kΩ	25°C	200	1000		120	1000		
			Full range	100			100			
CMRR	Common-mode rejection ratio	V_{IC} = ±13.5 V	25°C	114	132		110	132		dB
			Full range	108			108			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±2 V to ±20 V	25°C	114	132		110	132		dB
			Full range	108			108			
		$V_{CC\pm}$ = ±2.5 V to ±20 V	Full range		380	600		380	600	µA
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, V_{IC} = ±13.5 V	25°C		380	600		380	600	
		$V_{CC\pm}$ = ±2 V to ±20 V	Full range			800			800	

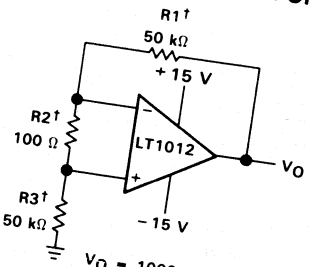
† Full range is −55°C to 125°C for the LT1012M and 0°C to 70°C for the LT1012C.

operating characteristics at T_A = 25°C, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	LT1012M			LT1012C			
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain		0.1	0.2		0.1	0.2		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f= 0.1 Hz to 10 Hz		0.5			0.5	0.65	
V_n	Equivalent input noise voltage	f= 10 Hz, See Note 3		17	30		17	30	nV
		f= 1 kHz		14	22		14	22	
I_n	Equivalent input noise current	f= 10 Hz		20			20		fA/

NOTE 3: This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearir testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION

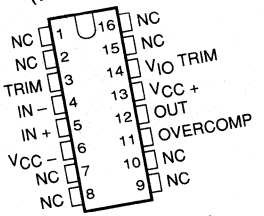


† Resistors must have low thermoelectric potential.
This circuit is also used as the burn-in configuration for the LT1012, with supply voltages increased to ±20 V, R1 = R3 = 20 kΩ, R2 = 200 Ω, A_V = 100.

FIGURE 1. TEST CIRCUIT FOR OFFSET VOLTAGE AND ITS TEMPERATURE COEFFICIENT

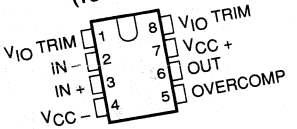
- **ery Low Input Noise Voltage:**
  .1 nV/√Hz Max , 0.85 nV/√Hz Typ at 1 kHz
  or LT1028AM, LT1028AC
- **Low Peak-To-Peak Input Noise Voltage . . .**
  35 nV Typ at f = 0.1 Hz to 10 Hz
- **Noise Voltage and Current 100% Tested**
- **Gain-Bandwidth Product . . . 50 MHz Min**
- **Slew Rate . . . 11 V/μs Min**
- **Input Offset Voltage . . . 40 μV Max at 25°C for LT1028AM, LT1028AC**
- **Offset Voltage Temperature Coefficient . . . 0.8 μV/°C Max for LT1028AM, LT1028AC**
- **Applications:**
  - **Low-Noise Frequency Synthesizers**
  - **High-Quality Audio**
  - **Infrared Detectors**
  - **Accelerometer and Gyro Amplifiers**
  - **350-Ω Bridge Signal Conditioning**
  - **Magnetic Search Coil Amplifiers**
  - **Hydrophone Amplifiers**

DW PACKAGE
(TOP VIEW)

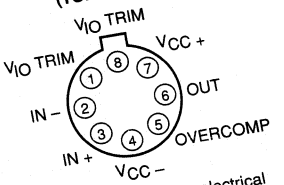


NC – No internal connection

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L package) is in electrical contact with the case.

description

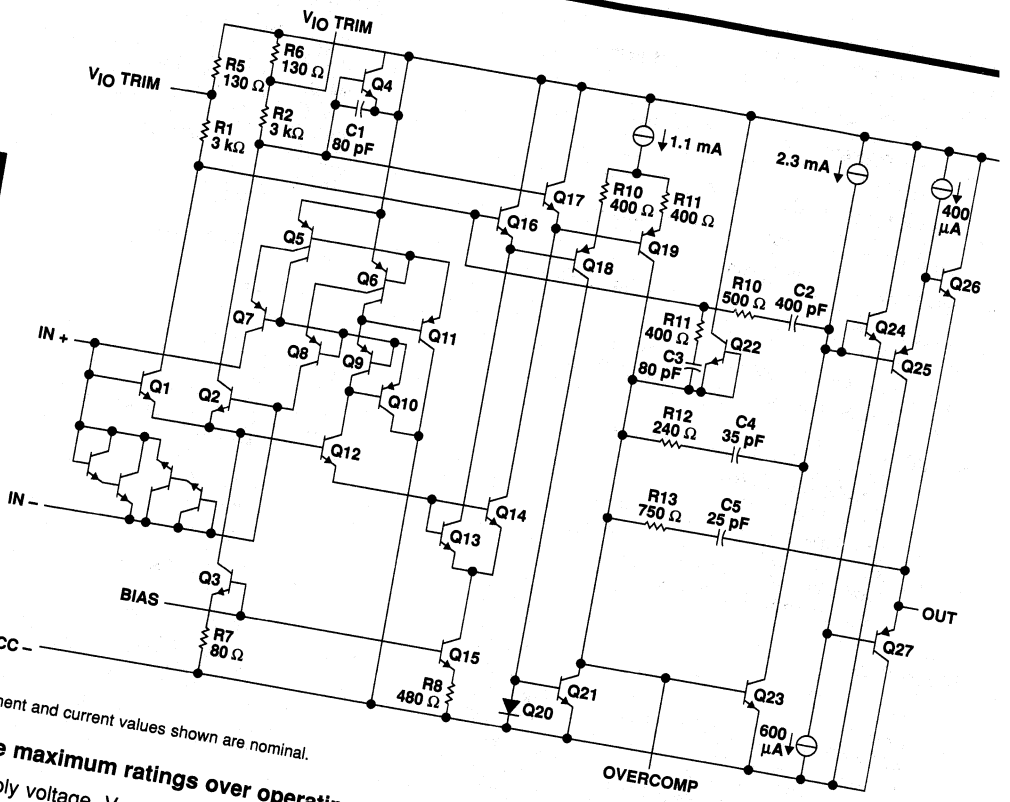
The LT1028 features excellent noise performance combined with high-speed specifications, distortion-free output, and true precision parameters. Although the LT1028 input stage operates at collector currents of nearly 1 mA to achieve low voltage noise, the input bias current is only 25 or 30 nA at 25°C. The noise voltage of the LT1028 is less than the noise of a 50-Ω resistor. Therefore, even in very-low-source-impedance transducer or audio amplifier applications, the device's contribution to total system noise will be negligible.

The LT1028AM and LT1028M are characterized for operation over the full military temperature range of −55°C to 125°C. The LT1028AC and LT1028C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL OUTLINE (DW)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	40 μV	—	LT1028ACJG	LT1028ACL	LT1028ACP
	80 μV	LT1028ACDW	LT1028CJG	LT1028CL	LT1028CP
−55°C to 125°C	40 μV	—	LT1028AMJG	LT1028AML	—
	80 μV	—	LT1028MJG	LT1028ML	—

schematic



All component and current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1): LT1028AM, LT1028M . . . . . 22 V
LT1028AC, LT1028C . . . . . 16 V
Supply voltage, V_{CC-} (see Note 1) LT1028AM, LT1028M . . . . . −22 V
LT1028AC, LT1028C . . . . . −16 V
Differential input current (see Note 2) . . . . . ±25 mA
Input voltage range, V_I (any input, see Note 1) . . . . . $V_{CC}\pm$
Duration of output short-circuit at (or below) 25°C (see Note 2) . . . . . unlimited
Operating free-air temperature, T_A: LT1028AM, LT1028M . . . . . −55°C to 125°C
LT1028AC, LT1028C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The specified values for this parameter takes into account junction temperature increase due to supply and output currents.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1028M			LT1028AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	80		10	40	µV
			– 55°C to 125°C			180			120	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.25	1		0.2	0.8	µV/°C
	Input offset voltage long-term drift	See Note 4	25°C		0.3			0.3		µV/mo
I_{IO}	Input offset current	V_{IC} = 0	25°C		18	100		12	50	nA
			– 55°C to 125°C			180			90	
I_{IB}	Input bias current	V_{IC} = 0	25°C		30	180		25	90	nA
			– 55°C to 125°C			300			150	
V_{ICR}	Common-mode input voltage range		25°C	±11	±12.2		±11	±12.2		V
			– 55°C to 125°C	±10.3			±10.3			
V_{OM}	Maximum peak output voltage swing	R_L ≥ 2 kΩ	25°C	±12	±13		±12.3	±13		V
			– 55°C to 125°C	±10.3			±10.3			
		R_L ≥ 600 Ω	25°C	±10.5	±12.2		±11	±12.2		
A_{VD}	Large-signal differential voltage amplification	V_O = ±12 V, R_L ≥ 2 kΩ	25°C	5	30		7	30		V/µV
		V_O = ±10 V, R_L ≥ 2 kΩ	– 55°C to 125°C	2			3			
		V_O = ±10 V, R_L ≥ 1 kΩ	25°C	3.5	20		5	20		
			– 55°C to 125°C	1.5			2			
		V_O = ±10 V, R_L ≥ 600 Ω	25°C	2	15		3	15		
r_{ic}	Common-mode input resistance		25°C		300			300		MΩ
r_{id}	Differential-mode input resistance		25°C		20			20		kΩ
c_i	Input capacitance		25°C		5			5		pF
z_o	Output impedance	V_O = 0, I_O = 0, Open loop	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		114	126		dB
		V_{IC} = ±10.3 V	– 55°C to 125°C	100			106			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±4 V to ±18V	25°C	110	132		117	133		dB
		$V_{CC\pm}$ = ±4.5 V to ±16V	– 55°C to 125°C	104			110			
I_{CC}	Supply current		25°C		7.6	10.5		7.4	9.5	mA
			– 55°C to 125°C			13			11.5	

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Input offset voltage long-term drift refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 µV.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	LT1028C			LT1028AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 3	25°C		20	80		10	40	μV
			0°C to 70°C			125			80	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.2	1		0.1	0.8	μV/°C
	Input offset voltage long-term drift	See Note 4	25°C		0.3			0.3		μV/mo
I_{IO}	Input offset current	V_{IC} = 0	25°C		18	100		12	50	nA
			0°C to 70°C			130			65	
I_{IB}	Input bias current	V_{IC} = 0	25°C		30	180		25	90	nA
			0°C to 70°C			240			120	
V_{ICR}	Common-mode input voltage range		25°C	±11	±12.2		±11	±12.2		V
			0°C to 70°C	±10.5			±10.5			
V_{OM}	Maximum peak output voltage swing	R_L ≥ 2 kΩ	25°C	±12	±13		±12.3	±13		V
			0°C to 70°C	±11.5			±11.5			
		R_L ≥ 600 Ω	25°C	±10.5	±12.2		±11	±12.2		
		RL ≥ 600 Ω, See Note 2	70°C	±9	±10.5		±9.5	±11		
A_{VD}	Large-signal differential voltage amplification	V_O = ±12 V, R_L ≥ 2 kΩ	25°C	5	30		7	30		V/μV
		V_O = ±10 V, R_L ≥ 2 kΩ	0°C to 70°C	3			5			
		V_O = ±10 V, R_L ≥ 1 kΩ	25°C	3.5	20		5	20		
			0°C to 70°C	2.5			4			
		V_O = ±10 V, R_L ≥ 600 Ω	25°C	2	15		3	15		
r_{ic}	Common-mode input resistance		25°C		300			300		MΩ
r_{id}	Differential-mode input resistance		25°C		20			20		kΩ
c_i	Input capacitance		25°C		5			5		pF
z_o	Output impedance	V_O = 0, I_O = 0, Open loop	25°C		80			80		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	110	126		114	126		dB
		V_{IC} = ±10.3 V	0°C to 70°C	106			110			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±4 V to ±18V	25°C	110	132		117	133		dB
		$V_{CC\pm}$ = ±4.5 V to ±16V	0°C to 70°C	107			114			
I_{CC}	Supply current		25°C		7.6	10.5		7.4	9.5	mA
			0°C to 70°C			11.5			10.5	

NOTES: 2. The specified values for this parameter takes into account junction temperature increase due to supply and output currents.
3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Input offset voltage long-term drift refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics, $V_{CC\pm} = \pm 15$ V, $V_{IC} = 0$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		LT1028M, LT1028C			LT1028AM, LT1028AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate	$A_V = -1$		11	15		11	15		V/μs
V_{NPP}	Peak-to-peak equivalent input noise vlotage	f = 0.1 Hz to 10 Hz			35	90		35	75	nV
V_n	Equivalent input noise voltage	f = 10 Hz,	See Note 5		1	1.9		1	1.7	nV/√Hz
		f = 1 kHz			0.9	1.2		0.85	1.1	
I_n	Equivalent input noise current	f = 10 Hz,	See Note 6		4.7	12		4.7	10	pA/√Hz
		f = 1 kHz,	See Note 6		1	1.8		1	1.6	
GBW	Gain bandwidth product	f = 20 kHz		50	75		50	75		MHz

NOTES: 5. 10-Hz equivalent input noise voltage is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

6. Noise current is defined and measured with balanced source resistors. The resulting voltage (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain noise current. Maximum 10-Hz noise current can be inferred from testing at 1 kHz.

D972, FEBRUARY 1971—REVISED MAY 1988

- **Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Designed to be Interchangeable with Motorola MC1558/MC1458 and Signetics S5558/N5558**

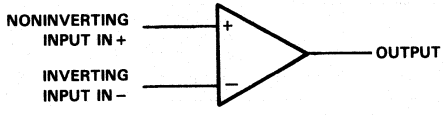
description

The MC1558 and MC1458 are dual general-purpose operational amplifiers with each half electrically similar to the uA741 except that offset null capability is not provided.

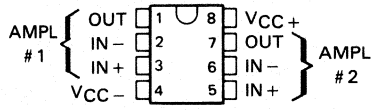
The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The MC1558 is characterized for operation over the full military temperature range of −55°C to 125°C; the MC1458 is characterized for operation from 0°C to 70°C.

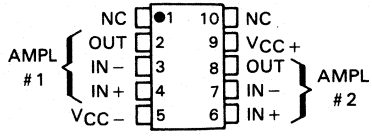
symbol (each amplifier)



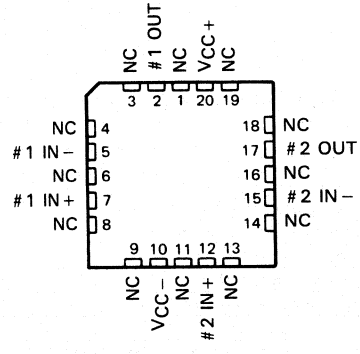
MC1558 . . . JG PACKAGE
MC1458 . . . D, JG, OR P PACKAGE
(TOP VIEW)



MC1558 . . . U FLAT PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



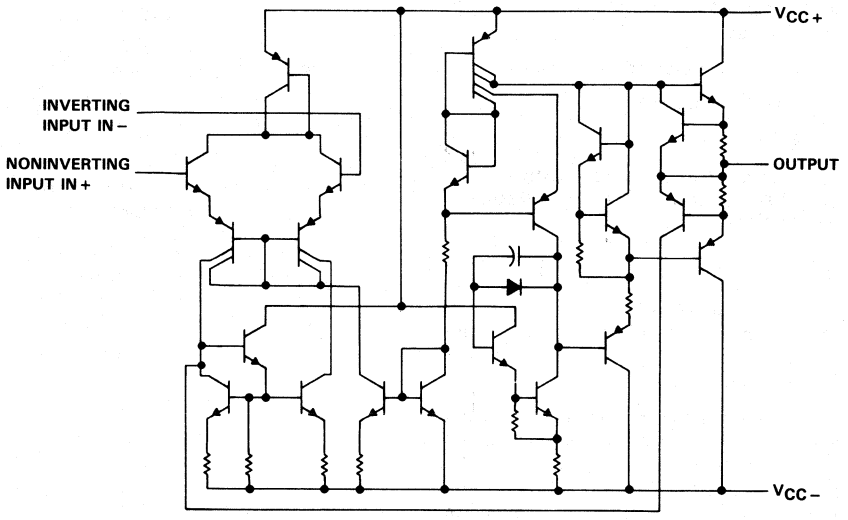
NC—No internal connection

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
MC1558	FK,JG,U	−55°C to 125°C	5 mV
MC1458	D,JG,P	0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e., MC1458DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC1558	MC1458	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage at either input (see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	65 to 150	°C
Case temperature for 60 seconds: FK package		260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	—
FK	680 mW	11.0 mW/°C	88°C	880 mW	275 mW
JG (MC1558)	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
JG (MC1458)	680 mW	6.6 mW/°C	47°C	528 mW	—
P	680 mW	8.0 mW/°C	65°C	640 mW	—
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5		1	6	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50	200		20	200		V/mV
			Full range	25			15			
B_{OM}	Maximum-output-swing bandwidth (closed-loop)	R_L = 2 kΩ, V_O ≥ ±10 V, A_{VD} = 1, THD ≤ 5%	25°C		14			14		kHz
B_1	Unity-gain bandwidth		25°C		1			1		MHz
ϕ_m	Phase margin	A_{VD} = 1	25°C		65°			65°		
A_m	Gain margin		25°C		11			11		dB
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
z_{ic}	Common-mode input impedance	f = 20 Hz	25°C		200			200		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0	25°C	70	90		70	90		dB
			Full Range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0	25°C		30	150		30	150	μV/V
			Full range			150			150	
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 0, f = 1 kHz, BW = 1 Hz	25°C		45			45		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current (both amplifiers)	No load, V_O = 0	25°C		3.4	5		3.4	5.6	mA
			Full range			6.6			6.6	
P_D	Total power dissipation (both amplifiers)	No load, V_O = 0	25°C		100	150		100	170	mW
			Full range			200			200	
V_{o1}/V_{o2}	Crosstalk attenuation		25°C		120			120		dB

†All characteristics are specified under open-loop operating conditions with zero common-mode input voltage unless otherwise specified. Full range for MC1558 is −55°C to 125°C and for MC1458 is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MC1558			MC1458			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.3			0.3		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		5%			5%		
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,		0.5			0.5		V/μs
		C_L = 100 pF,	See Figure 1							

PARAMETER MEASUREMENT INFORMATION

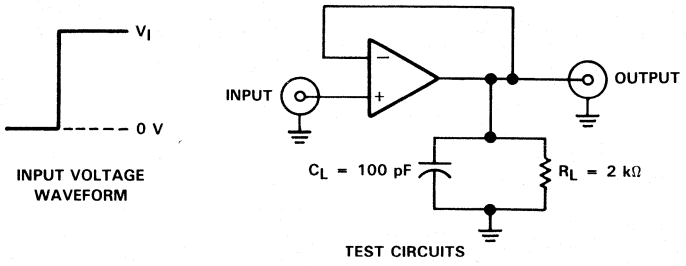


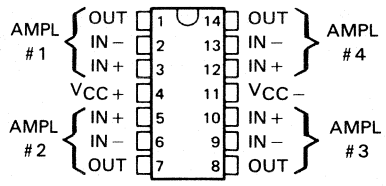
FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2517, FEBRUARY 1979—REVISED MAY 1988

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Designed to be Interchangeable with Motorola MC3303, MC3403**

MC3303, MC3403 . . . D, J, OR N PACKAGE
(TOP VIEW)

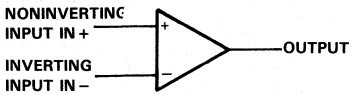


description

The MC3303 and the MC3403 are quadruple operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC} − 1.5 V. Quiescent supply currents are less than one-half those of the uA741.

The MC3303 is characterized for operation from −40°C to 85°C and the MC3403 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

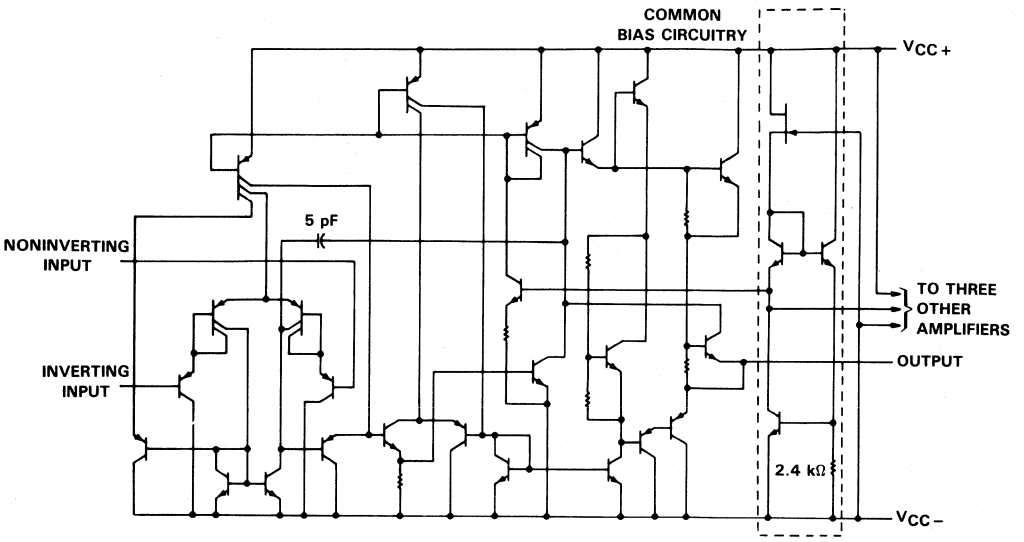


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	MC3403D	MC3403J	MC3403N
−40°C to 85°C	8 mV	MC3303D	MC3303J	MC3303N

D packages are available taped and reeled. Add "R" suffix to the device type when ordering. (e.g., MC3403DR)

schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MC3303	MC3403	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	V
Differential input voltage (see Note 2)		±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature; V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403

PARAMETER		TEST CONDITIONS†		MC3303			MC3403			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	See Note 4	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 4	Full range		10			10		μV/°C
I_{IO}	Input offset current	See Note 4	25°C		30	75		30	50	nA
			Full range			250			200	
α_{IIO}	Temperature coefficient of input offset current	See Note 4	Full range		50			50		pA/°C
I_{IB}	Input bias current	See Note 4	25°C		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 12	V_{CC-} to 12.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	12	12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	10	12		±10	±13		
		R_L = 2 kΩ	Full range	10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	C_L = 200 pF, R_L = 2 kΩ	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±2.5 to ±15 V	25°C		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§		25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	No load, See Note 4	25°C		2.8	7		2.8	7	mA

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for MC3303, and 0°C to 70°C for MC3403.
‡The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.
§Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
NOTE 4: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at V_O = 0 for MC3403, and V_O = 7 V for MC3303.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MC3303			MC3403			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V			10		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V			−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	V_{CC+} − 1.7			V_{CC+} − 1.7			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±15 V to ±2.5 V			150			150	μV/V
I_{CC}	Supply current	No load, V_O = 2.5 V		2.5	7		2.5	7	mA
V_{o1}/V_{o2}	Crosstalk attenuation	f = 1 kHz to 20 kHz		120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡Output will swing essentially to ground.

operating characteristics, V_{CC+} = 14 V, V_{CC-} = 0 V for MC3303; $V_{CC\pm}$ = ±15 V for MC3403; T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, R_L = 2 kΩ, See Figure 1		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		μs
t_f	Fall time			0.35		μs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

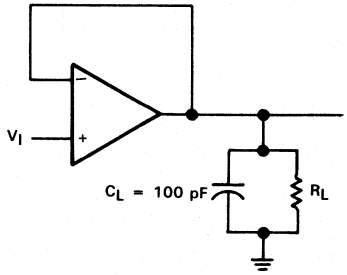


FIGURE 1. UNITY-GAIN AMPLIFIER

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

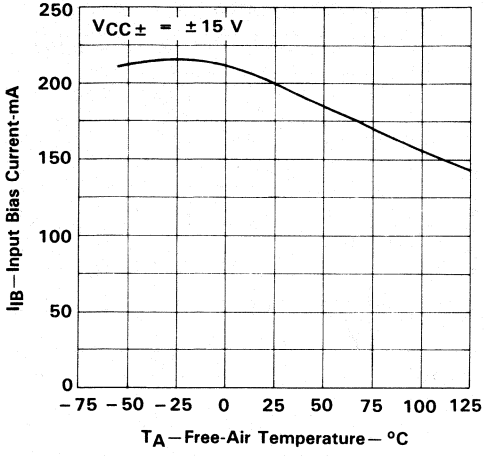


FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

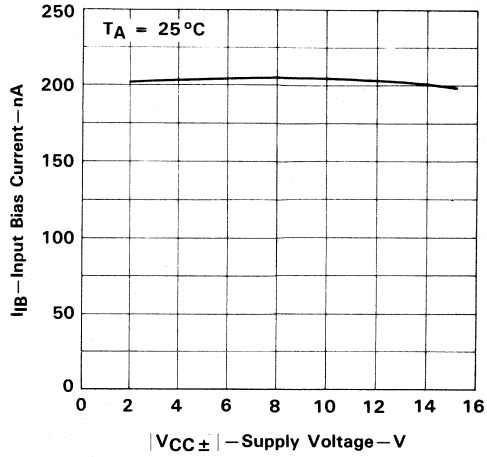


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

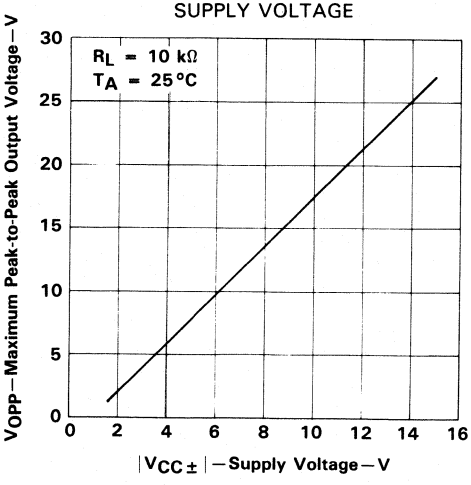


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

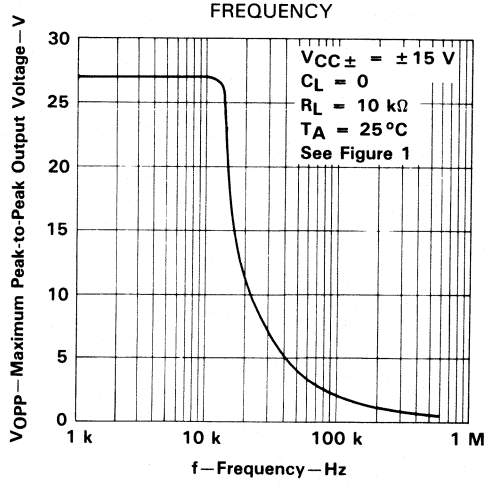


FIGURE 5

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

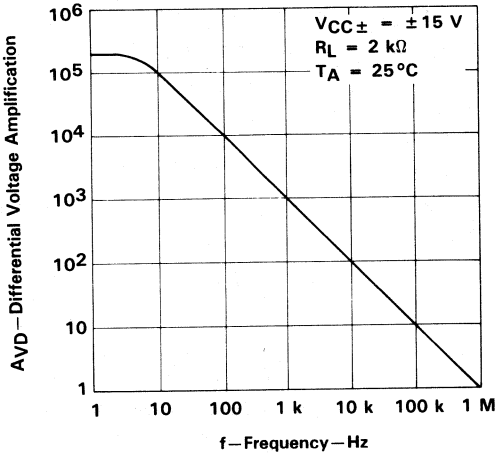


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

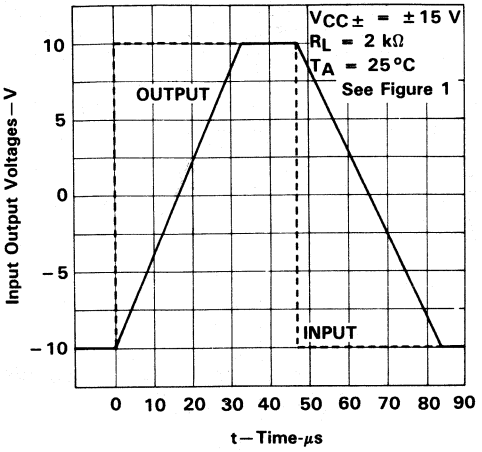


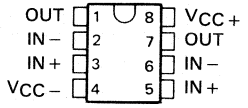
FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

D2563, NOVEMBER 1979 – REVISED MAY 1988

- **Equivalent Input Noise Voltage . . . 5 nV/$\sqrt{Hz}$ Typ at 1 kHz**
- **Unity-Gain Bandwidth . . . 10 MHz Typ**
- **Common-Mode Rejection Ratio . . . 100 dB Typ**
- **High DC Voltage Gain . . . 100 V/m Typ**
- **Peak-to-Peak Output Voltage Swing . . . 32 V Typ with $V_{CC\pm}$ = ±18 V and R_L = 600 Ω**
- **High Slew Rate . . . 9 V/μs Typ**
- **Wide Supply Voltage Range . . . ±3 V to ±20 V**
- **Designed to be Interchangeable with Signetics NE5532 and NE5532A**

NE5532, NE5532A . . . JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



Description

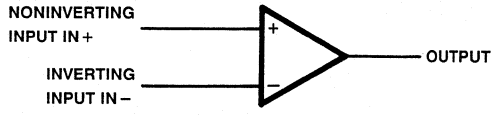
The NE5532 and NE5532A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are internally compensated for unity gain operation. The NE5532A has specified maximum limits for equivalent input noise voltage.

The NE5532 and NE5532A are characterized for operation from 0°C to 70°C.

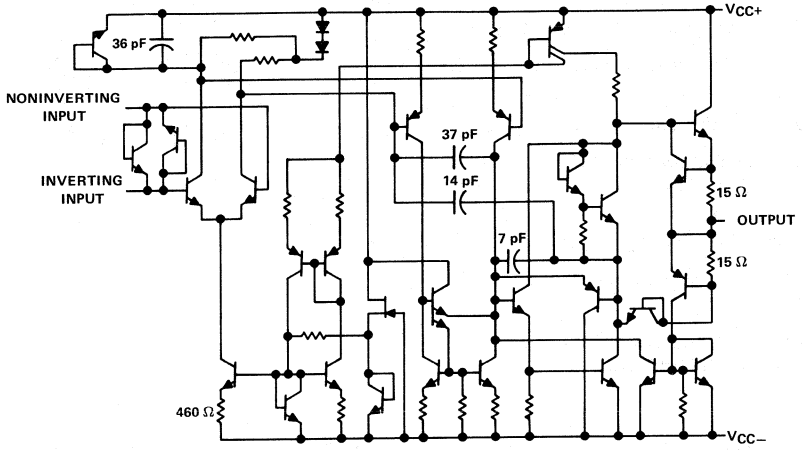
AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE	
		CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5532JG NE5532AJG	NE5532P NE5532AP

Symbol (each amplifier)



schematic (each amplifier)



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −22 V
Input voltage, either input (see Notes 1 and 2) . . . . . $V_{CC\pm}$
Input current (see Note 3) . . . . . ±10 mA
Duration of output short-circuit (see Note 4) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

electrical characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C			0.5	4	mV
			T_A = 0°C to 70°C				5	
I_{IO}	Input offset current	T_A = 25°C				10	150	nA
		T_A = 0°C to 70°C					200	
I_{IB}	Input bias current	T_A = 25°C				200	800	nA
		T_A = 0°C to 70°C					1000	
V_{ICR}	Common-mode input voltage range				±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L ≥ 600 Ω	$V_{CC\pm}$ = ±15 V		24	26		V
			$V_{CC\pm}$ = ±18 V		30	32		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 600 Ω, V_O = ±10 V	T_A = 25°C		15	50		V/mV
			T_A = 0°C to 70°C		10			
		R_L ≥ 2 kΩ, V_O = ±10 V	T_A = 25°C		25	100		
			T_A = 0°C to 70°C		15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz				2.2		V/mV
B_{OM}	Maximum-output-swing bandwidth	R_L = 600 Ω,	V_O = ±10 V			140		kHz
		R_L = 600 Ω,	$V_{CC\pm}$ = ±18 V,	V_O = ±14 V		100		
B_1	Unity-gain bandwidth	R_L = 600 Ω,	C_L = 100 pF			10		MHz
r_i	Input resistance				30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB,	R_L = 600 Ω,	f = 10 kHz		0.3		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min			70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0			80	100		dB
I_{OS}	Output short-circuit current					38		mA
I_{CC}	Total supply current	No load,	V_O = 0			8	16	mA
V_{o1}/V_{o2}	Crosstalk attenuation	V_{o1} = 10 V peak,	f = 1 kHz			110		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

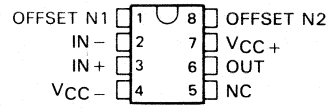
operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	NE5532			NE5532A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/ms
	Overshoot factor	V_I = 100 mV, A_{VD} = 1, R_L = 600 Ω, C_L = 100 pF		10%			10%		
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

D2757, OCTOBER 1983—REVISED JUNE 1988

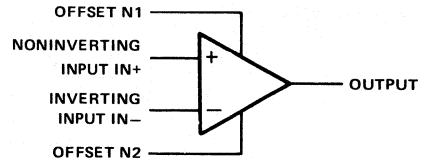
- **Ultra-Low Offset Voltage . . .30 μV Typ (OP-07E)**
- **Ultra-Low Offset Voltage Temperature Coefficient . . . 0.3 μV/°C Typ (OP-07E)**
- **Ultra-Low Noise**
- **No External Components Required**
- **Replaces Chopper Amplifiers at a Lower Cost**
- **Single-Chip Monolithic Fabrication**
- **Wide Input Voltage Range 0 to ±14 V Typ**
- **Wide Supply Voltage Range ±3 V to ±18 V**
- **Essentially Equivalent to Fairchild μA714 Operational Amplifiers**
- **Direct Replacement for PMI OP-07C, OP-07D, OP-07E**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol



description

These devices represent a breakthrough in operational amplifier performance. Low offset and long-term stability are achieved by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are required for offset nulling and frequency compensation. The true differential input, with a wide input voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP-07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

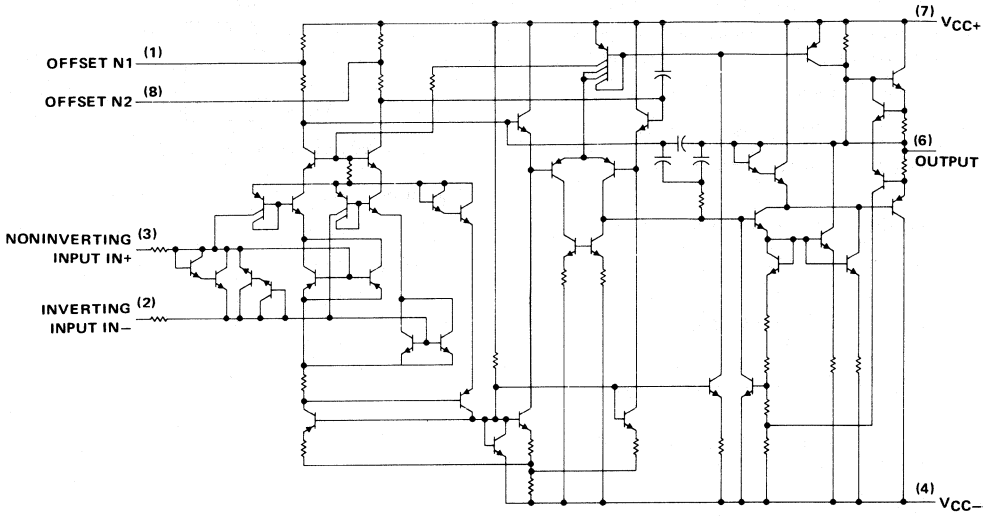
These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	150 μV	OP-07CD OP-07DD	OP-07CJG OP-07DJG	OP-07CP OP-07DP
	75 μV	OP-07ED	OP-07EJG	OP-07EP

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., OP-07CDR)

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	22 V
Supply voltage V_{CC-}	–22 V
Differential input voltage (see Note 2)	±30 V
Input voltage (either input, see Note 3)	±22 V
Duration of output short circuit (see Note 4)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 5)	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.
5. For operation above 64°C free-air temperature, derate the D package to 464 mW at 70°C at the rate of 5.8 mW/°C.

electrical characteristics at specified free-air temperature, $V_{CC}\pm$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		OP-7C			OP-7D			OP-7E			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		60	150		60	150		30	75	μV
			0°C to 70°C		85	250		85	250		45	130	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	0°C to 70°C		0.5	1.8		0.7	2.5		0.3	1.3	μV/°C
	Long-term drift of input offset voltage	See Note 6			0.4			0.5			0.3		μV/mo
	Offset adjustment range	R_S = 20 kΩ, See Figure 1	25°C		±4			±4			±4		mV
I_{IO}	Input offset current		25°C		0.8	6		0.8	6		0.5	3.8	nA
			0°C to 70°C		1.6	8		1.6	8		0.9	5.3	
α_{IIO}	Temperature coefficient of input offset current		0°C to 70°C		12	50		12	50		8	35	pA/°C
I_{IB}	Input bias current		25°C		±1.8	±7		±2	±12		±1.2	±4	nA
			0°C to 70°C		±2.2	±9		±3	±14		±1.5	±5.5	
α_{IIB}	Temperature coefficient of input bias current		0°C to 70°C		18	50		18	50		13	35	pA/°C
V_{ICR}	Common-mode input voltage range		25°C	±13	±14		±13	±14		±13	±14		V
			0°C to 70°C	±13	±13.5		±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	R_L ≥ 10 kΩ	25°C	±12	±13		±12	±13		±12.5	±13		V
		R_L ≥ 2 kΩ		±11.5	±12.8		±11.5	±12.8		±12	±12.8		
		R_L ≥ 1 kΩ			±12			±12		±10.5	±12		
		R_L ≥ 2 kΩ	0°C to 70°C	±11	±12.6		±11	±12.6		±12	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±3 V, V_O = ±0.5 V, R_L ≥ 500 kΩ	25°C	100	400			400		150	400		V/mV
		V_O = ±10 V, R_L = 2 kΩ	25°C	120	400		120	400		200	500		
			0°C to 70°C	100	400		100	400		180	450		
B_1	Unity gain bandwidth		25°C	0.4	0.6		0.4	0.6		0.4	0.6		MHz
r_i	Input resistance		25°C	8	33		7	31		15	50		MΩ
CMRR	Common-mode rejection ratio	V_{IC} = ±13 V, R_S = 50 Ω	25°C	100	120		94	110		106	123		dB
			0°C to 70°C	97	120		94	106		103	123		
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±3 V to ±18 V, R_S = 50 Ω	25°C		7	32		7	32		5	20	μV/V
			0°C to 70°C		10	51		10	51		7	32	
P_D	Power dissipation	V_O = 0, No load	25°C		80	150		80	150		75	120	mW
		$V_{CC\pm}$ = ±3 V, V_O = 0, No load			4	8		4	8		4	6	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		OP-07C			OP-07D			OP-07E			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_n	Equivalent input noise voltage	T_A = 25°C	f = 10 Hz		10.5			10.5			10.3		nV/√Hz
			f = 100 Hz		10.2			10.3			10.0		
			f = 1 kHz		9.8			9.8			9.6		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, T_A = 25°C			0.38			0.38			0.35		μV
I_n	Equivalent input noise current	T_A = 25°C	f = 10 Hz		0.35			0.35			0.32		pA/√Hz
			f = 100 Hz		0.15			0.15			0.14		
			f = 1 kHz		0.13			0.13			0.12		
I_{NPP}	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz, T_A = 25°C			15			15			14		pA
SR	Slew rate	$R_L \geq 2$ kΩ, T_A = 25°C			0.3			0.3			0.3		V/μs

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

TYPICAL APPLICATION DATA

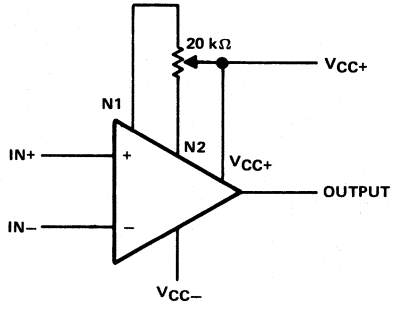


FIGURE 1. INPUT OFFSET VOLTAGE NULL CIRCUIT

- **Direct Replacements for PMI and LTC OP-27 and OP-37 Series**

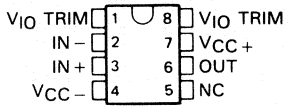
Features of OP-27A, OP-27C, OP-37A, and OP-37C:

- **Maximum Equivalent Input Noise Voltage: 3.8 nV/$\sqrt{Hz}$ at 1 kHz 5.5 nV/$\sqrt{Hz}$ at 10 Hz**
- **Very Low Peak-to-Peak Noise Voltage at 0.1 Hz to 10 Hz . . . 80 nV Typ**
- **Low Input Offset Voltage . . . 25 μV Max**
- **High Voltage Amplification . . . 1 V/μV Min**

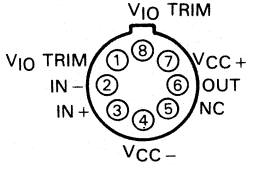
Feature of OP-37 Series:

- **Minimum Slew Rate . . . 11 V/μs**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



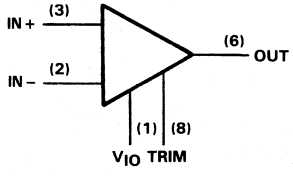
NC—No internal connection

description

The OP-27 and OP-37 operational amplifiers combine outstanding noise performance with excellent precision and high-speed specifications. The wideband noise is only 3 nV/$\sqrt{Hz}$, and with the 1/f noise corner at 2.7 Hz, low noise is maintained for all low-frequency applications.

The outstanding characteristics of the OP-27 and OP-37 make these devices excellent choices for low-noise amplifier applications requiring precision performance and reliability. Additionally, the OP-37 is free of latch-up in high-gain, large-capacitive-feedback configurations.

symbol



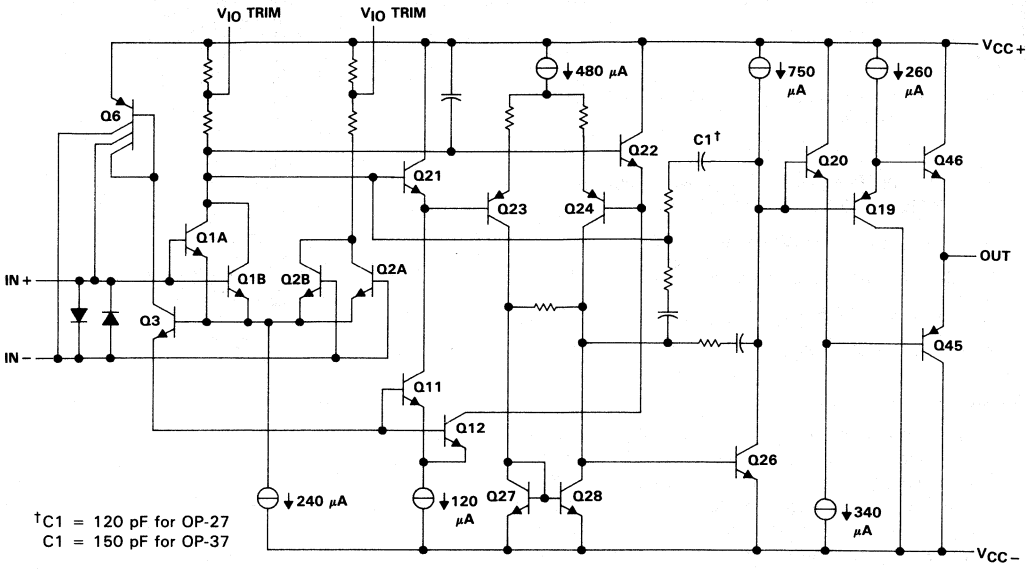
The OP-27 series is compensated for unity gain. The OP-37 series is decompensated for increased bandwidth and slew rate and is stable down to a gain of 5.

The OP-27A, OP-27C, OP-37A, and OP-37C are characterized for operation over the full military temperature range of −55°C to 125°C. The OP-27E, OP-27G, OP-37E, and OP-37G are characterized for operation from −25°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	STABLE GAIN	PACKAGE		
			CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
−25°C to 85°C	25 μV	1	OP27EJG	OP27EL	OP27EP
		5	OP37EJG	OP37EL	OP37EP
	100 μV	1	OP27GJG	OP27GL	OP27GP
		5	OP37GJG	OP37GL	OP37GP
−55°C to 125°C	25 μV	1	OP27AJG	OP27AL	OP27AP
		5	OP37AJG	OP37AL	OP37AP
	100 μV	1	OP27CJG	OP27CL	OP27CP
		5	OP37CJG	OP37CL	OP37CP

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −22 V
Input voltage . . . . . $V_{CC\pm}$
Duration of output short circuit . . . . . unlimited
Differential input current (see Note 2) . . . . . ±25 mA
Continuous power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: OP-27A, OP-27C, OP-37A, OP-37C . . . . . −55°C to 125°C
OP-27E, OP-27G, OP-37E, OP-37G . . . . . −25°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} unless otherwise noted.
2. The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Excessive input current will flow if a differential input voltage in excess of approximately ±0.7 V is applied between the inputs unless some limiting resistance is used.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG (OP-27A, OP-27C, OP-37A, OP-37C)	1050 mW	8.4 mW/°C	546 mW	210 mW
JG (OP-27E, OP-27G, OP-37E, OP-37G)	825 mW	6.6 mW/°C	429 mW	N/A
L (OP-27A, OP-27C, OP-37A, OP-37C)	825 mW	6.6 mW/°C	429 mW	165 mW
L (OP-27E, OP-27G, OP-37E, OP-37G)	650 mW	5.2 mW/°C	338 mW	N/A
P	1000 mW	8.0 mW/°C	520 mW	N/A

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ecommended operating conditions

		OP-27A, OP-37A			OP-27C, OP-37C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}		4	15	22	4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	−4	−15	−22	V
Common-mode input voltage, V_{ICR}	$V_{CC\pm}$ = ±15 V, T_A = 25°C			±11			±11	V
	$V_{CC\pm}$ = ±15 V, T_A = −55°C to 125°C			±10.3			±10.2	
Operating free-air temperature, T_A		−55		125	−55		125	°C

lectrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP-27A, OP-37A			OP-27C, OP-37C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0	25°C		10	25		30	100	µV
		R_S = 50 Ω, See Note 3	−55°C to 125°C			60			300	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		−55°C to 125°C		0.2	0.6		0.4	1.8	µV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		7	35		12	75	nA
			−55°C to 125°C			50			135	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±10	±40		±15	±80	nA
			−55°C to 125°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−55°C to 125°C	±10.3			±10.2			
V_{OM}	Peak output voltage swing	R_L ≥ 2 kΩ	25°C	±12	±13.8		±11.5	±13.5		V
		R_L ≥ 0.6 kΩ		±10	±11.5		±10	±11.5		
		R_L ≥ 2 kΩ	−55°C to 125°C	±11.5			±10.5			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	1000	1800		700	1500		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V		800	1500			1500		
		R_L ≥ 0.6 kΩ, V_O = ±1 V, V_{CC} = ± 4 V		250	700		200	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	−55°C to 125°C	600			300			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	V_O = 0, I_O = 0	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	114	126		100	120		dB
		V_{IC} = ±10 V	−55°C to 125°C	108			94			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	100	120		94	118		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	−55°C to 125°C	96			86			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 µV. See Figure 3.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4	15	22	V
Supply voltage, V_{CC-}		−4	−15	−22	V
Common-mode input voltage, range	$V_{CC\pm}$ = ±15 V, T_A = 25°C			±11	V
	$V_{CC\pm}$ = ±15 V, T_A = −55°C to 125°C			±10.5	
Operating free-air temperature, T_A		−25		85	°C

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	OP-27E, OP-37E			OP-27G, OP-37G			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0	25°C		10	25		30	100	μV
		R_S = 50 Ω, See Note 3	−25°C to 85°C			50			220	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		−25°C to 85°C		0.2	0.6		0.4	1.8	μV/°C
	Long-term drift of input offset voltage	See Note 4			0.2	1		0.4	2	μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0	25°C		7	35		12	75	nA
			−25°C to 85°C			50			135	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0	25°C		±10	±40		±15	±80	nA
			−25°C to 85°C			±60			±150	
V_{ICR}	Common-mode input voltage range		25°C	±11			±11			V
			−25°C to 85°C	±10.5			±10.5			
V_{OM}	Peak output voltage swing	R_L ≥ 2 kΩ	25°C	±12	±13.8		±11.5	±13.5		V
		R_L ≥ 0.6 kΩ		±10	±11.5		±10	±11.5		
		R_L ≥ 2 kΩ	−25°C to 85°C	±11.7			±11			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	1000	1800		700	1500		V/mV
		R_L ≥ 1 kΩ, V_O = ±10 V		800	1500			1500		
		R_L ≥ 0.6 kΩ, V_O = ±1 V, V_{CC} = ±4 V		250	700		200	500		
		R_L ≥ 2 kΩ, V_O = ±10 V	−25°C to 85°C	750			450			
$r_{i(CM)}$	Common-mode input resistance				3			2		GΩ
r_o	Output resistance	V_O = 0, I_O = 0	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = ±11 V	25°C	114	126		100	120		dB
		V_{IC} = ±10 V	−25°C to 85°C	110			96			
k_{SVR}	Supply voltage rejection ratio	$V_{CC\pm}$ = ±4 V to ±18 V	25°C	100	120		94	118		dB
		$V_{CC\pm}$ = ±4.5 V to ±18 V	−25°C to 85°C	97			90			

NOTES: 3. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after applying power.
4. Long-term drift of input offset voltage refers to the average trend line of offset voltage versus time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{IO} during the first 30 days are typically 2.5 μV. See Figure 3.

OP-27 operating characteristics over operating free-air temperature range, $V_{CC\pm}$ = ± 15 V

PARAMETER		TEST CONDITIONS	OP-27A, OP-27E			OP-27C, OP-27G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 1$, $R_L \geq 2$ kΩ	1.7	2.8		1.7	2.8		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, RS = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω,		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 100 kHz	5	8		5	8		MHz

OP-37 operating characteristics over operating free-air temperature range, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS	OP-37A, OP-37E			OP-37C, OP-37G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$A_{VD} \geq 5$, $R_L \geq 2$ kΩ	11	17		11	17		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz, R_S = 100 Ω, See Figure 34		0.08	0.18		0.09	0.25	μV
V_n	Equivalent input noise voltage	f = 10 Hz, R_S = 100 Ω		3.5	5.5		3.8	8	nV/√Hz
		f = 30 Hz, R_S = 100 Ω		3.1	4.5		3.3	5.6	
		f = 1 kHz, R_S = 100 Ω		3.0	3.8		3.2	4.5	
I_n	Equivalent input noise current	f = 10 Hz, See Figure 35		1.5	4		1.5		pA/√Hz
		f = 30 Hz, See Figure 35		1.0	2.3		1.0		
		f = 1 kHz, See Figure 35		0.4	0.6		0.4	0.6	
GBW	Gain bandwidth product	f = 10 kHz	45	63		45	63		MHz
		$A_V \geq 5$, f = 1 MHz		40			40		

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	vs Temperature	1
ΔV_{IO}	Change in input offset voltage	vs Time after power-on	2
		vs Time (long-term drift)	3
I_{IO}	Input offset current	vs Temperature	4
I_{IB}	Input bias current	vs Temperature	5
V_{ICR}	Common-mode input voltage range	vs Supply voltage	6
V_{OM}	Maximum peak output voltage	vs Load resistance	7
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	8, 9
A_{VD}	Differential voltage amplification	vs Supply voltage	10
		vs Load resistance	11
		vs Frequency	12, 13, 14
CMRR	Common-mode rejection ratio	vs Frequency	15
k_{SVR}	Supply voltage rejection ratio	vs Frequency	16
SR	Slew rate	vs Temperature	17
		vs Supply voltage	18
		vs Load resistance	19
ϕ_m	Phase margin	vs Temperature	20, 21
ϕ	Phase shift	vs Frequency	12, 13
V_n	Equivalent input noise voltage	vs Bandwidth	22
		vs Source resistance	23
		vs Supply voltage	24
		vs Temperature	25
		vs Frequency	26
I_n	Equivalent input noise current	vs Frequency	27
GBW	Gain bandwidth product	vs Temperature	20, 21
I_{OS}	Short-circuit output current	vs Time	28
I_{CC}	Supply current	vs Supply voltage	29
	Pulse response	Small-signal	30, 32
		Large-signal	31, 33

TYPICAL CHARACTERISITCS†

INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNIT
vs
FREE-AIR TEMPERATURE

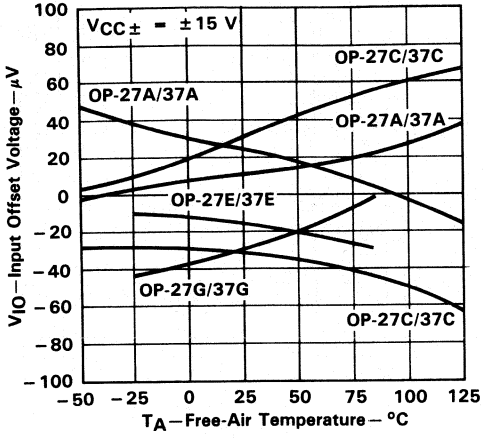

FIGURE 1

WARM-UP CHANGE IN
INPUT OFFSET VOLTAGE
vs
ELAPSED TIME

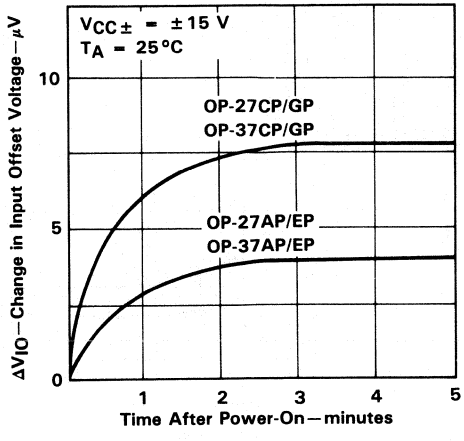

FIGURE 2

LONG-TERM DRIFT OF
INPUT OFFSET VOLTAGE
OF REPRESENTATIVE UNITS

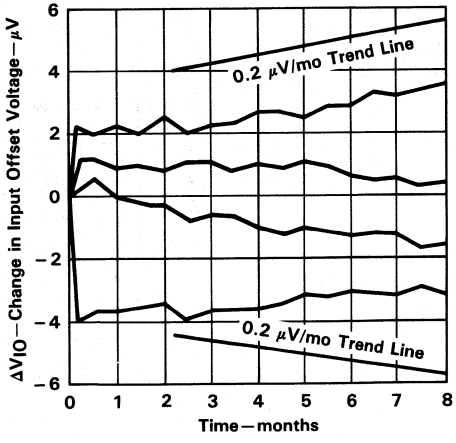

FIGURE 3

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

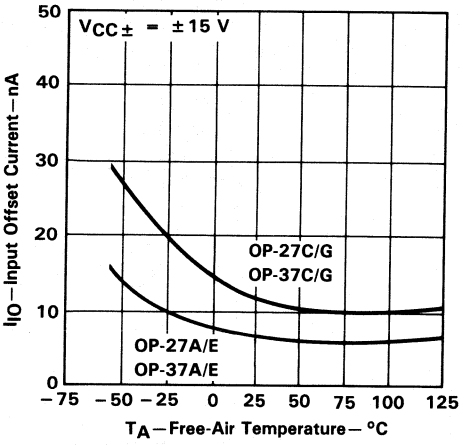

FIGURE 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

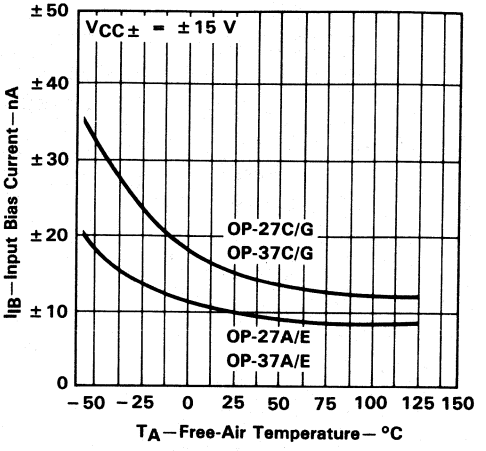

FIGURE 5

COMMON-MODE INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

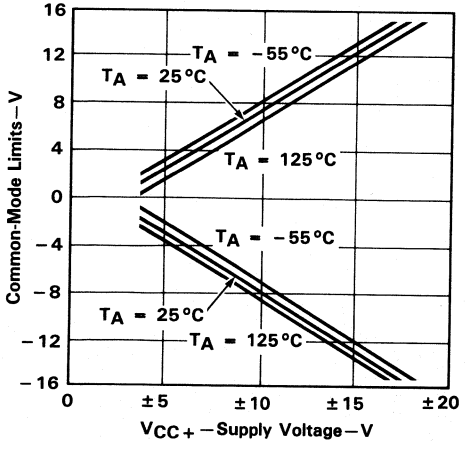

FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

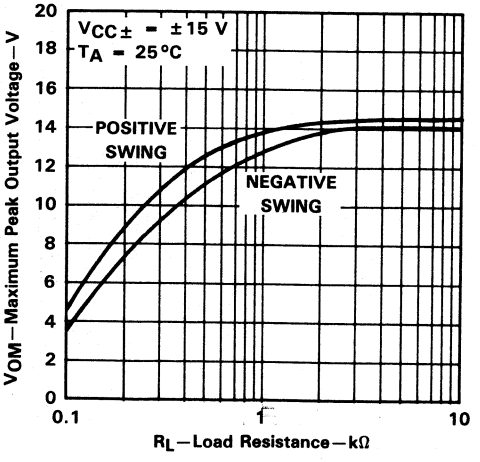

FIGURE 7

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

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TYPICAL CHARACTERISTICS

OP-27
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

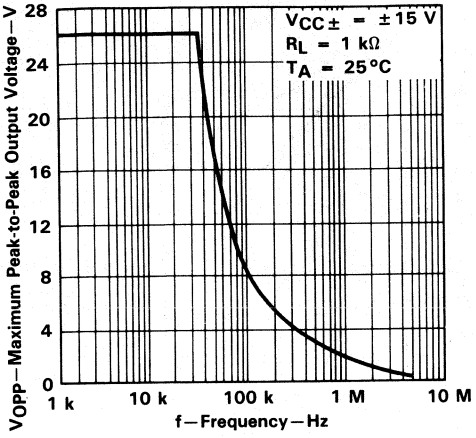


FIGURE 8

OP-37
MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

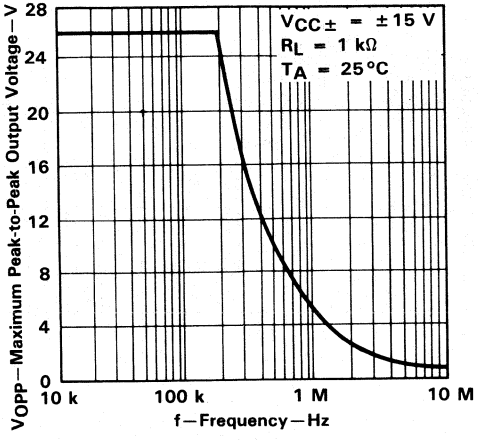


FIGURE 9

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
TOTAL SUPPLY VOLTAGE

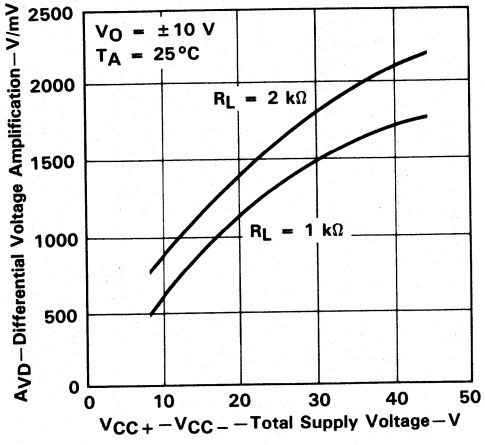


FIGURE 10

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

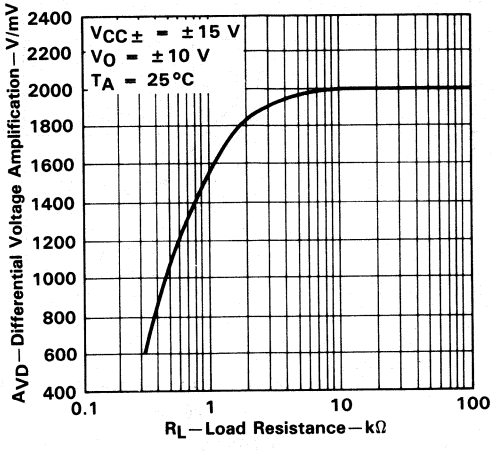


FIGURE 11

TYPICAL CHARACTERISTICS

OP-27
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

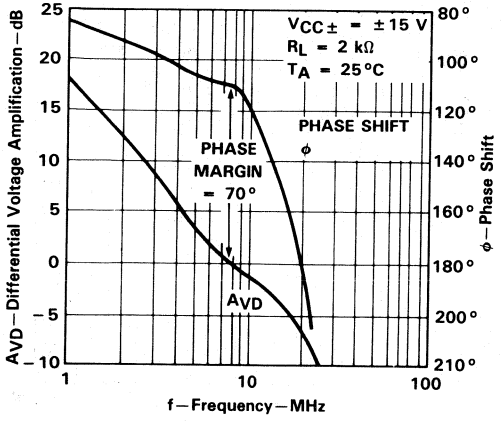


FIGURE 12

OP-37
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

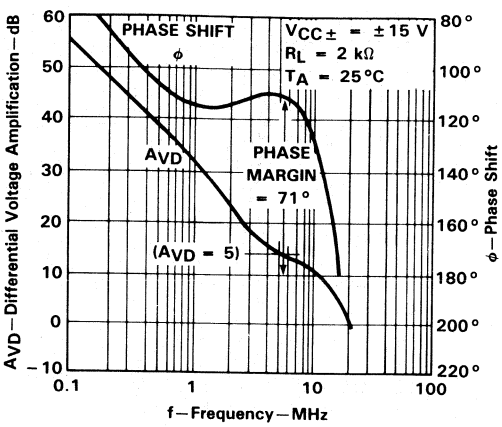


FIGURE 13

OP-27A, OP-27E, OP-37A, OP-37E
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY

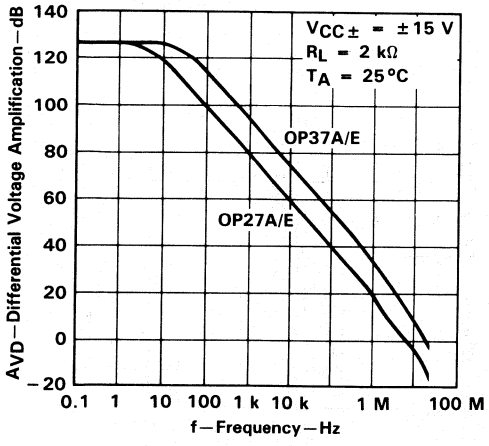


FIGURE 14

OP-27A, OP-27E, OP-37A, OP-37E
COMMON-MODE REJECTION RATIO vs FREQUENCY

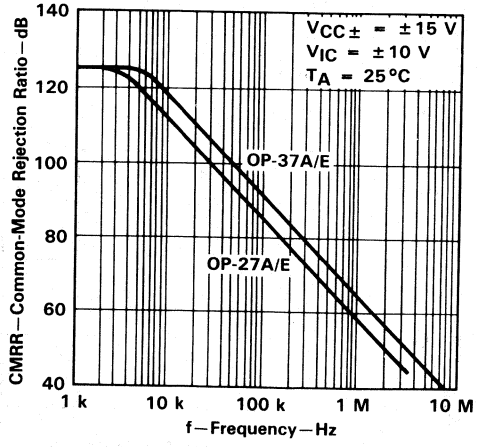


FIGURE 15

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

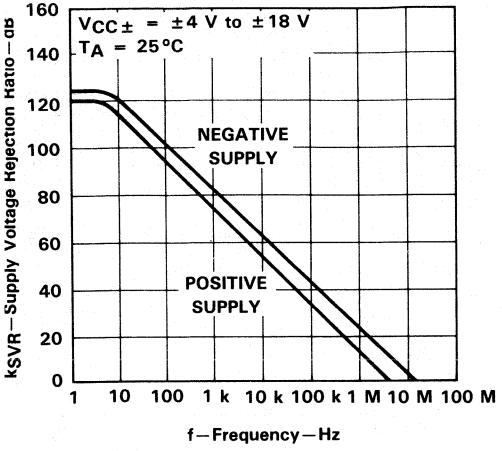


FIGURE 16

SLEW RATE
vs
FREE-AIR TEMPERATURE

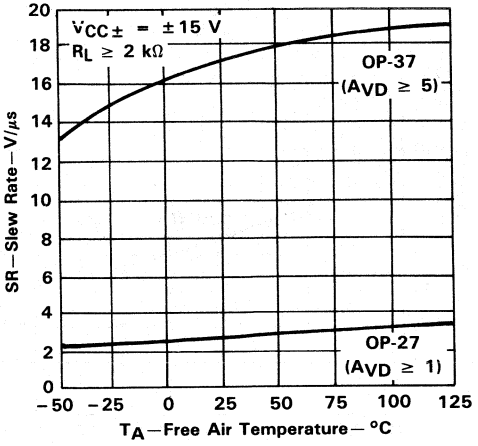


FIGURE 17

OP-37
SLEW RATE
vs
SUPPLY VOLTAGE

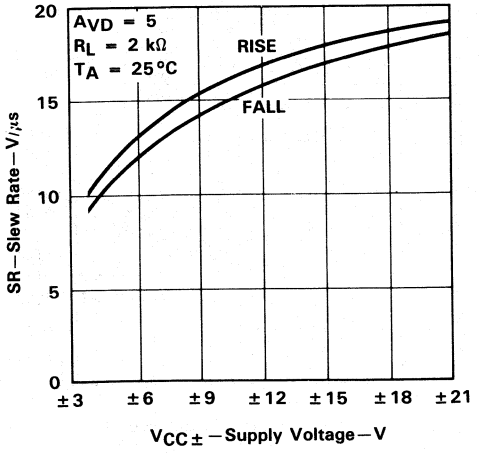


FIGURE 18

OP-37
SLEW RATE
vs
LOAD RESISTANCE

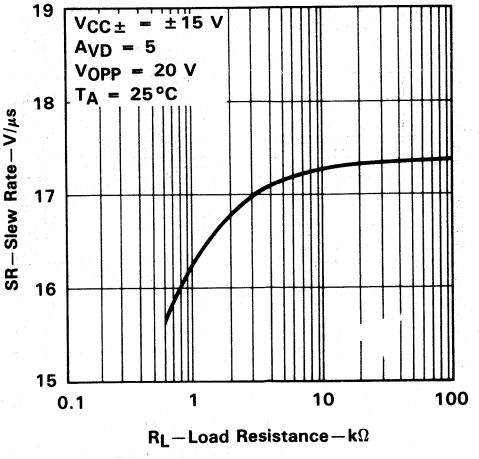


FIGURE 19

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

OP-27
PHASE MARGIN AND
GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

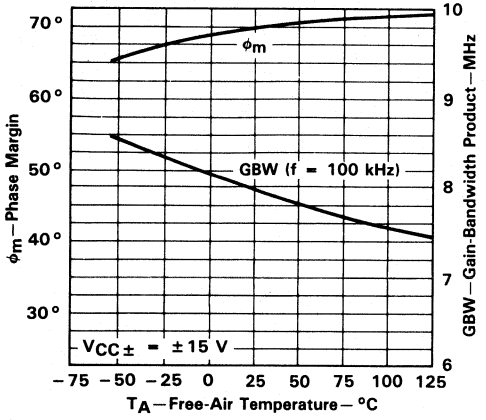


FIGURE 20

OP-37
PHASE MAGIN AND
GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

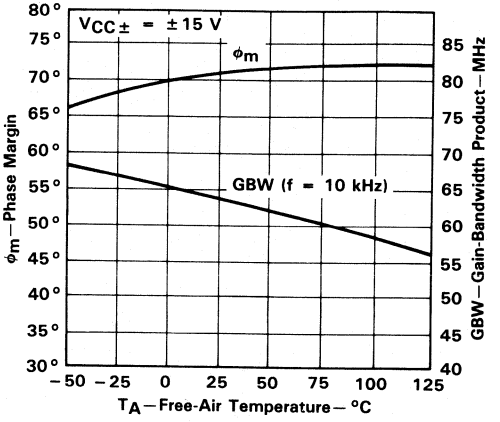


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
vs
BANDWIDTH

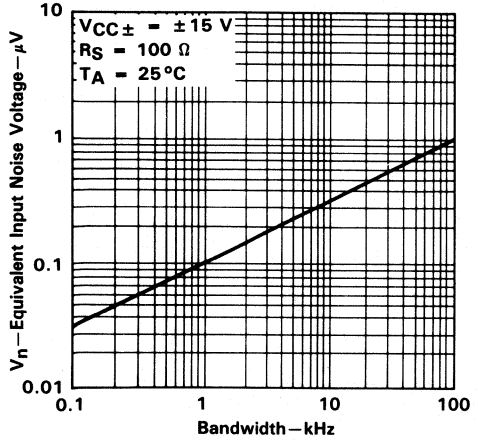


FIGURE 22

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

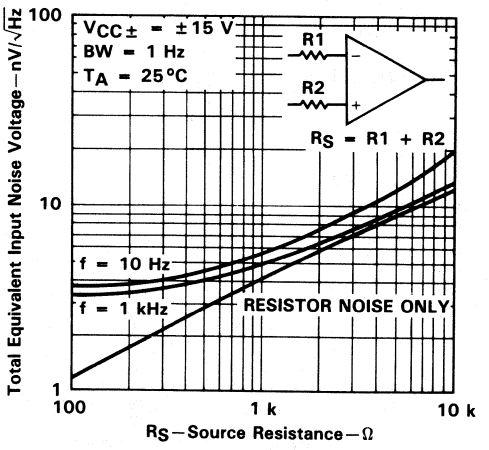


FIGURE 23

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
TOTAL SUPPLY VOLTAGE

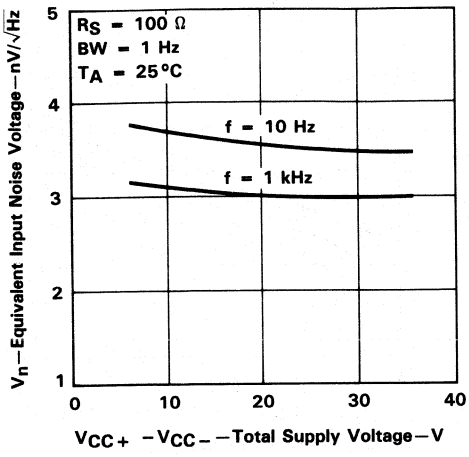


FIGURE 24

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREE-AIR TEMPERATURE

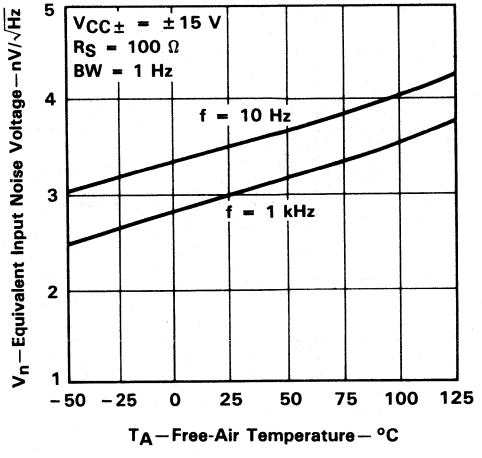


FIGURE 25

OP-27A, OP-27E, OP-37A, OP-37E
EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

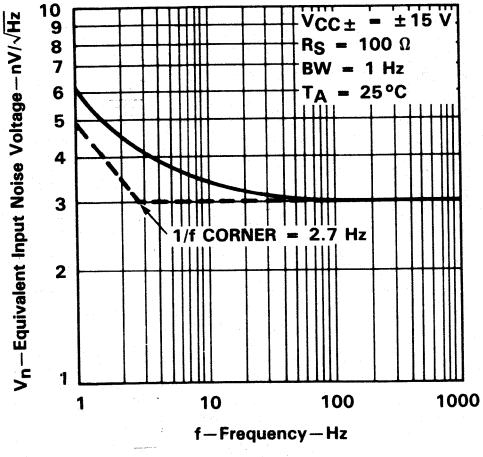


FIGURE 26

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

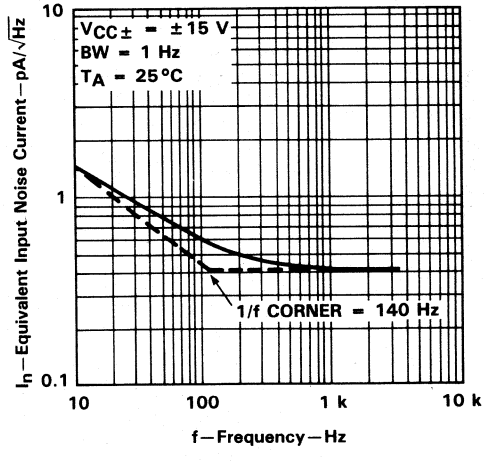


FIGURE 27

†Data for temperatures below –25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
ELAPSED TIME

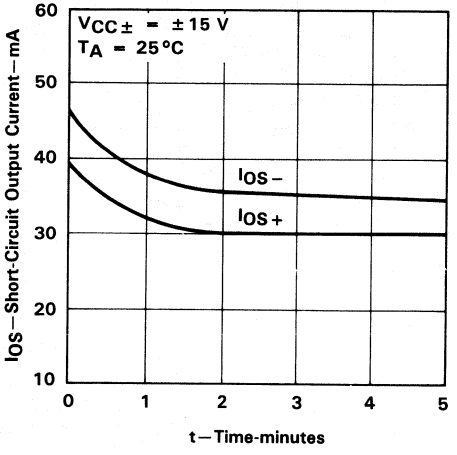


FIGURE 28

SUPPLY CURRENT
vs
TOTAL SUPPLY VOLTAGE

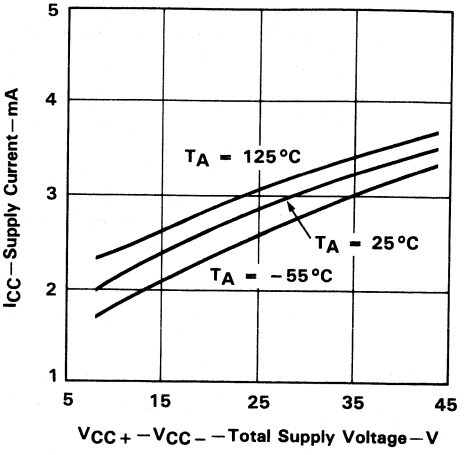


FIGURE 29

OP-27
VOLTAGE FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

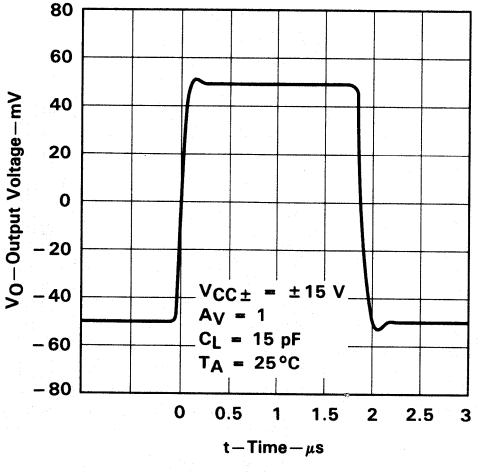


FIGURE 30

OP-27
VOLTAGE FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

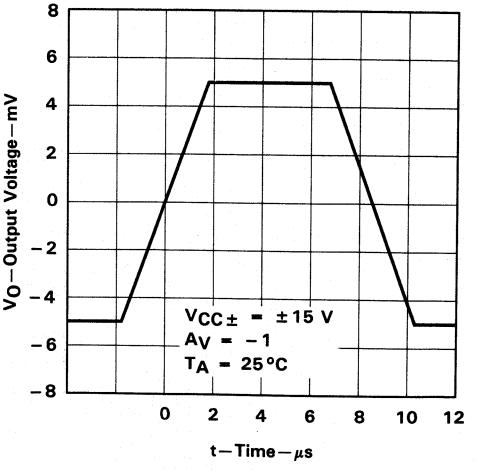


FIGURE 31

†Data for temperatures below −25°C and above 85°C are applicable to the OP-27A, OP-27C, OP-37A, and OP-37C only.

TYPICAL CHARACTERISTICS

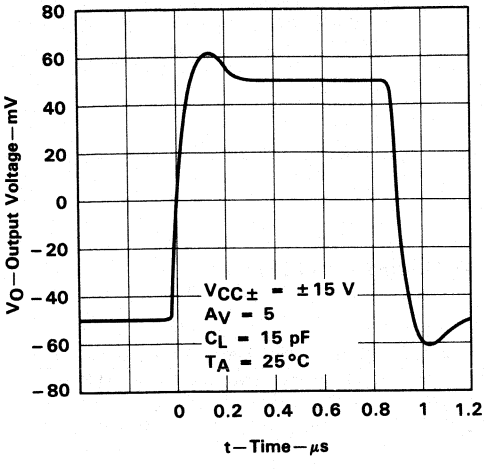


FIGURE 32

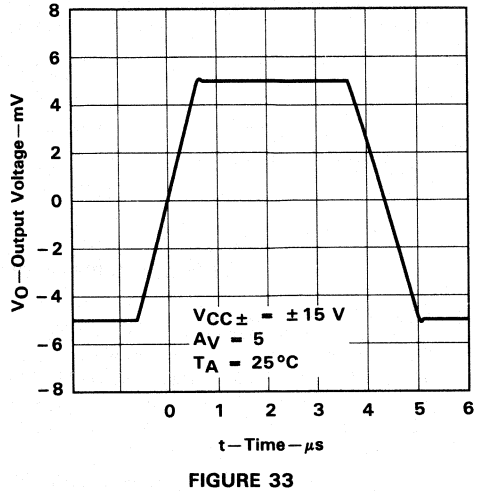


FIGURE 33

TYPICAL APPLICATION DATA

general

The OP-27 and OP-37 series devices may be inserted directly into OP-07, OP-05, μA725, and SE5534 sockets with or without removing external compensation or nulling components. In addition, the OP-27 and OP-37 may be fitted to μA741 sockets by removing or modifying external nulling components.

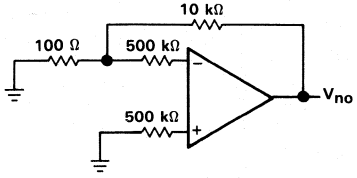
noise testing

Figure 34 shows a test curcuit for 0.1-Hz to 10-Hz peak-to-peak noise measurement of the OP-27 and OP-37. The frequency response of this noise tester indicates that the 0.1-Hz corner is defined by only one zero. Because the time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz, the test time to measure 0.1-Hz to 10-Hz noise should not exceed 10 seconds.

TYPICAL APPLICATION DATA

When measuring noise on a large number of units, a noise-voltage density test is recommended. A 10-Hz noise-voltage density measurement correlates well with a 0.1-Hz to 10-Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.

Figure 35 shows a circuit measuring current noise and the formula for calculating current noise.



$$I_n = \frac{[V_{no}^2 - (130\ nV)^2]^{1/2}}{1\ M\Omega \times 100}$$

FIGURE 35. CURRENT NOISE TEST CIRCUIT AND FORMULA

offset voltage adjustment

The input offset voltage and temperature coefficient of the OP-27 and OP-37 are permanently trimmed to a low level at wafer testing. However, if further adjustment of V_{IO} is necessary, using a 10-kΩ nulling potentiometer, as shown in Figure 36, does not degrade the temperature coefficient $\propto V_{IO}$. Trimming to a value other than zero creates an $\propto V_{IO}$ of $V_{IO}/300\ \mu V/°C$. For example, if V_{IO} is adjusted to 300 μV, the change in $\propto V_{IO}$ is 1 $\mu V/°C$.

The adjustment range with a 10-kΩ potentiometer is approximately ±2.5 mV. If a smaller adjustment range is needed, the sensitivity and resolution of the nulling can be inproved by using a smaller potentiometer in conjunction with fixed resistors. The example in Figure 37 has an approximate null range of ±200 μV.

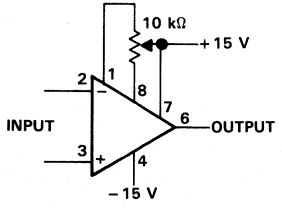


FIGURE 36. STANDARD INPUT OFFSET VOLTAGE ADJUSTMENT

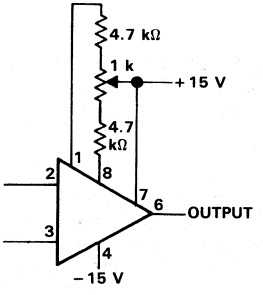


FIGURE 37. INPUT OFFSET VOLTAGE ADJUSTMENT WITH IMPROVED SENSITIVITY

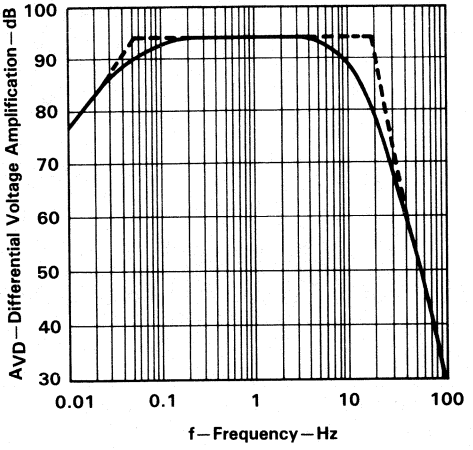
offset voltage and drift

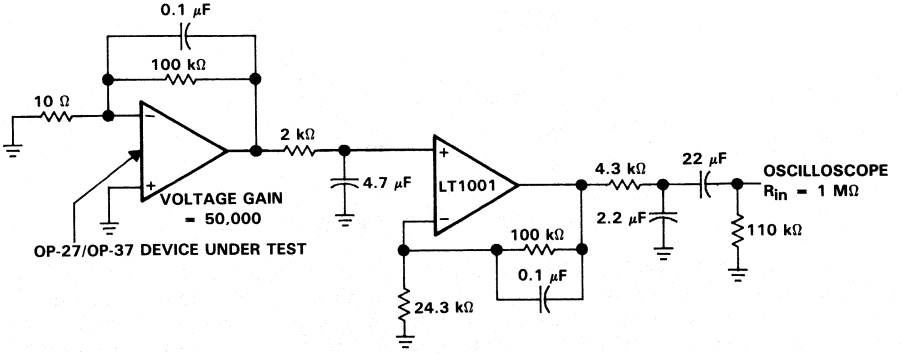
Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals can exceed the inherent temperature coefficient $\propto V_{IO}$ of the amplifier. Air currents should be minimized, package leads should be short, and the two input leads should be close together and at the same temperature.

The circuit shown in Figure 38 measures offset voltage. This circuit can also be used as the burn-in configuration for the OP-27 and OP-37, with the supply voltage increased to ±20 V, R1 = R3 = 10 kΩ, R2 = 200 Ω, and A_{VD} = 100.

TYPICAL APPLICATION DATA

noise testing (continued)





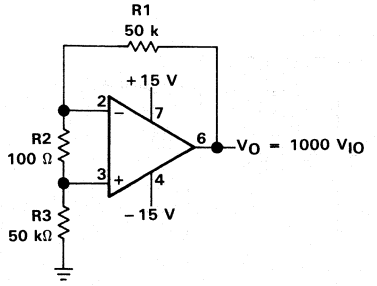
NOTE: All capacitor values are for non-polarized capacitors only.

FIGURE 34. 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE TEST CIRCUIT AND FREQUENCY RESPONSE

Measuring the typical 80-nV peak-to-peak noise performance of the OP-27 and OP-37 requires the following special test precautions:

1. The device should be warmed up for at least five minutes. As the operational amplifier warms up, the offset voltage typically changes 4 μV due to the chip temperature increasing from 10°C to 20°C starting from the moment the power supplies are turned on. In the 10-s measurement interval, these temperature-induced effects can easily exceed tens of nanovolts.
2. For similar reasons, the device should be well shielded from air currents to eliminate the possiblity of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.
3. Sudden motion in the vicinity of the device should be avoided, as it produces a feedthrough effect that increases observed noise.

TYPICAL APPLICATION DATA



NOTE: Resistors must have low thermoelectric potential.

FIGURE 38. TEST CIRCUIT FOR OFFSET VOLTAGE AND OFFSET VOLTAGE TEMPERATURE COEFFICIENT

unity gain buffer applications

The resulting output waveform when $R_f \leq 100\ \Omega$ and the input is driven with a fast large-signal pulse (> 1 V) is shown in the pulsed-operation diagram in Figure 39.

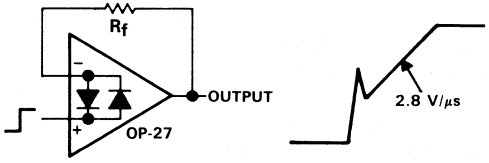
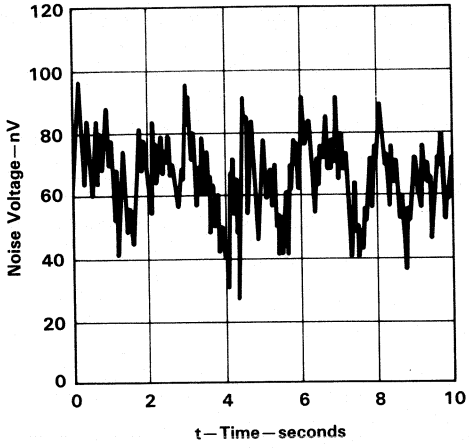
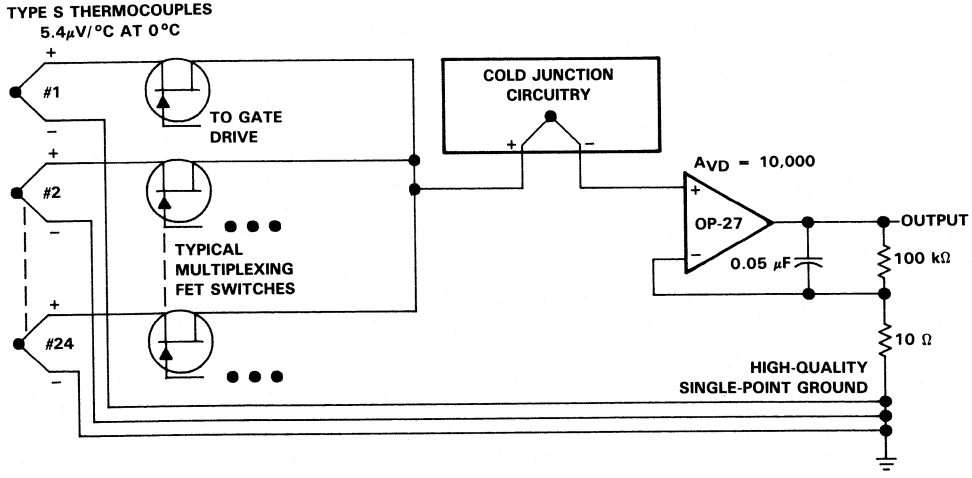


FIGURE 39. PULSED OPERATION

During the initial (fast-feedthrough-like) portion of the output waveform, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. When $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements (load current ≤ 20 mA at 10 V), the amplifier stays in its active mode, and a smooth transition occurs. When $R_f > 2\ k\Omega$, a pole is created with R_f and the amplifier's input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f eliminates this problem.

TYPICAL APPLICATION





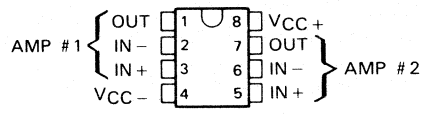
NOTE A: If 24 channels are multiplexed per second, and the output is required to settle to 0.1% accuracy, the amplifier's bandwidth cannot be limited to less than 30 Hz. The peak-to-peak noise contribution of the OP-27 will still be only 0.11 μV, which is equivalent to an error of only 0.02°C.

FIGURE 40. LOW-NOISE, MULTIPLEXED THERMOCOUPLE AMPLIFIER AND 0.1-Hz TO 10-Hz PEAK-TO-PEAK NOISE VOLTAGE

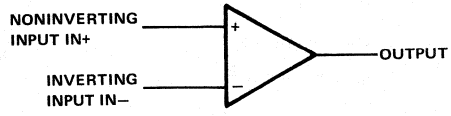
D2785, OCTOBER 1983—REVISED JUNE 1988

- Matched Gain and Offset Between Amplifiers
- Unity-Gain Bandwidth . . . 3 MHz Min
- Slew Rate . . . 1.5 V/ns Min
- Low Equivalent Input Noise Voltage . . . 2 $\mu V/\sqrt{Hz}$ Max (20 Hz to 20 kHz)
- No Frequency Compensation Required
- No Latch Up
- Wide Common-Mode Voltage Range
- Low Power Consumption
- Designed to be Interchangeable with Raytheon RC4559

D OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
RC4559	D,P	−0°C to 70°C	6 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e.,RC4559DR)

description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage V_{CC-} (see Note 1) . . . . . −18 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage (any input, see Notes 1 and 3) . . . . . ±15 V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4) . . . . . unlimited
Continuous total dissipation . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	25°C		2	6	mV
			0°C to 70°C			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	100	nA
			0°C to 70°C			200	
I_{IB}	Input bias current	V_O = 0	25°C		40	250	nA
			0°C to 70°C			500	
V_I	Input voltage range		25°C	±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L \geq 3\ k\Omega$	25°C	±12	±13		V
		R_L = 600 Ω	25°C	±9.5	±10		
		$R_L \geq 2\ k\Omega$	0°C to 70°C	±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	300		V/mV
			0°C to 70°C	15			
B_{OM}	Maximum output-swing bandwidth	V_{OPP} = 20 V, R_L = 2 kΩ	25°C	24	32		kHz
B_1	Unity-gain bandwidth		25°C	3	4		MHz
r_i	Input resistance		25°C	0.3	1		MΩ
CMRR	Common-mode rejection ratio	V_O = 0	25°C	80	100		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_O = 0	25°C		10	75	μV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 1 kΩ, f = 20 Hz to 20 kHz	25°C		1.4	2	μV
I_n	Equivalent input noise current	f = 20 Hz to 20 kHz	25°C		25		pA
I_{CC}	Supply current (both amplifiers)	No load, No signal	25°C		3.3	5.6	mA
			0°C		4	6.6	
			70°C		3	5	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, R_S = 1 kΩ, f = 10 kHz	25°C		90		dB
			25°C		90		

†All characteristics are specified under open-loop operation, unless otherwise noted.

matching characteristics at V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0		±0.2		mV
I_{IO}	Input offset current	V_O = 0		±7.5		nA
I_{IB}	Input bias current	V_O = 0		±15		nA
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ		±1		dB

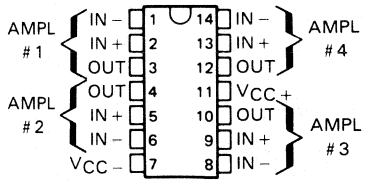
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		80		μs
	Overshoot			18%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF	1.5	2		V/μs

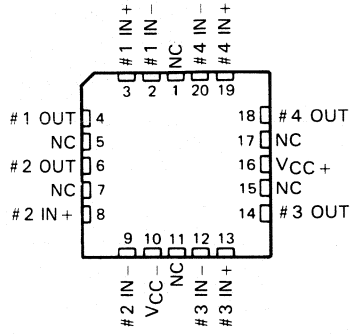
D2142, MARCH 1978—REVISED NOVEMBER 1988

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Designed to be Interchangeable with Raytheon RM4136, RV4136, and RC4136**
- **Low Noise . . . 8 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz**

RM4136 . . . J OR W PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGE
(TOP VIEW)



RM4136
FK CHIP CARRIER PACKAGE
(TOP VIEW)



NC—No internal connection

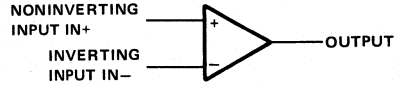
description

The RM4136, RV4136, and RC4136 are quad high-performance operational amplifiers with each amplifier electrically similar to the uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The RM4136 is characterized for operation over the full military temperature range of −55°C to 125°C, the RV4136 is characterized for operation from −40°C to 85°C, and the RC4136 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

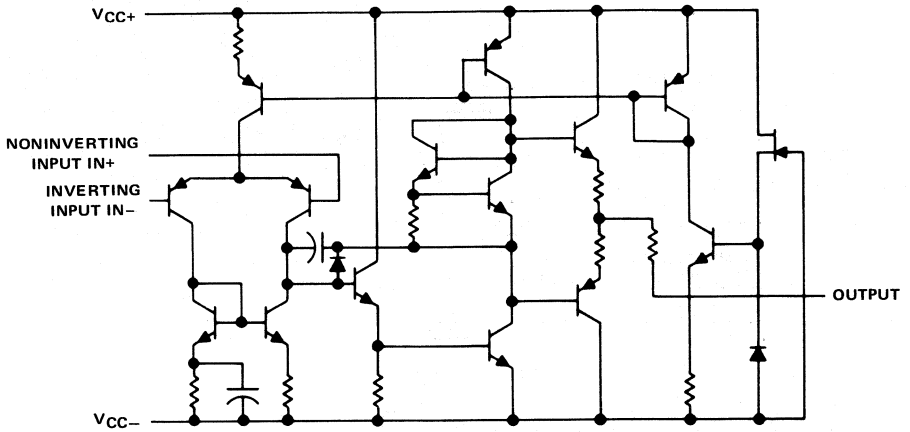


AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT (W)
0°C to 70°C	6 mV	RC4136D	–	RC4136J	RC4136N	–
−40°C to 85°C	6 mV	RV4136D	–	RV4136J	RV4136N	–
−55°C to 125°C	4 mV	–	RM4136FK	RM4136J	–	RM4136W

The D packages are available taped and reeled. Add the suffix R to the device type. (e.g., RC4136DR)

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		RM4136	RV4136	RC4136	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	800 mW	7.6 mW/°C	45°C	608 mW	494 mW	–
FK	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J (RM4136)	800 mW	11.0 mW/°C	77°C	800 mW	715 mW	275 mW
J (others)	800 mW	8.2 mW/°C	52°C	656 mW	533 mW	–
N	800 mW	9.2 mW/°C	63°C	736 mW	598 mW	–
W	800 mW	8.0 mW/°C	50°C	640 mW	520 mW	200 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		RM4136			RV4136			RC4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		0.5	4		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	150		5	200		5	200	nA
			Full range			500			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		140	400		140	500		140	500	nA
			Full range			1500			1500			800	
V_i	Input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		±12	±14		V
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		±10	±13		
		$R_L \geq$ 2 kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, $R_L \geq$ 2 kΩ	25°C	50	350		20	300		20	300		V/mV
			Full range	25			15			15			
B_1	Unity-gain bandwidth		25°C		3.5			3			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio	V_O = 0, R_S = 50 Ω	25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, BW = 1 Hz, f = 1 kHz, R_S = 100 Ω	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	V_O = 0, No load	25°C		5	11.3		5	11.3		5	11.3	mA
			MIN T_A		6	13.3		6	13.7		6	13.7	
			MAX T_A		4.5	10		4.5	10		4.5	10	
P_D	Total power dissipation (All four amplifiers)	V_O = 0, No load	25°C		150	340		150	340		150	340	mW
			MIN T_A		180	400		180	400		180	400	
			MAX T_A		135	300		135	300		135	300	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, f = 10 kHz, R_S = 1 kΩ	25°C		105			105			105		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for RM4136, −40°C to 85°C for RV4136, and 0°C to 70°C for RC4136.

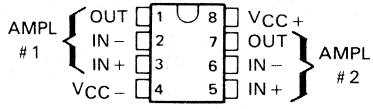
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		RM4136			RV4136, RC4136			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV,	R_L = 2 kΩ,		0.13			0.13		μs
	Overshoot factor	C_L = 100 pF			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V,	R_L = 2 kΩ,		1.7			1.7		V/μs
		C_L = 100 pF								

D2141, MARCH 1976—REVISED DECEMBER 1988

- **Continuous-Short-Circuit Protection**
- **Wide Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Unity Gain Bandwidth 3 MHz Typical**
- **Gain and Phase Match Between Amplifiers**
- **Low Noise . . . 8 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz**
- **Designed to be Interchangeable with Raytheon RM4558, RV4558, and RC4558**

D, JG, OR P PACKAGE
(TOP VIEW)



Description

The RM4558, RV4558, and RC4558 are dual general-purpose operational amplifiers with each half electrically similar to uA741 except that offset null capability is not provided.

The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

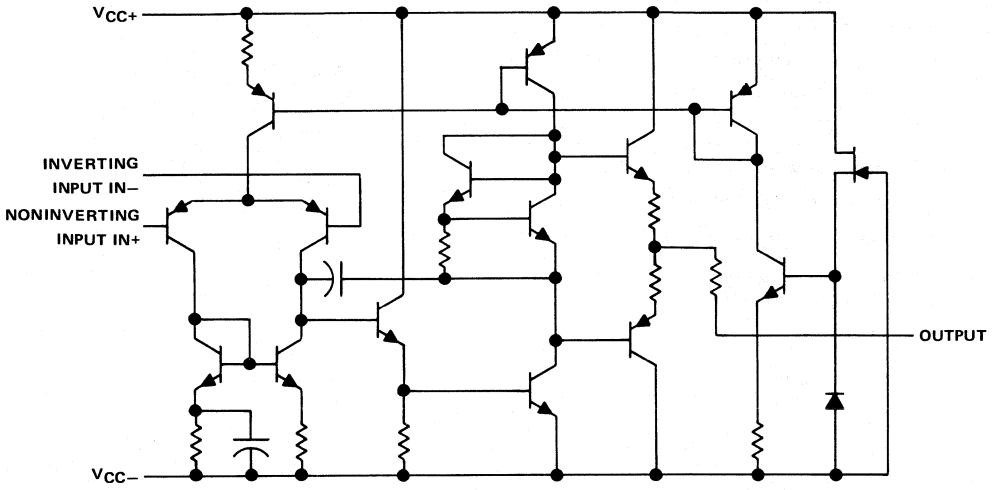
The RM4558 is characterized for operation over the full military temperature range of −55°C to 125°C, the RV4558 is characterized for operation from −40°C to 85°C, and the RC4558 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGES		
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	6 mV	RC4558D	RC4558JG	RC4558P
−40°C to 85°C	6 mV	RV4558D	RV4558JG	RV4558P
−55°C to 125°C	5 mV	—	RM4558JG	—

The D packages are available taped and reeled. Add the suffix "R" to the device type (e.g., RC4558DR).

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	RM4558	RV4558	RC4558	UNIT
Supply voltage V_{CC+} (see Note 1)	22	18	18	V
Supply voltage V_{CC-} (see Note 1)	−22	−18	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (any input, see Notes 1 and 3)	±15	±15	±15	V
Duration of output short-circuit to ground, one amplifier at a time (see Note 4)	unlimited	unlimited	unlimited	
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package		260	260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
JG (RM4558)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (RV4558) (RC4558)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

TEXAS INSTRUMENTS
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lectrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		RM4558			RV4558			RC4558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		0.5	5		0.5	6		0.5	6	mV
			Full range			6			7.5			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	200		5	200		5	200	nA
			Full range			500			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		140	500		140	500		150	500	nA
			Full range			1500			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±14		±12	±14		±12	±14		V
V_{OM}	Maximum output voltage swing	R_L = 10 kΩ	25°	±12	±14		±12	±14		±12	±14		V
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V	25°C	50	350		20	300		20	300		V/mV
			Full range	25			15			15			
B_1	Unity-gain bandwidth		25°C		2	3.5		3			3		MHz
r_i	Input resistance		25°C	0.3	5		0.3	5		0.3	5		MΩ
CMRR	Common-mode rejection ratio		25°C	70	90		70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±15 V to ±9 V	25°C		30	150		30	150		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, R_S = 100 Ω, f = 1 kHz, BW = 1 Hz	25°C		8			8			8		nV/√Hz
I_{CC}	Supply current (Both amplifiers)	No load, V_O = 0	25°C		2.5	5.6		2.5	5.6		2.5	5.6	mA
			MIN T_A		3	6.6		3	6.6		3	6.6	
			MAX T_A		2	5		2.3	5		2.3	5	
P_D	Total power dissipation (Both amplifiers)	No load, V_O = 0	25°C		75	170		75	170		75	170	mW
			MIN T_A		90	200		90	200		90	200	
			MAX T_A		60	150		70	150		70	150	
V_{o1}/V_{o2}	Crosstalk attenuation	Open loop	R_S = 1 kΩ, f = 10 kHz	25°C		85			85			85	dB
		A_{VD} = 100		25°C		105			105			105	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is −55°C to 125°C for RM4558, −40°C to 85°C for RV4558, and 0°C to 70°C for RC4558.

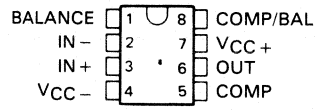
operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	RM4558			RV4558			RC4558			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF		0.13			0.13			0.13		ns
	Overshoot			5%			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF	1.1	1.7		1.1	1.7		1.1	1.7		V/μs

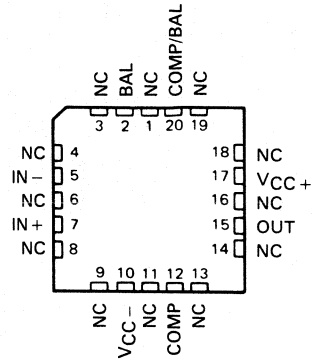
D2532, JULY 1979—REVISED MAY 1988

- Equivalent Input Noise Voltage 3.5 nV/$\sqrt{\text{Hz}}$ Typ
- Unity-Gain Bandwidth . . . . . 10 MHz Typ
- Common-Mode Rejection Ratio 100 dB Typ
- High DC Voltage Gain . . . . 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 32 V Typ with $V_{CC\pm}$ = ±18 V and R_L = 600 Ω
- High Slew Rate . . . . . 13 V/μs Typ
- Wide Supply Voltage Range ±3 V to ±20 V
- Low Harmonic Distortion
- Designed to be Interchangeable with Signetics SE5534, SE5534A, NE5534, and NE5534A

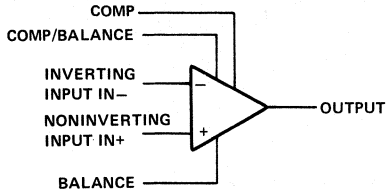
SE5534, SE5534A . . . JG PACKAGE
NE5534, NE5534A . . . D, JG OR P PACKAGE
(TOP VIEW)



SE5534, SE5534A
FK CHIP CARRIER PACKAGE
(TOP VIEW)



symbol



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	4 mV	NE5534D	—	NE5534JG	NE5534P
		NE5534AD	—	NE5534AJG	NE5534AP
−55°C to 125°C	2 mV	—	SE5534FK	SE5534JG	—
		—	SE5534AFK	SE5534AJG	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering (e.g., NE5534DR).

SE5534A FROM TI NOT RECOMMENDED FOR NEW DESIGNS

description

The SE5534, SE5534A, NE5534, and NE5534A are monolithic high-performance operational amplifiers combining excellent dc and ac characteristics. Some of the features include very low noise, high output drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, and high slew rate.

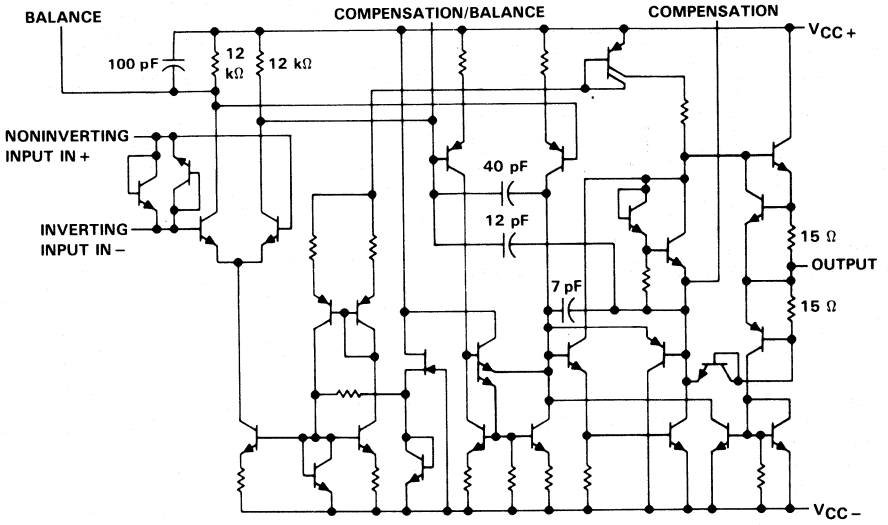
These operational amplifiers are internally compensated for a gain equal to or greater than three. Optimization of the frequency response for various applications can be obtained by use of an external compensation capacitor between pins 5 and 8. The devices feature input-protection diodes, output short-circuit protection, and offset-voltage nulling capability.

description (continued)

For the NE5534A, a maximum limit is specified for equivalent input noise voltage.

The SE5534 and SE5534A are characterized for operation over the full military temperature range of −55°C to 125°C; the NE5534 and NE5534A are characterized for operation from 0°C to 70°C.

schematic



All component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	22 V
Supply voltage, V_{CC-} (see Note 1)	−22 V
Input voltage either input (see Notes 1 and 2)	V_{CC+}
Input current (see Note 3)	±10 mA
Duration of output short-circuit (see Note 4)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: SE5534, SE5534A	−55°C to 125°C
NE5534, NE5534A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
3. Excessive current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs unless some limiting resistance is used.
4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	N/A
FK (see Note 5)	1375 mW	11.0 mW/°C	880 mW	275 mW
JG (SE5534__)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (NE5534__)	825 mW	6.6 mW/°C	528 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	N/A

NOTE 5: For the FK package, power rating and derating factor will vary with actual mounting technique used. The values stated here are believed to be conservative.

electrical characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SE5534, SE5534A			NE5534, NE5534A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		0.5	2		0.5	4	mV
			T_A = full range			3			5	
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		10	200		20	300	nA
			T_A = full range			500			400	
I_{IE}	Input bias current	$V_O = 0$	$T_A = 25°C$		400	800		500	1500	nA
			T_A = full range			1500			2000	
V_{ICR}	Common-mode input voltage range			±12	±13		±12	±13		V
V_{OPP}	Maximum peak-to-peak output voltage swing	$R_L \ge 600\ \Omega$	$V_{CC\pm} = \pm 15$ V	24	26		24	26		V
			$V_{CC\pm} = \pm 18$ V	30	32		30	32		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L \ge 600\ \Omega$	$T_A = 25°C$	50	100		25	100		V/mV
			T_A = full range	25			15			
A_{vd}	Small-signal differential voltage amplification	f = 10 kHz	$C_C = 0$		6			6		V/mV
			$C_C = 22$ pF		2.2			2.2		
B_{OM}	Maximum-output-swing bandwidth	$V_O = \pm 10$ V,	$C_C = 0$		200			200		kHz
		$V_O = \pm 10$ V,	$C_C = 22$ pF		95			95		
		$V_{CC\pm} = \pm 18$ V, $R_L = 600\ \Omega$,	$V_O = \pm 14$ V, $C_C = 22$ pF		70			70		
B_1	Unity-gain bandwidth	$C_C = 22$ pF,	$C_L = 100$ pF		10			10		MHz
r_i	Input resistance			50	100		30	100		kΩ
z_c	Output impedance	$A_{VD} = 30$ dB, $C_C = 22$ pF,	$R_L = 600\ \Omega$, f = 10 kHz		0.3			0.3		Ω
CMRR	Common-mode rejection ratio	$V_O = 0$, $R_S = 50\ \Omega$	$V_{IC} = V_{ICR}$ min,	80	100		70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC+} = \pm 9$ V to ± 15 V, $V_O = 0$,	$R_S = 50\ \Omega$	86	100		80	100		dB
I_{OS}	Output short-circuit current				38			38		mA
I_{CC}	Supply current	No load, $V_O = 0$	$T_A = 25°C$		4	6.5		4	8	mA
			T_A = full range			9				

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range is $T_A = -55°C$ to 125°C for SE5534 and SE5534A and 0°C to 70°C for NE5534 and NE5534A.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SE5534, NE5534			SE5534A, NE5534A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	C_C = 0		13			13		V/μs
		C_C = 22 pF		6			6		
t_r	Rise time	V_I = 50 mV, A_{VD} = 1, R_L = 600 Ω, C_C = 22 pF, C_L = 100 pF		20			20		ns
	Overshoot factor			20%			20%		
t_r	Rise time	V_I = 50 mV, A_{VD} = 1, R_L = 600 Ω, C_C = 47 pF, C_L = 500 pF		50			50		ns
	Overshoot factor			35%			35%		
V_n	Equivalent input noise voltage	f = 30 Hz		7			5.5	7	nV/√Hz
		f = 1 kHz		4			3.5	4.5	
I_n	Equivalent input noise current	f = 30 Hz		2.5			1.5		pA/√Hz
		f = 1 kHz		0.6			0.4		
F	Average noise figure	R_S = 5 kΩ, f = 10 Hz to 20 kHz					0.9		dB

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT BIAS CURRENT and INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

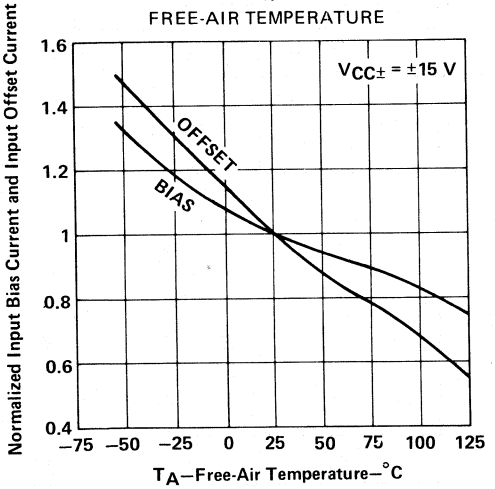


FIGURE 1

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

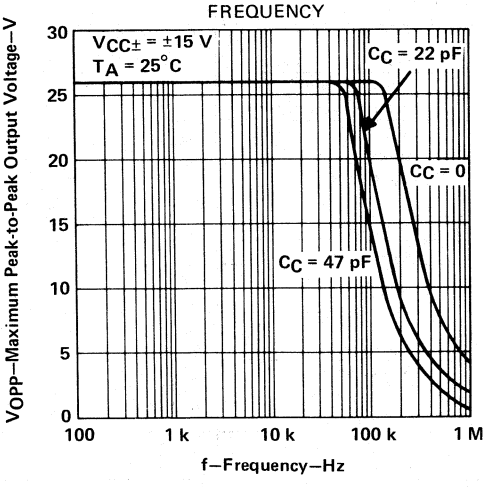


FIGURE 2

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

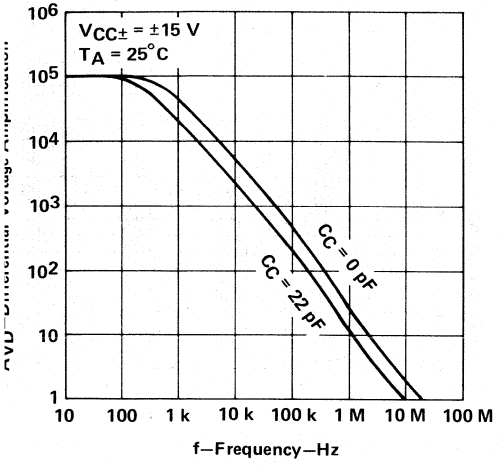


FIGURE 3

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

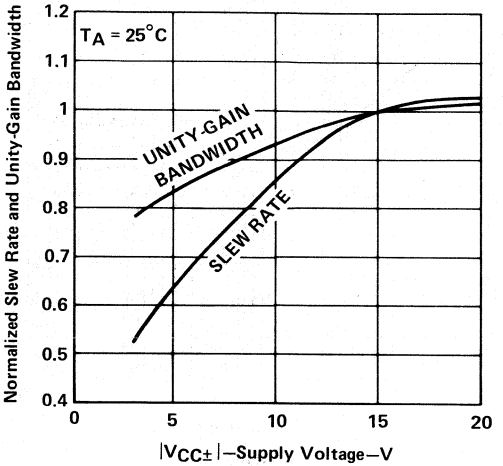


FIGURE 4

NORMALIZED SLEW RATE and
UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

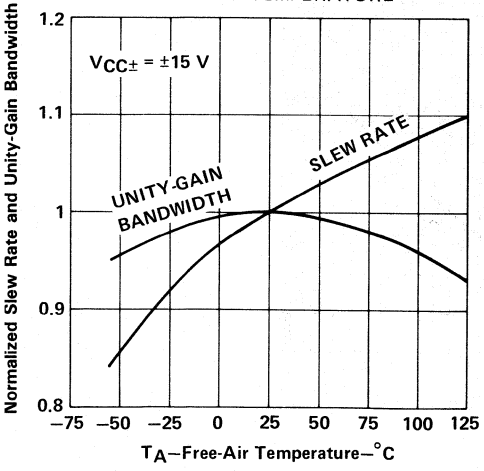


FIGURE 5

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

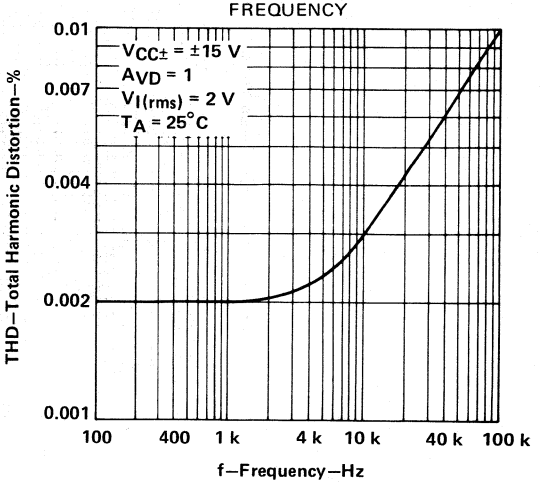


FIGURE 6

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

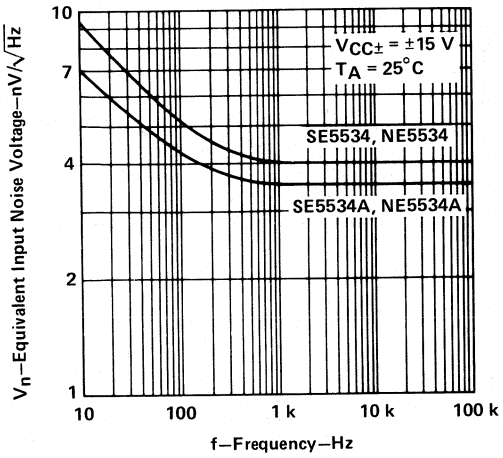


FIGURE 7

EQUIVALENT INPUT NOISE CURRENT
vs
FREQUENCY

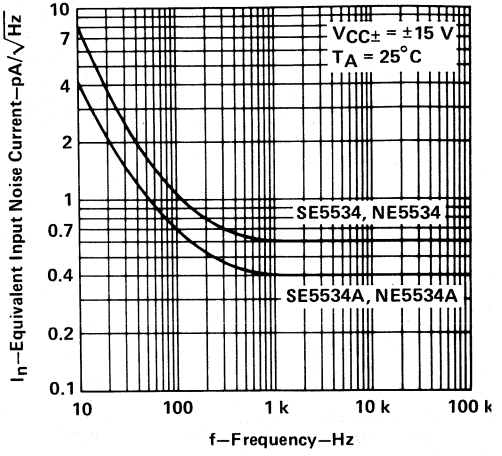


FIGURE 8

TOTAL EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

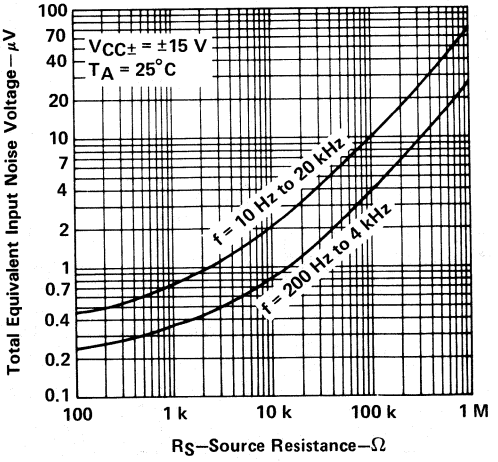


FIGURE 9

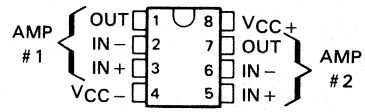
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D1661, SEPTEMBER 1973—REVISED JULY 1988

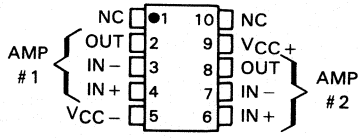
- **Very Low Power Consumption**
- **Power Dissipation with ±2-V Supplies . . . 170 μW Typ**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Popular Dual Op Amp Pin-Out**

TL022M IS NOT RECOMMENDED FOR NEW DESIGNS

TL022M . . . JG PACKAGE
TL022C . . . D, JG, OR P PACKAGE
(TOP VIEW)

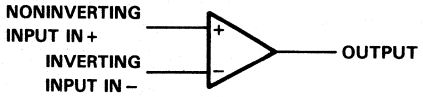


TL022M . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each amplifier)



escription

The TL022 is a dual low-power operational amplifier designed to replace higher power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use.

The TL022M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL022C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	CERAMIC FLAT PACK (U)
0°C to 70°C	5 mV	TL022CD	TL022CJG	TL022CP	—
−55°C to 125°C	5 mV	—	TL022MJG	—	TL022MU

The D package is available taped and reeled. Add the suffix R to the device type (i.e. TL022CDR)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL022M	TL022C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL022M only, the unlimited duration of the short-circui applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	–
JG (TL022M)	680 mW	8.4 mW/°C	69°C	672 mW	210 mW
JG (TL022C)	680 mW	6.6 mW/°C	47°C	528 mW	–
P	680 mW	8.0 mW/°C	65°C	640 mW	–
U	675 mW	5.4 mW/°C	25°C	432 mW	135 mW

lectrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	V_O = 0	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplication	R_L ≥ 10 kΩ, V_O = ±10 V	25°C	72	86		60	80		dB
			Full range	66			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, R_S = 50 Ω	25°C		30	150		30	200	μV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (both amplifiers)	No load, V_O = 0	25°C		130	250		130	250	μA
			Full range			250			250	
P_D	Total dissipation (both amplifiers)	No load, V_O = 0	25°C		3.9	6		3.9	7.5	mW
			Full range			6			7.5	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for TL022M is −55°C to 125°C and for TL022C is 0°C to 70°C.

ɔperating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL022M			TL022C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.3			0.3		μs
	Overshoot factor				5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

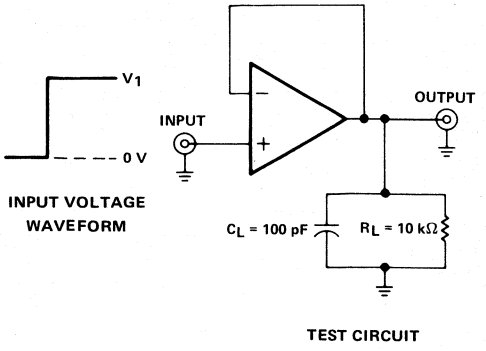


FIGURE 1. RISE TIME, OVERSHOOT FACTOR, AND SLEW RATE

TYPICAL CHARACTERISTICS

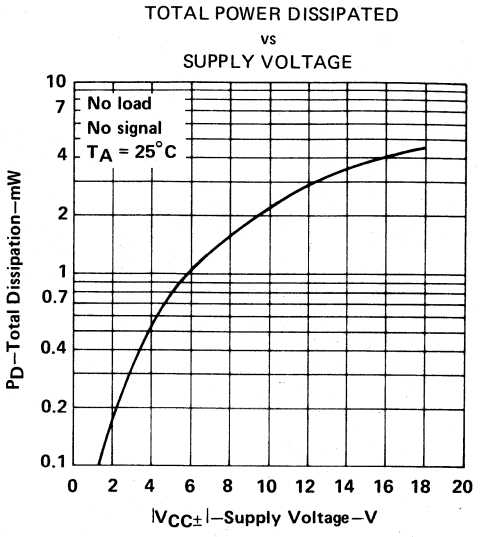
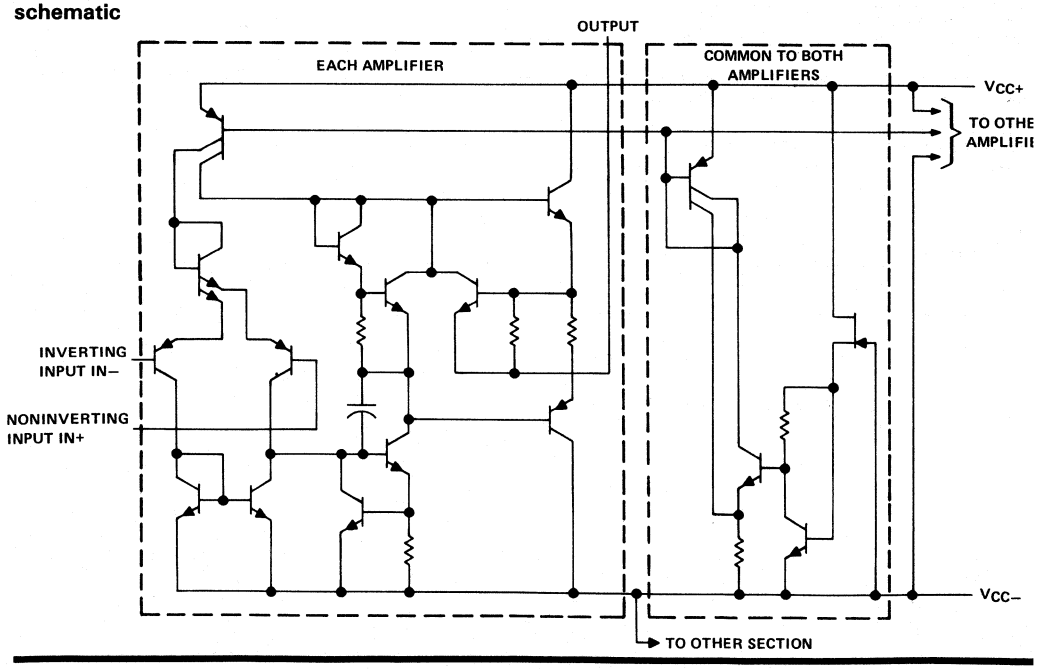


FIGURE 2

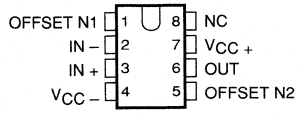
schematic



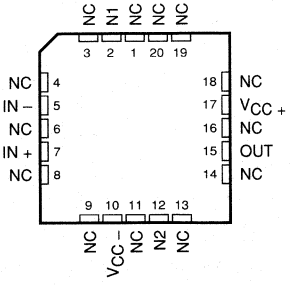
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 6.5 mW Typ**
- **Output Short-Circuit Protection**

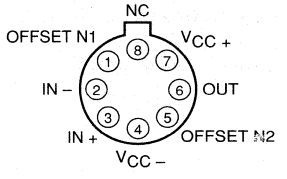
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

description

The TL031 and TL031A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

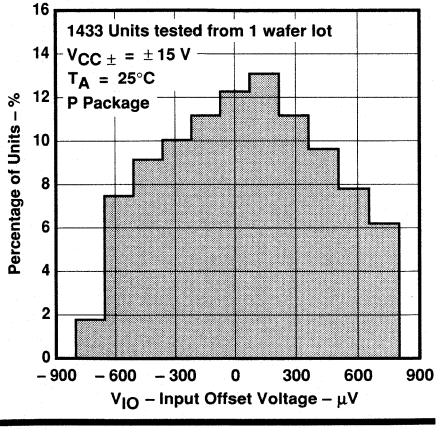
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL031 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL031 has been designed to be functionally compatible and pin compatible with the TL061.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	TL031ACD	—	TL031ACJG	TL031ACL	TL031ACP
	1.5 mV	TL031CD	—	TL031CJG	TL031CL	TL031CP
– 40°C to 85°C	0.8 mV	TL031AID	—	TL031AIJG	TL031AIL	TL031AIP
	1.5 mV	TL031ID	—	TL031IJG	TL031IL	TL031IP
– 55°C to 125°C	0.8 mV	TL031AMD	TL031AMFK	TL031AMJG	TL031AML	TL031AMP
	1.5 mV	TL031MD	TL031MFK	TL031MJG	TL031ML	TL031MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL031CDR).

DISTRIBUTION OF TL031A
INPUT OFFSET VOLTAGE



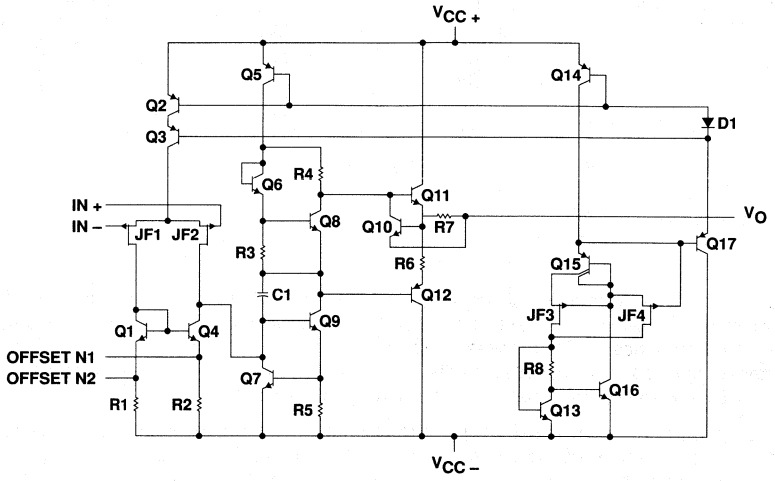
description (continued)

Two offset voltage grades are available: TL031 (1.5 mV max) and TL031A (800 μV max).

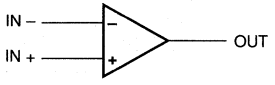
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic



symbol



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

ıbsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O . . . . . ± 40 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C

ıOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031M	25°C		0.54	3.5		0.5	1.5	mV
				Full range			6.5			4.5	
			TL031AM	25°C		0.41	2.8		0.34	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL031M	25°C to 125°C		5.1			4.3		µV/°C
			TL031AM	25°C to 125°C		5.1			4.3		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation	No load, V_O = 0		25°C		1.9	2.5		6.5	8.4	mW
				−55°C		1.1	2.5		4.7	8.4	
				125°C		1.8	2.5		5.8	8.4	
I_{CC}	Supply current	No load, V_O = 0		25°C		192	250		217	280	µA
				−55°C		114	250		156	280	
				125°C		178	250		197	280	

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2.0		2	2.9		V/μs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR−	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/μs
					−55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL031M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AM		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 7: For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL031I	25°C to 85°C		6.5			6.2		μV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation	No load, V_O = 0		25°C		1.9	2.5		6.5	8.4	mW
				−40°C		1.4	2.5		5.4	8.4	
				85°C		1.9	2.5		6.2	8.4	
I_{CC}	Supply current	No load, V_O = 0		25°C		192	250		217	280	μA
				−40°C		144	250		181	280	
				85°C		189	250		207	280	

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

8. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2.0		2	2.9		V/μs
					−40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
$SR-$	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					−40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL031I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AI		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation	No load, V_O = 0		25°C		1.9	2.5		6.5	8.4	mW
				0°C		1.8	2.5		6.3	8.4	
				70°C		1.9	2.5		6.3	8.4	
I_{CC}	Supply current	No load, V_O = 0		25°C		192	250		217	280	µA
				0°C		184	250		211	280	
				70°C		189	250		210	280	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

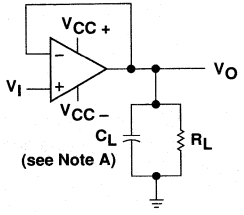
8. This parameter is tested on a sample basis for the TL031A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2			2.9		V/μs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
$SR-$	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					0°C		3.7		3.2	5.0		
					70°C		4.0		3.2	5.0		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL031C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		61			61		nV/√Hz
				f = 1 kHz			41			41		
		TL031AC		f = 10 Hz	25°C		61			61		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

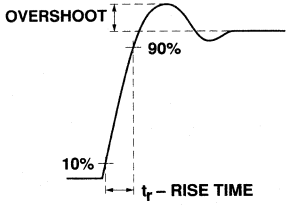


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

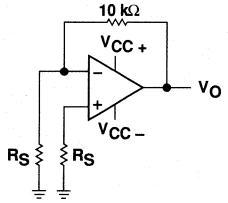
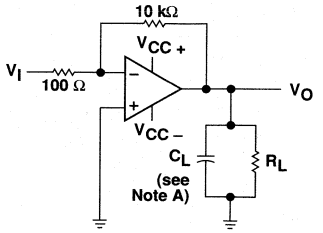


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

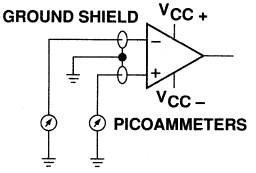


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL031 and TL031A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE

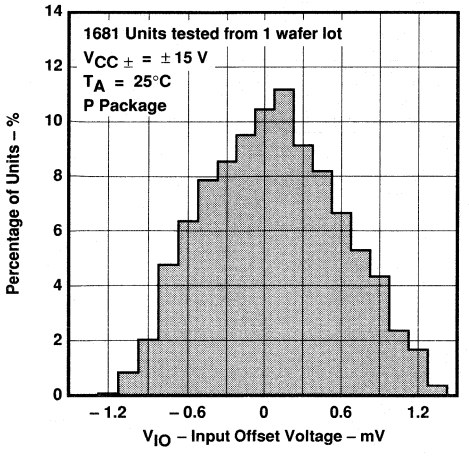


FIGURE 6

DISTRIBUTION OF TL031
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

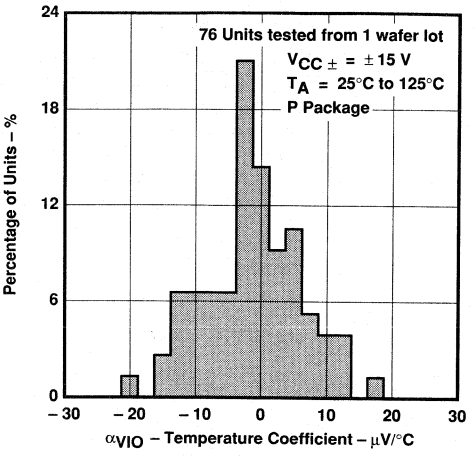


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

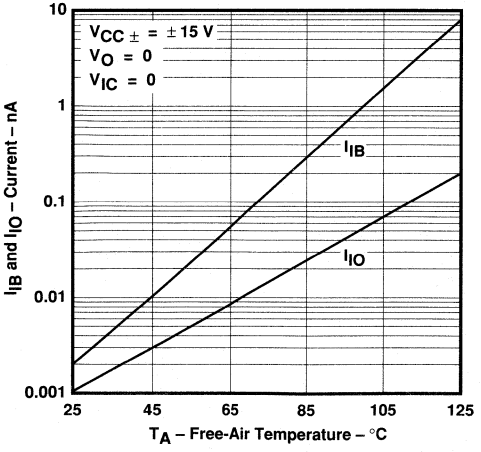


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

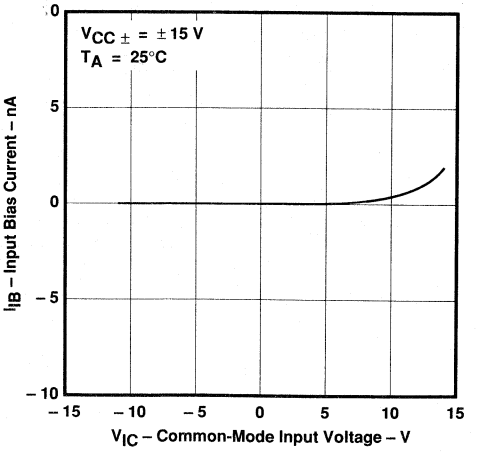


FIGURE 9

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TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

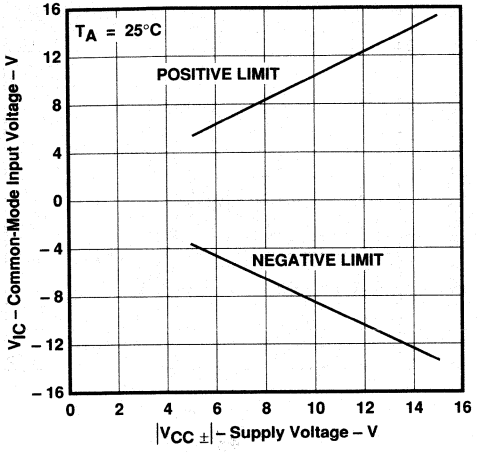

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

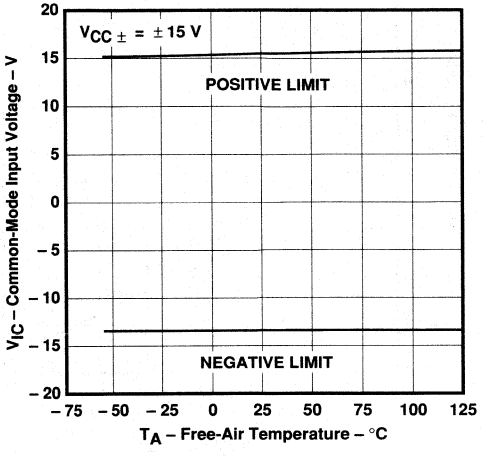

FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

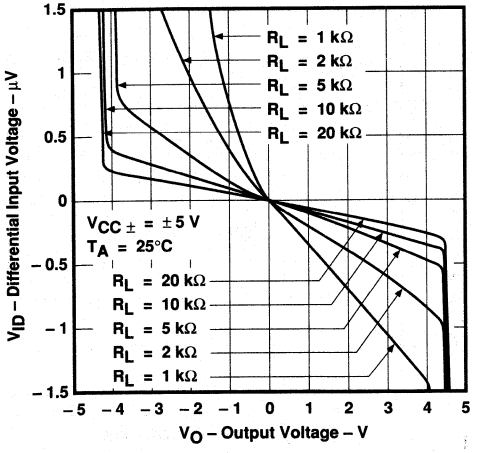

FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

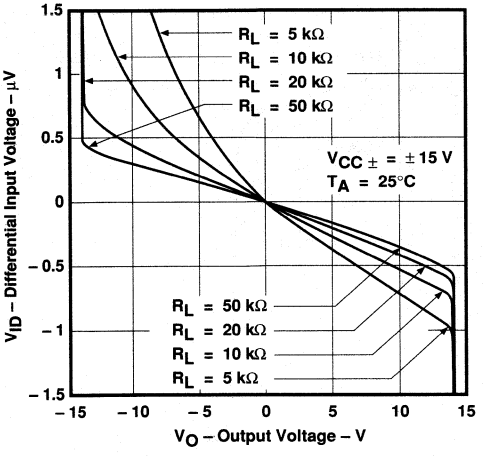

FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

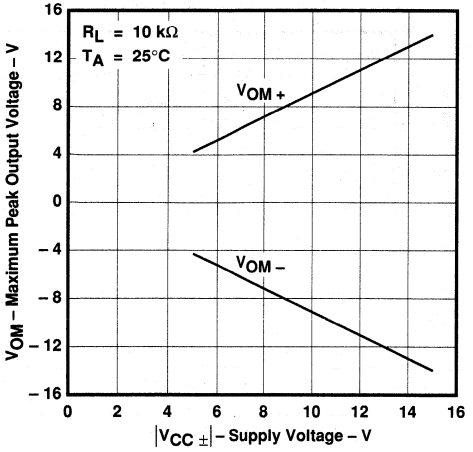

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

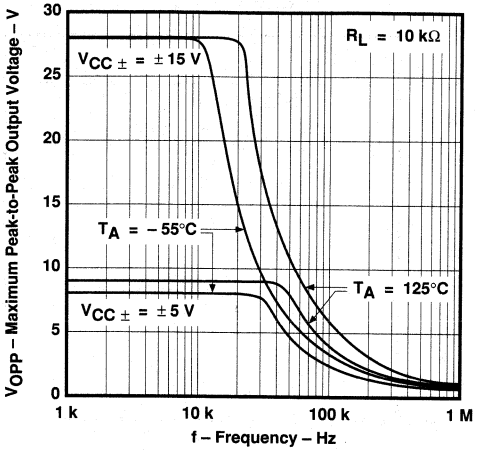

FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

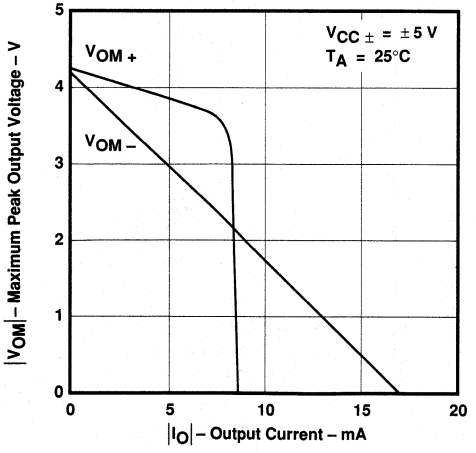

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

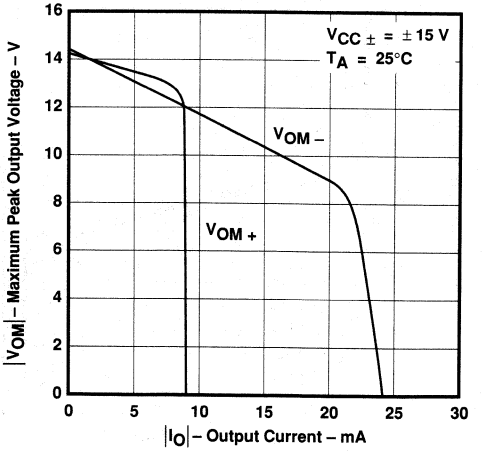

FIGURE 17

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

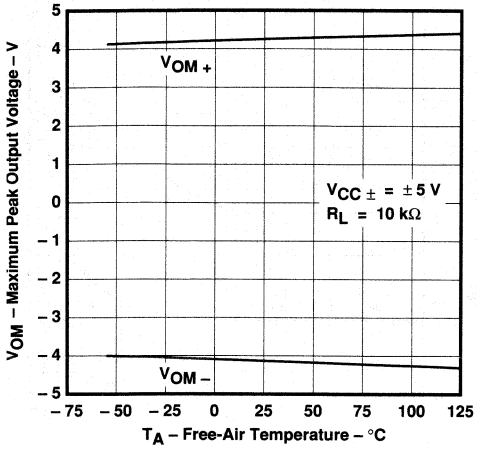

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

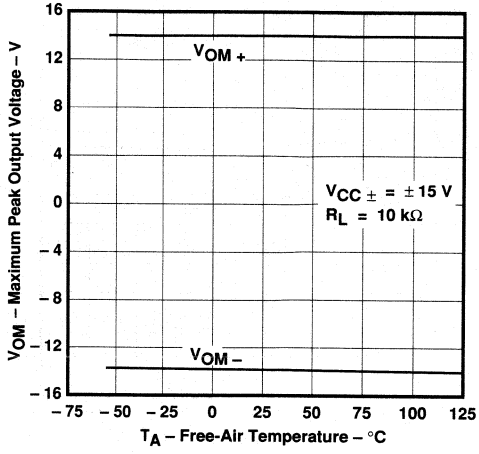

FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

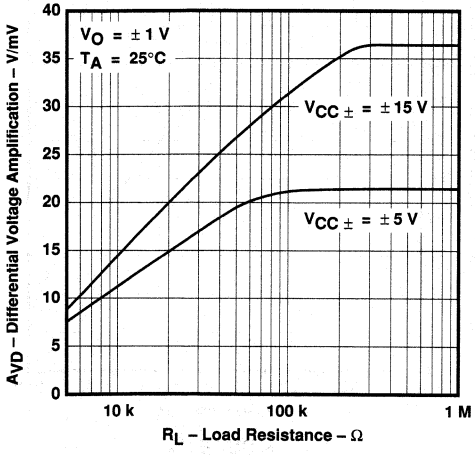

FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

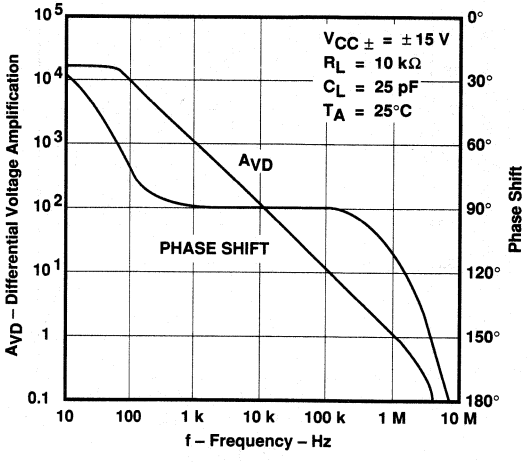

FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

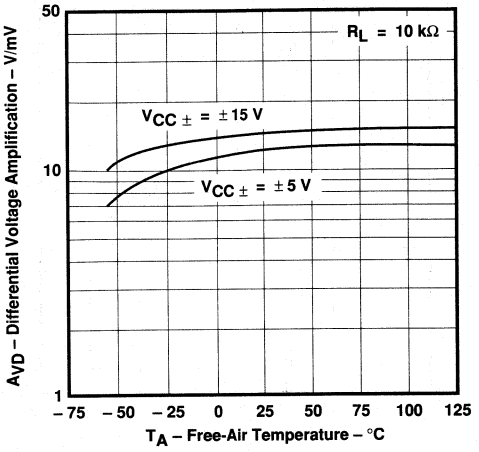

FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

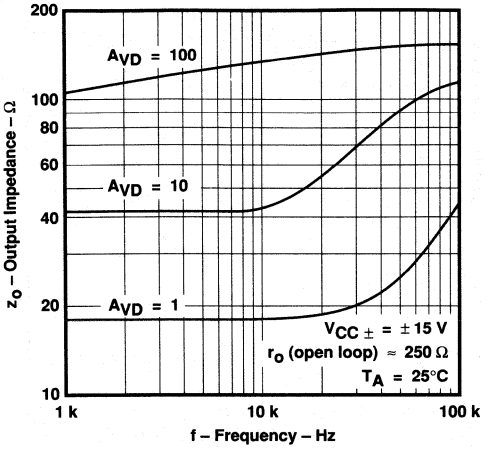

FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

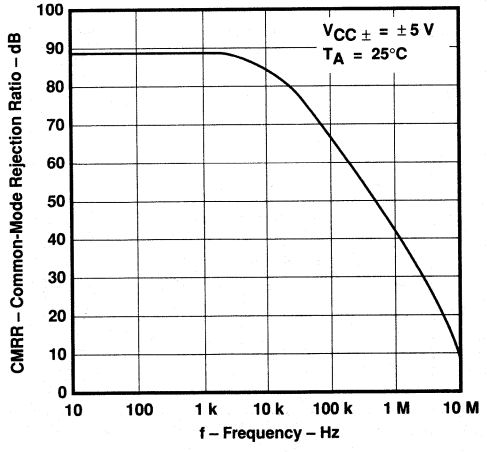

FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

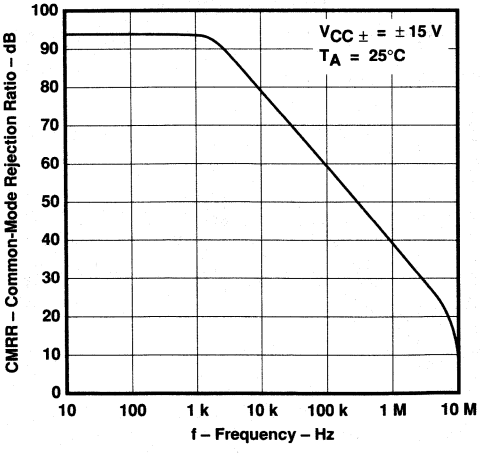

FIGURE 25

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TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

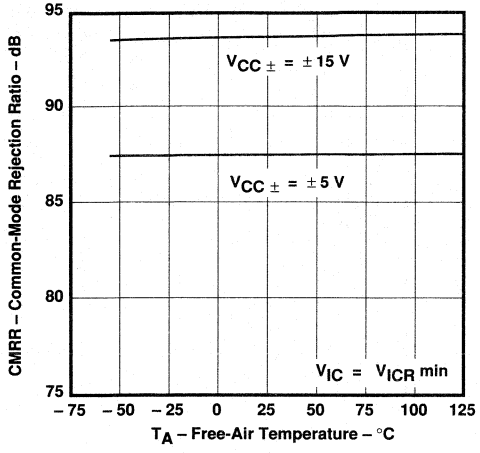

FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

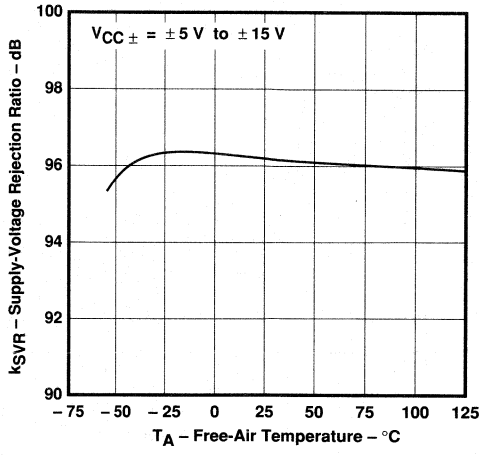

FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

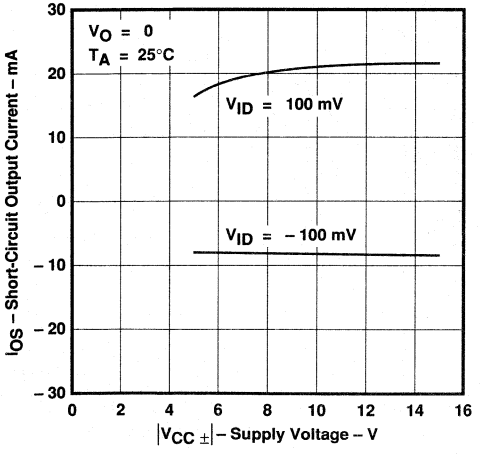

FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

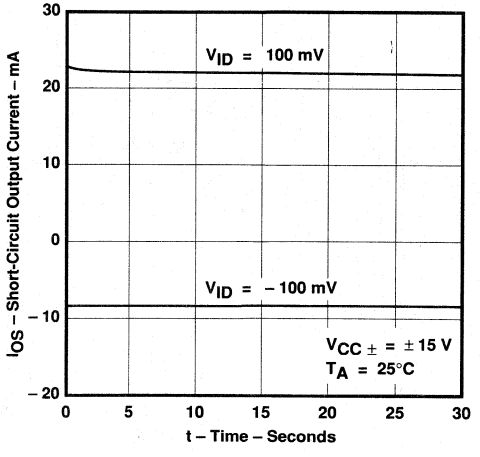

FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

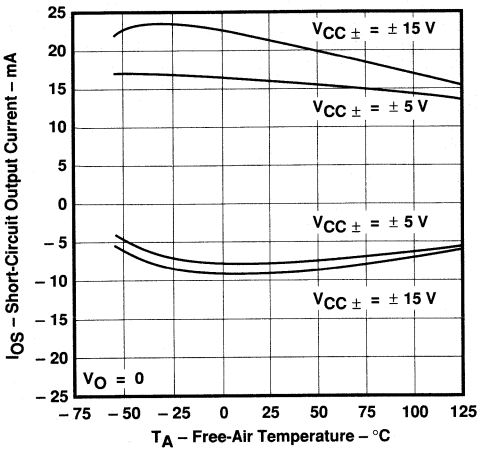

FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

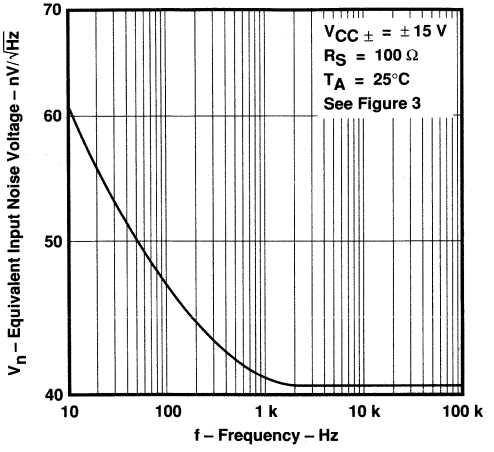

FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

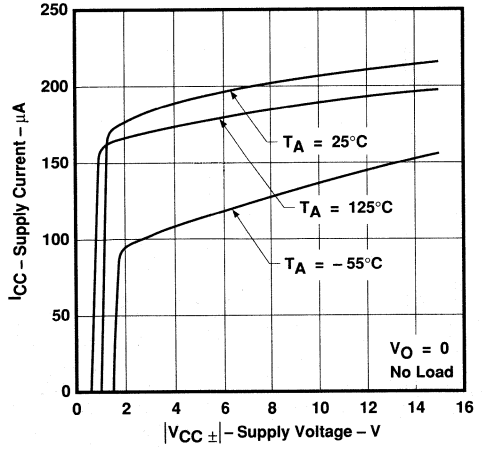

FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

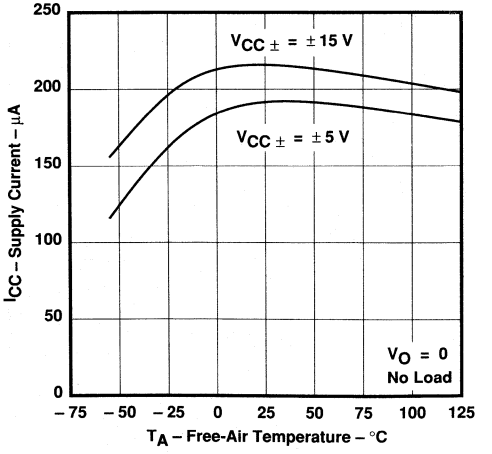

FIGURE 33

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

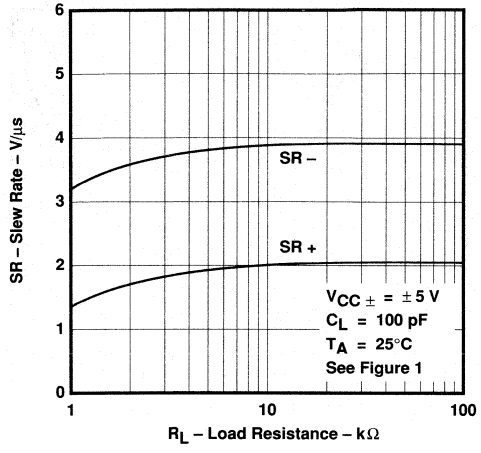

FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

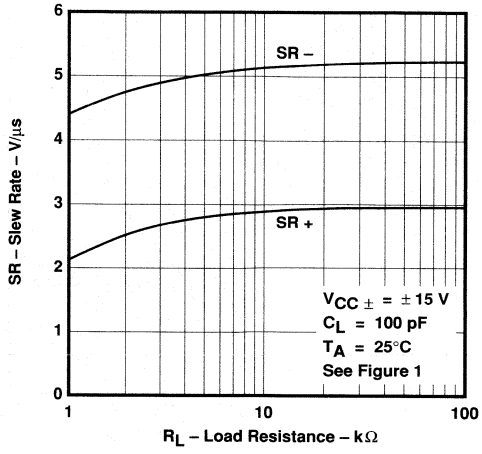

FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

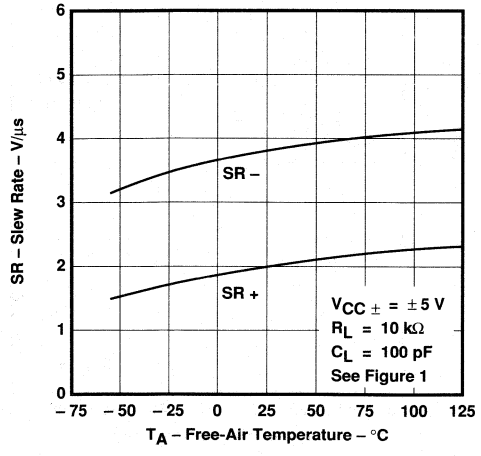

FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

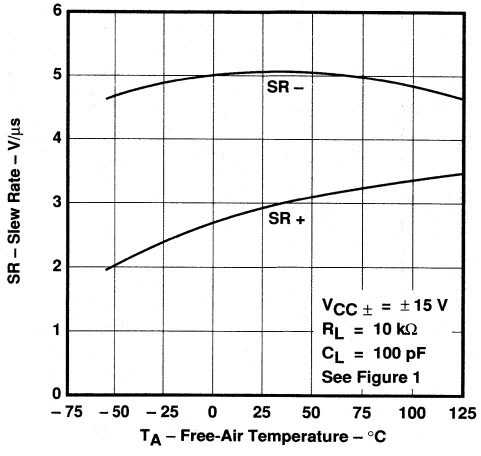

FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

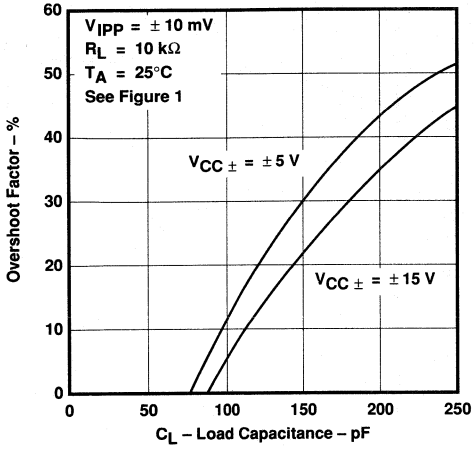

FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

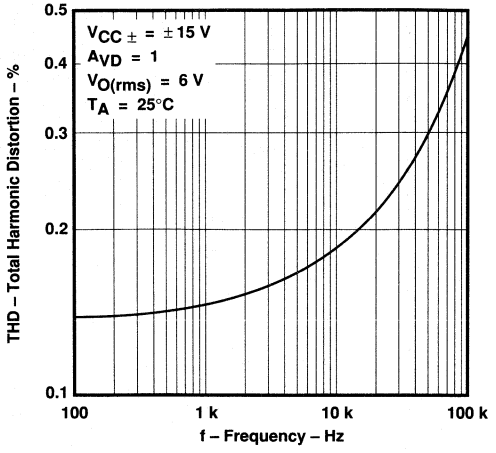

FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

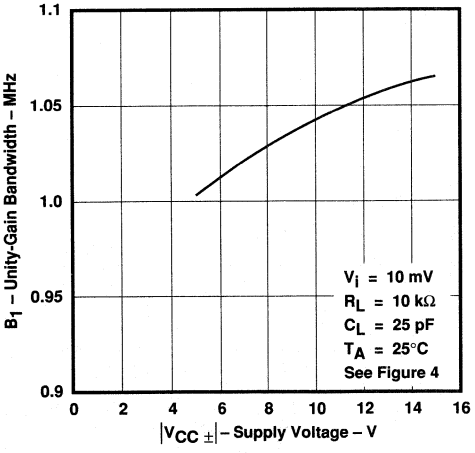

FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

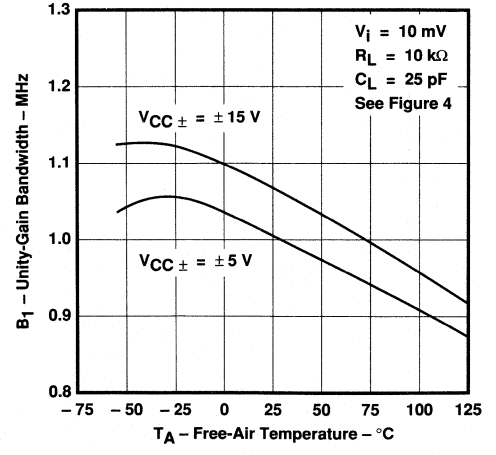

FIGURE 41

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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

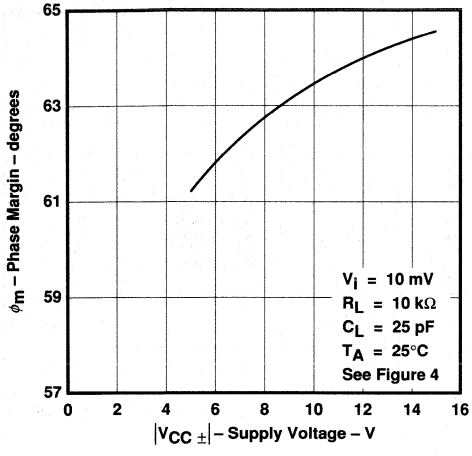


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

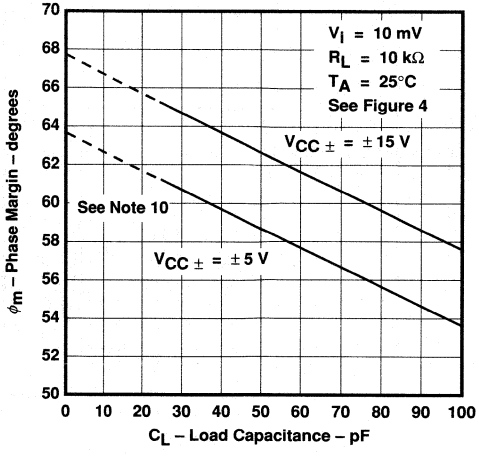


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

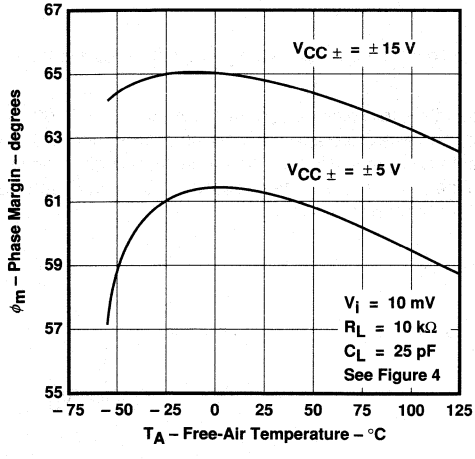


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

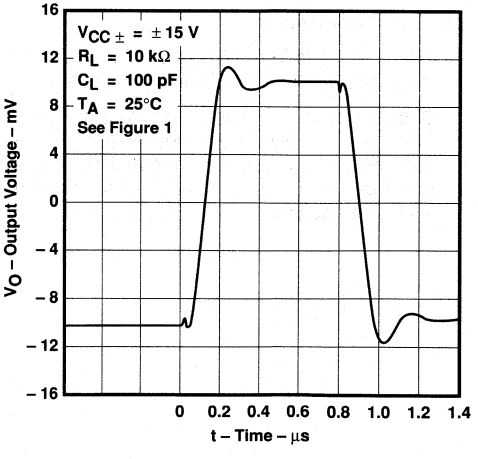


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

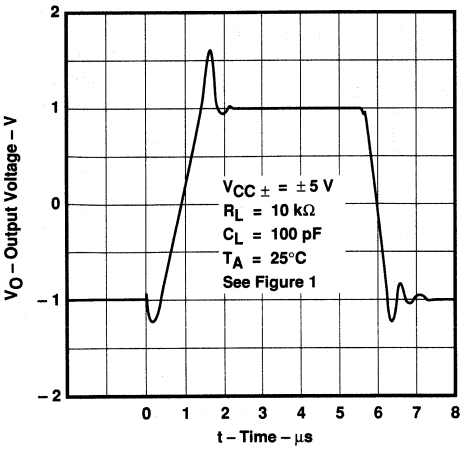


FIGURE 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

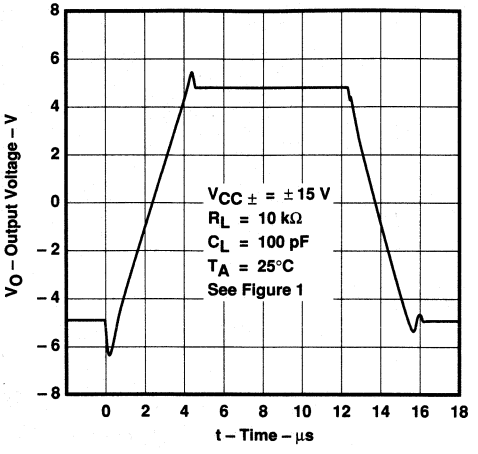


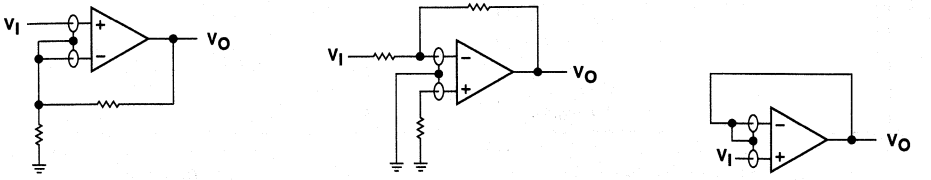
FIGURE 47

TYPICAL APPLICATION DATA

input characteristics

The TL031 and TL031A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL031 and TL031A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



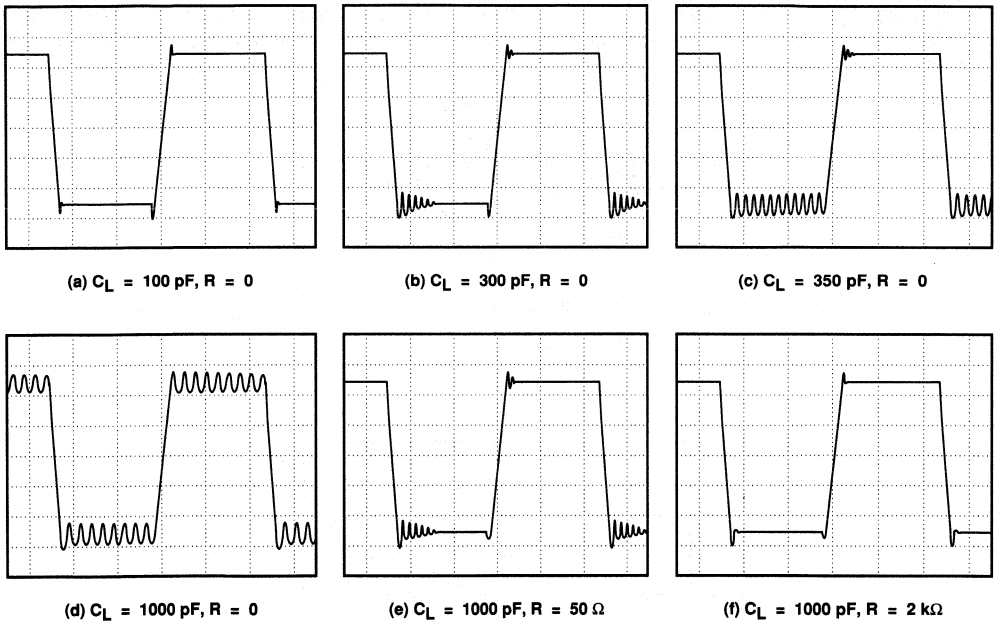
(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 48. USE OF GUARD RINGS

TYPICAL APPLICATION DATA

›utput characteristics

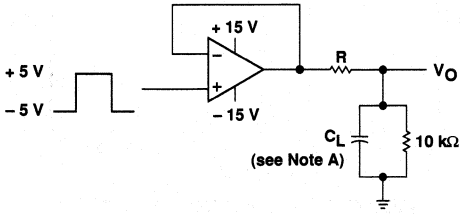
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL031 and TL031A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

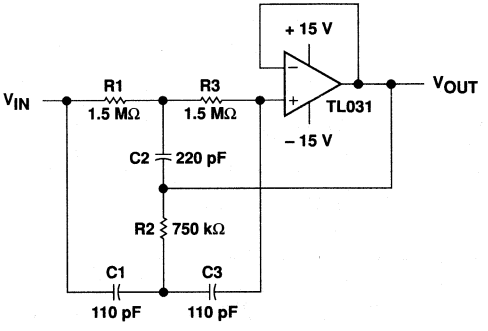
TYPICAL APPLICATION DATA

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. The circuit ir Figure 51 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1 C1}$$

With the resistors and capacitors shown in Figure 51, the center frequency is 1 kHz. Note tha $C1 = C3 = C2 \div 2$ and also that $R1 = R3 = 2 \times R2$. The center frequency can be modified by varying these values. When adjusting the center frequency, be sure that the operational amplifier still has sufficien gain at the frequency of interest.



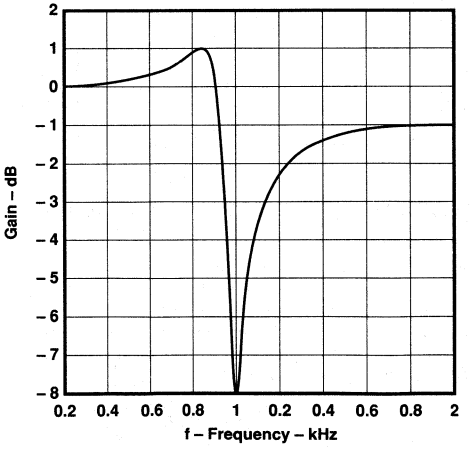


FIGURE 51. HIGH-Q NOTCH FILTER

TYPICAL APPLICATION DATA

transimpedance amplifier

The low-power precision TL031 allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL031A greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves ten-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F \left(\frac{R1 + R2}{R2}\right)$$

Using the resistor values shown in the schematic, for a 1-nA input current, the output voltage equals – 0.1 V. If the V_O limit for the TL031A is measured to be ± 12 V, the maximum input current for these resistor values is ± 120 nA. Similarly, one LSB on a ten-bit scale corresponds to 12 mV of output voltage or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = -\left[V_{IO} + R_F(I_{IN} + I_{IB})\right]\left(\frac{R1 + R2}{R2}\right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL031A inputs as shown in Figuire 52.

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

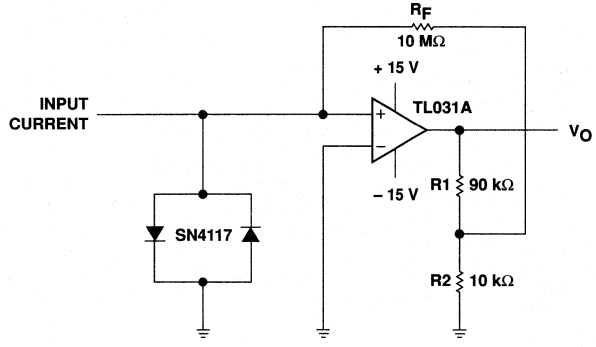


FIGURE 52. TRANSIMPEDANCE AMPLIFIER

TYPICAL APPLICATION DATA

4- to 20-mA current loops

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 53 requires three wires from the transmitting to receiving circuitry while the second variation in Figure 54 requires only two wires but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL031A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL031A is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\ V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\ mA$$

The circuits presently provide 4-to 20-mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL031A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\ V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\ mA - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA..

Thanks to the low power consumption of the TL031A, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

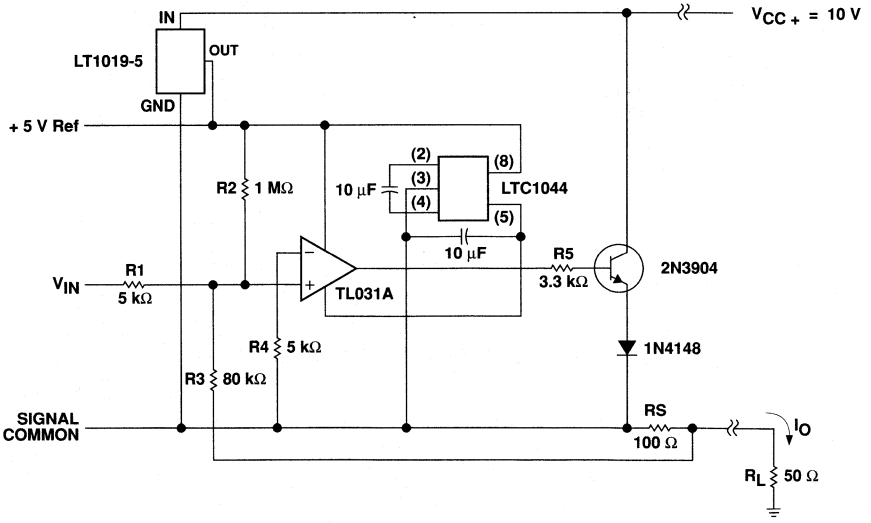


FIGURE 53. 2-WIRE 4- TO 20-mA CURRENT LOOP

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TYPICAL APPLICATION DATA

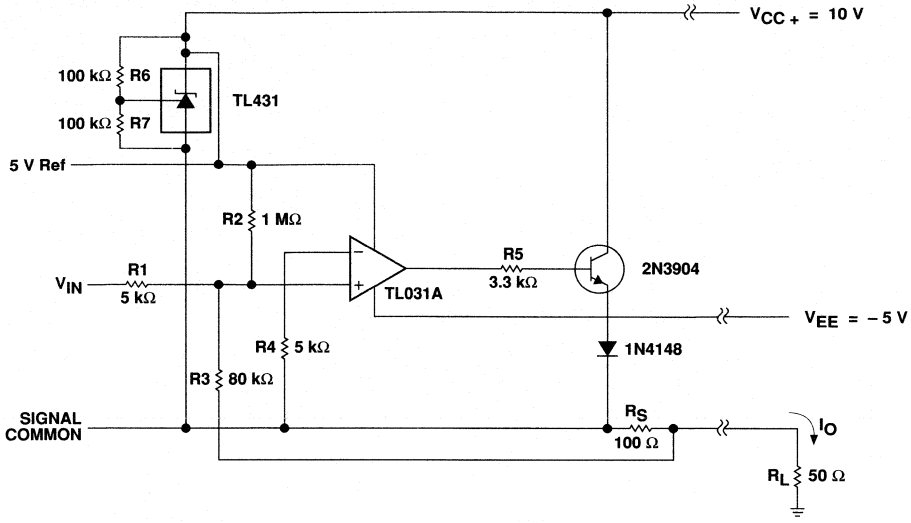
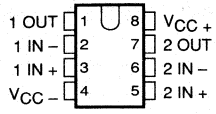


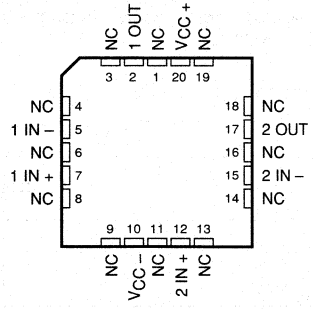
FIGURE 54. 3-WIRE 4- TO 20-mA CURRENT LOOP

- **Maximum Offset Voltage . . . 800 μV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 13 mW Typ**
- **Output Short-Circuit Protection**

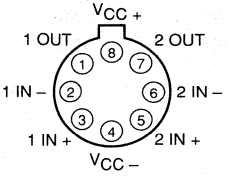
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case

NC – No internal connection

escription

The TL032 and TL032A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

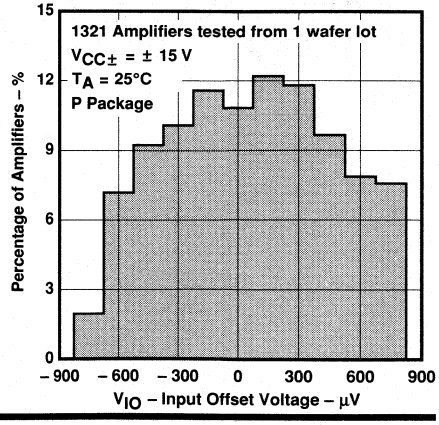
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low power consumption make the TL032 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL032 has been designed to be

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	0.8 mV	TL032ACD	—	TL032ACJG	TL032ACL	TL032ACP
	1.5 mV	TL032CD	—	TL032CJG	TL032CL	TL032CP
– 40°C to 85°C	0.8 mV	TL032AID	—	TL032AIJG	TL032AIL	TL032AIP
	1.5 mV	TL032ID	—	TL032IJG	TL032IL	TL032IP
– 55°C to 125°C	0.8 mV	TL032AMD	TL032AMFK	TL032AMJG	TL032AML	TL032AMP
	1.5 mV	TL032MD	TL032MFK	TL032MJG	TL032ML	TL032MP

packages are available taped-and-reeled. Add "R" suffix to device type when rdering (e.g., TL032CDR).

DISTRIBUTION OF TL032A
INPUT OFFSET VOLTAGE



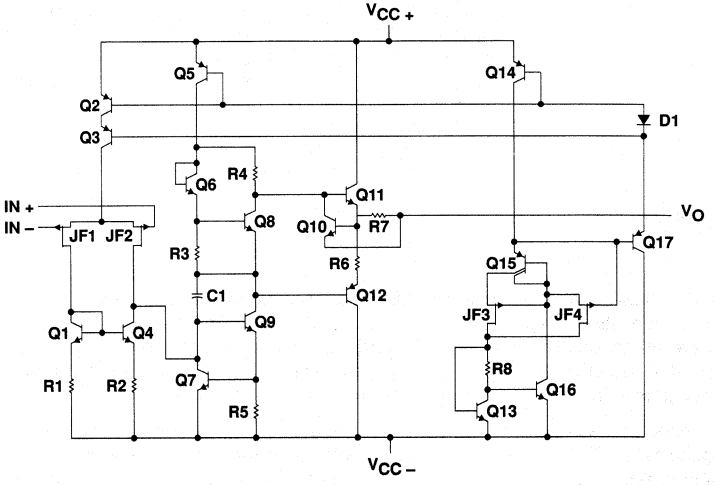
description (continued)

functionally compatible and pin compatible with the TL062. Two offset voltage grades are available: TL032 (1.5 mV max) and TL032A (800 μV max).

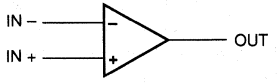
A variety of available packaging options includes small-outline and chip carrier versions for high densit system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C t 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices ar characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



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bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O (each output) . . . . . ± 40 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			± 5	± 15		± 5	± 15		± 5	± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm} = \pm 15$ V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL032M	25°C		0.69	3.5		0.57	1.5	mV
				Full range			6.5			4.5	
			TL032AM	25°C		0.53	2.8		0.39	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL032M	25°C to 125°C		9.7			9.7		μV/°C
			TL032AM	25°C to 125°C		9.7			9.7		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, V_O = 0		25°C		3.8	5		13	17	mW
				−55°C		2.3	5		9.4	17	
				125°C		3.6	5		11.8	17	
I_{CC}	Supply current (two amplifiers)	No load, V_O = 0		25°C		384	500		434	560	μA
				−55°C		228	500		312	560	
				125°C		356	500		394	560	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

›perating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
$SR-$	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/μs
					−55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL032M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AM		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 7: For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032I	25°C to 85°C		11.4			10.8		μV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, V_O = 0		25°C		3.8	5		13	17	mW
				−40°C		2.9	5		10.9	17	
				85°C		3.7	5		12.4	17	
I_{CC}	Supply current (two amplifiers)	No load, V_O = 0		25°C		384	500		434	560	μA
				−40°C		288	500		362	560	
				85°C		372	500		414	560	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					−40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
SR−	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					−40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL032I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AI		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL032C	25°C to 70°C		11.5			10.8		μV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (two amplifiers)	No load, V_O = 0		25°C		3.8	5		13	17	mW
				0°C		3.7	5		12.7	17	
				70°C		3.8	5		12.6	17	
I_{CC}	Supply current (two amplifiers)	No load, V_O = 0		25°C		384	500		434	560	μA
				0°C		368	500		422	560	
				70°C		378	500		420	560	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

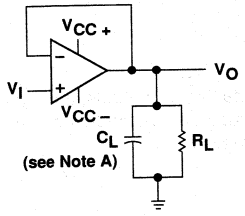
8. This parameter is tested on a sample basis for the TL032A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

perating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
SR−	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					0°C		3.7		3.2	5.0		
					70°C		4		3.2	5.0		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL032C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		49			49		nV/√Hz
				f = 1 kHz			41			41		
		TL032AC		f = 10 Hz	25°C		49			49		
				f = 1 kHz			41			41	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

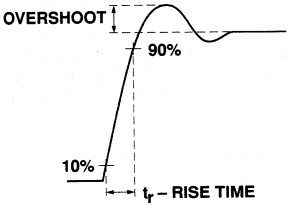


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

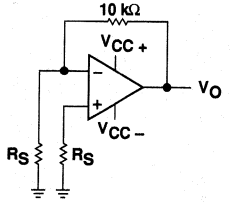
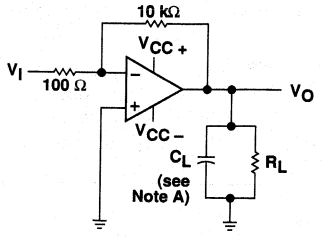


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

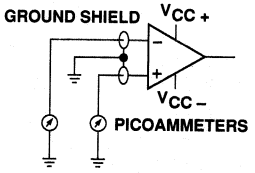


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL032 and TL032A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

able of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE

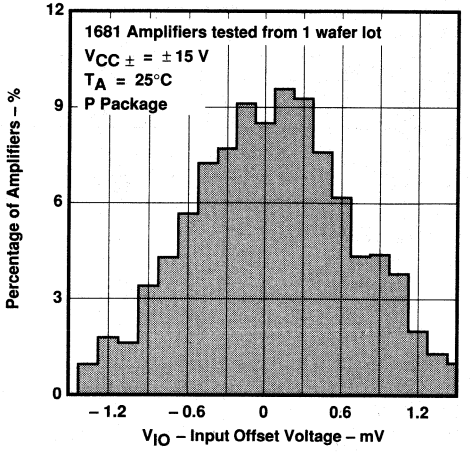


FIGURE 6

DISTRIBUTION OF TL032
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

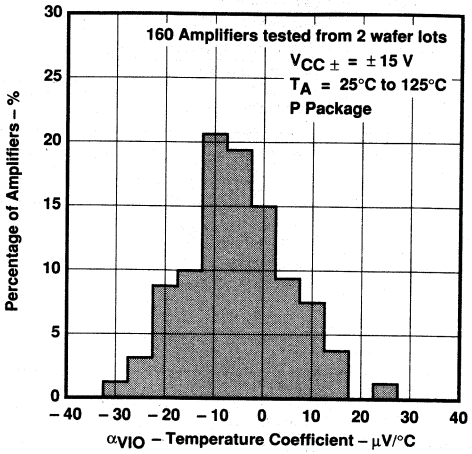


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

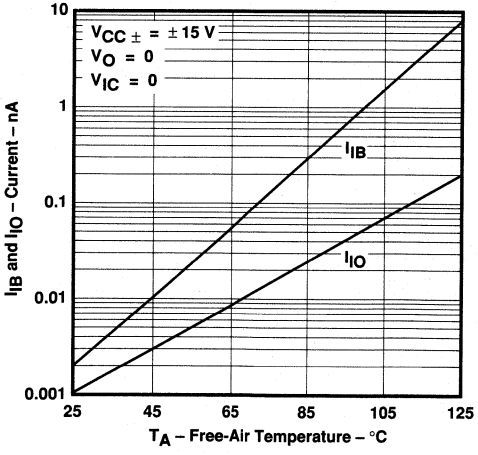


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

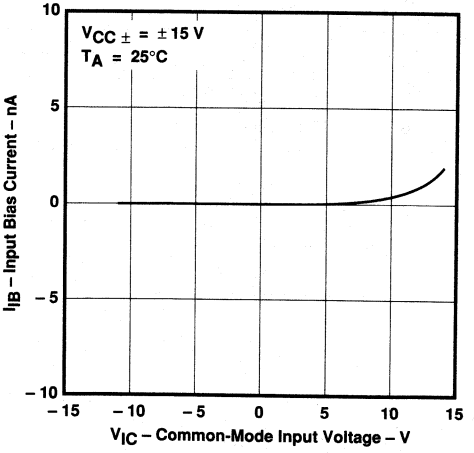


FIGURE 9

TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

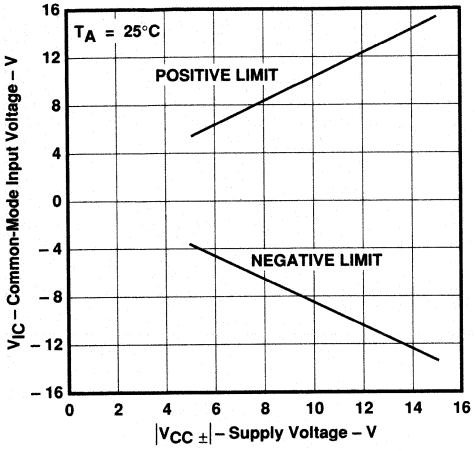


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

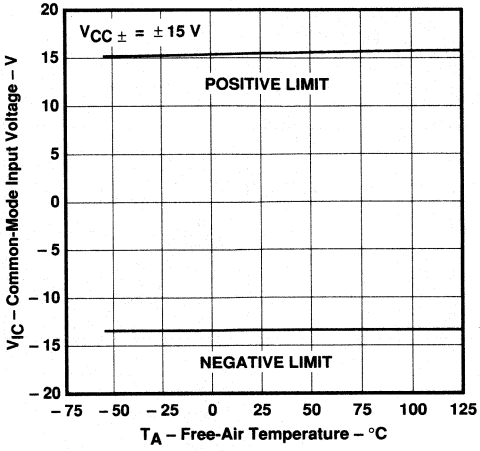


FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

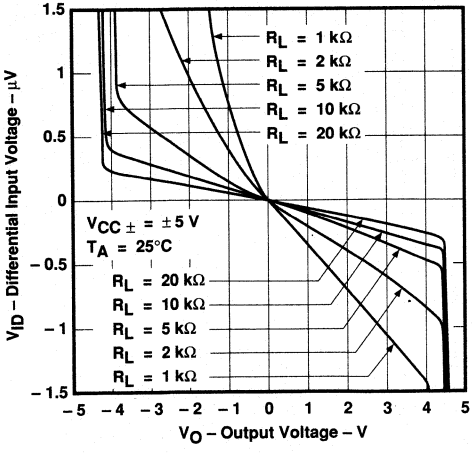


FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

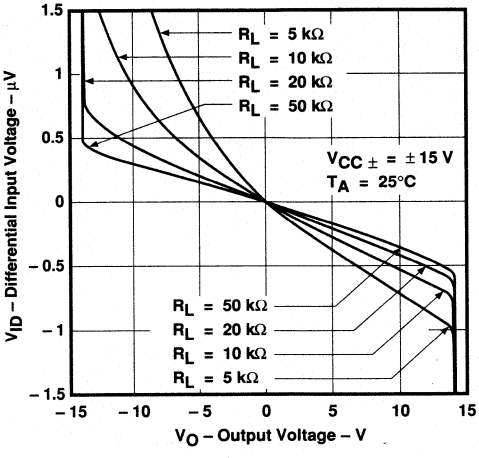


FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

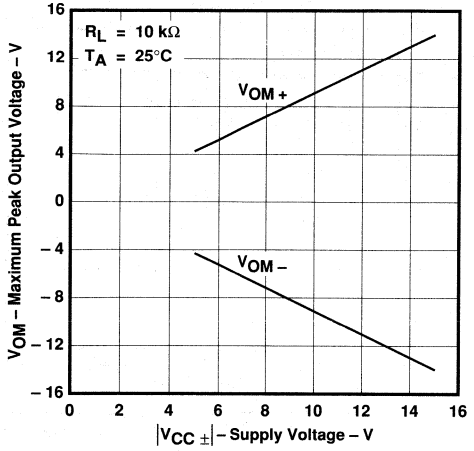


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

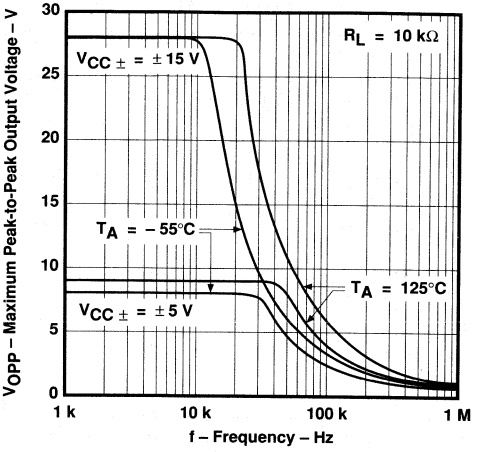


FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

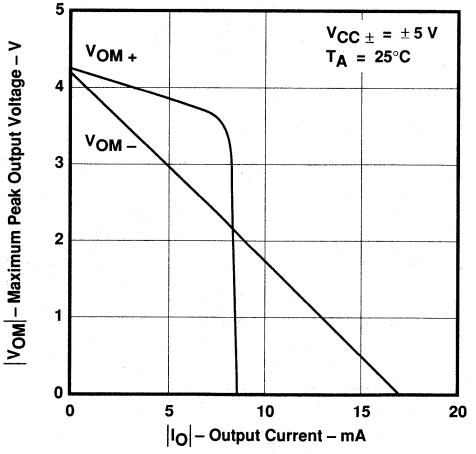


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

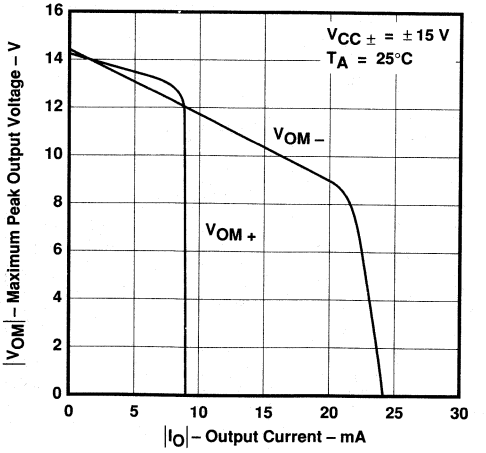


FIGURE 17

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

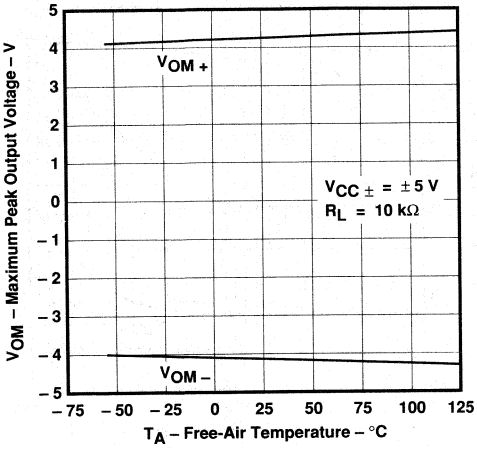


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

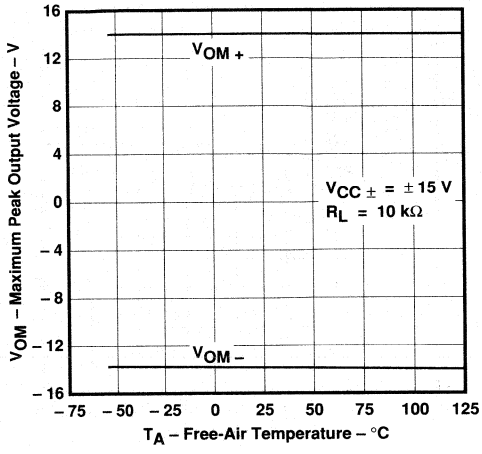


FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

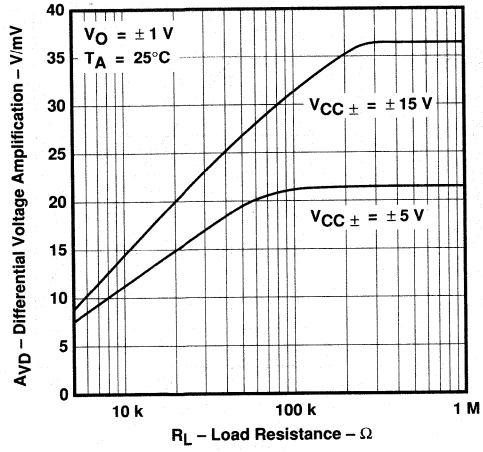


FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

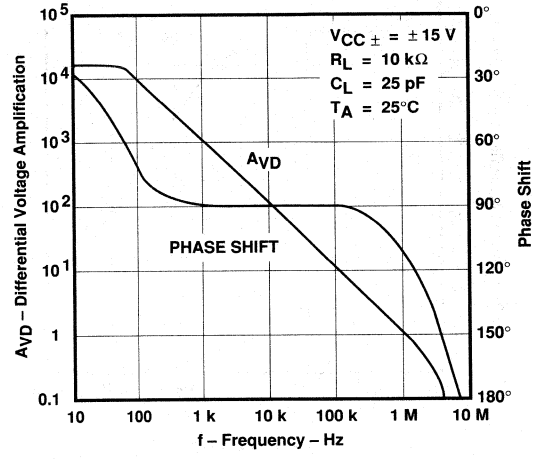


FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

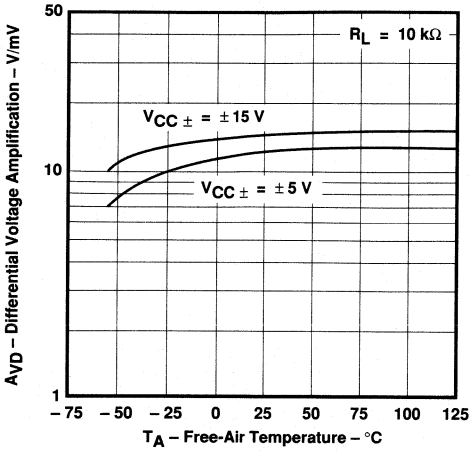


FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

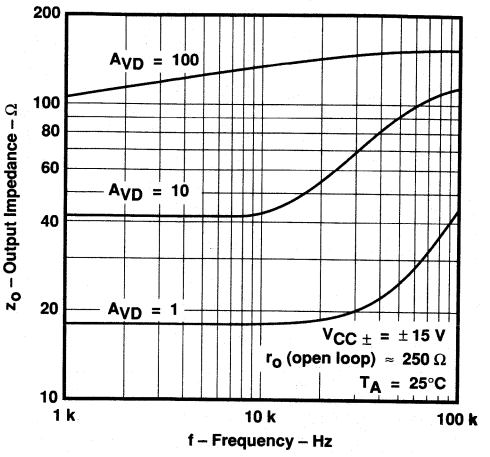


FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

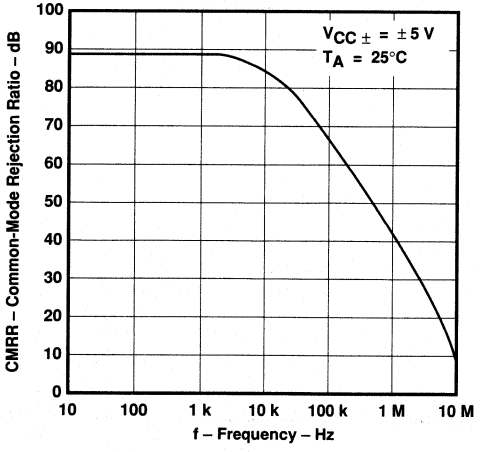


FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

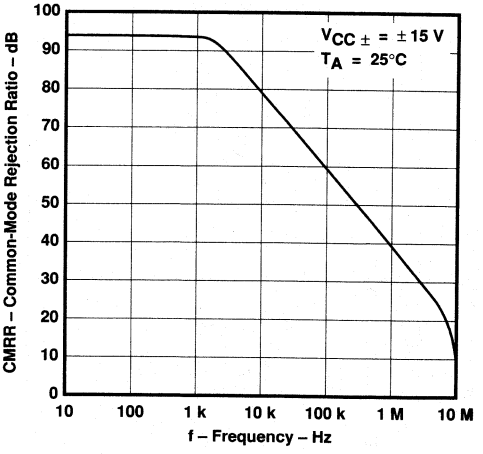


FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

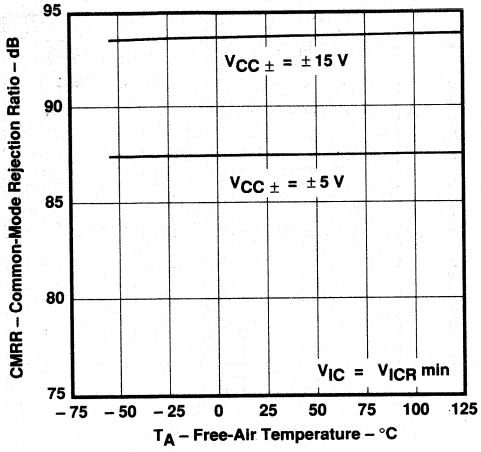


FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

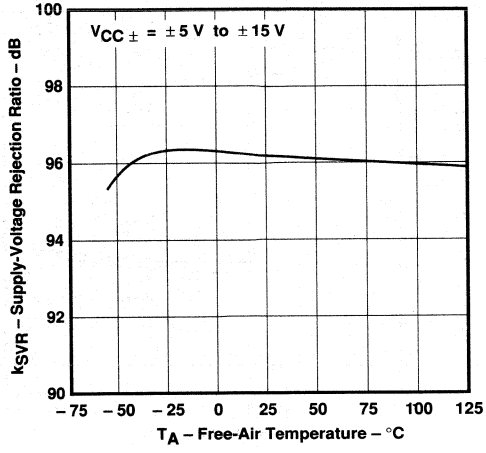


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

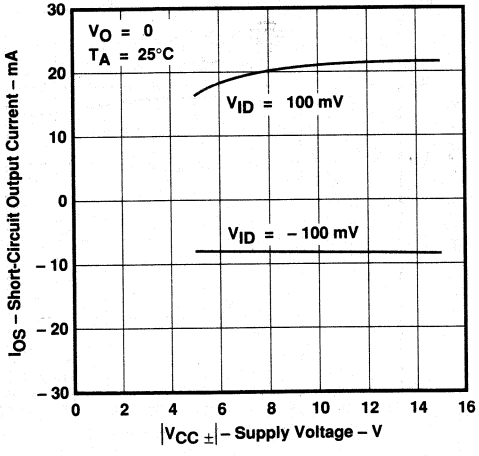


FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

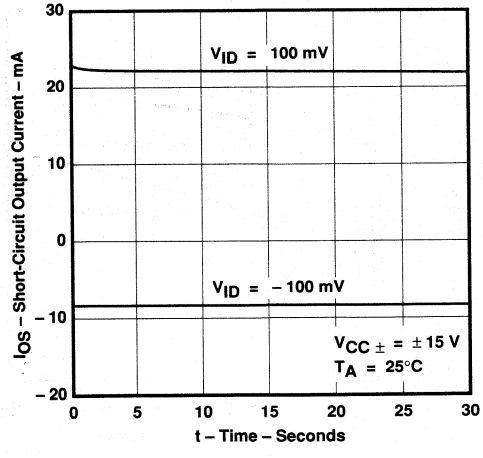


FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

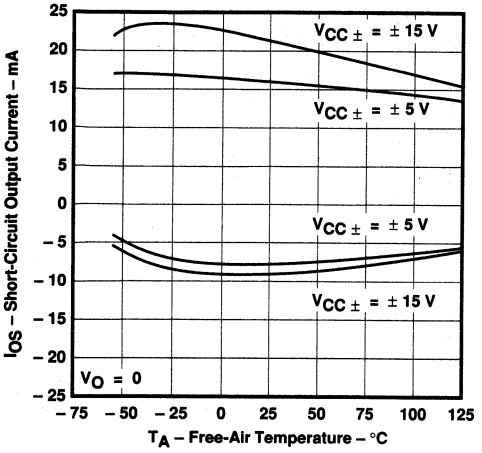


FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

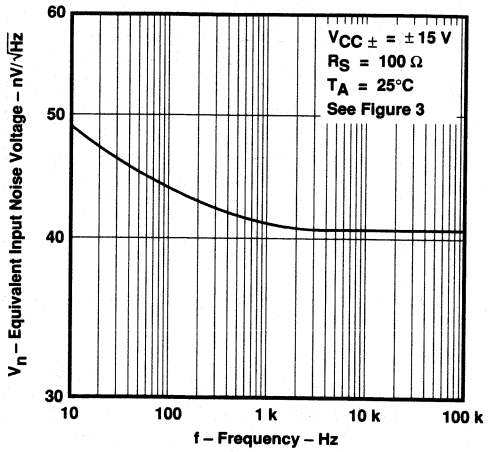


FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

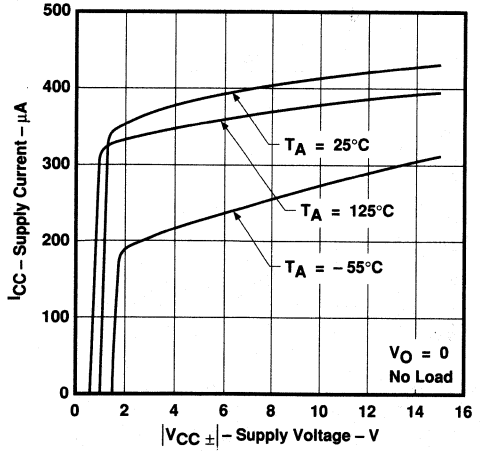


FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

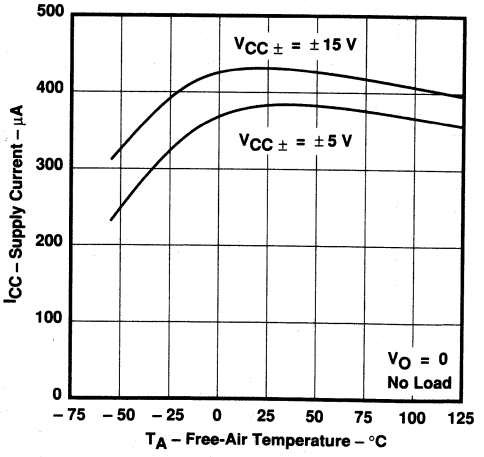


FIGURE 33

TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

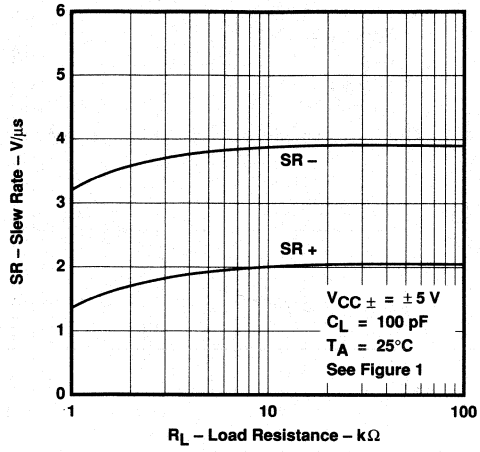


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

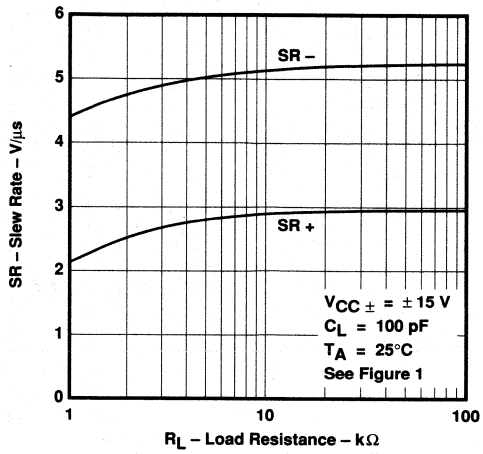


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

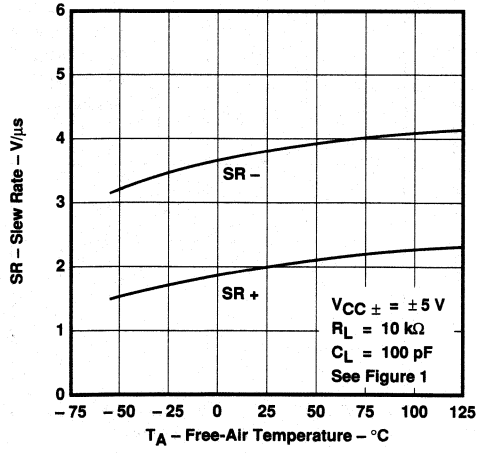


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

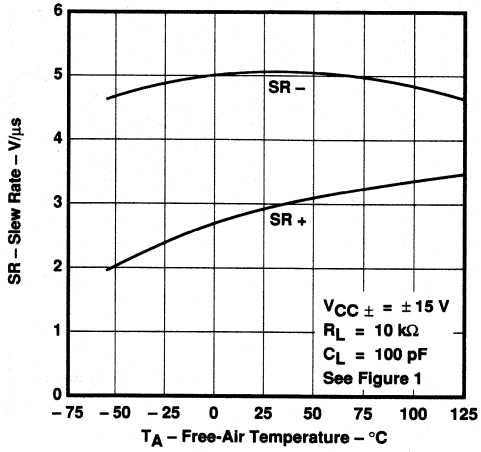


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

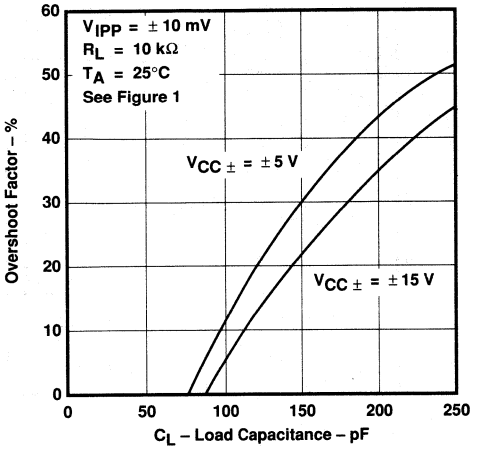


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

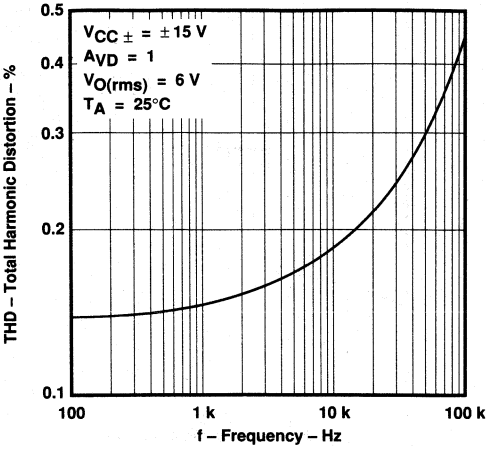


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

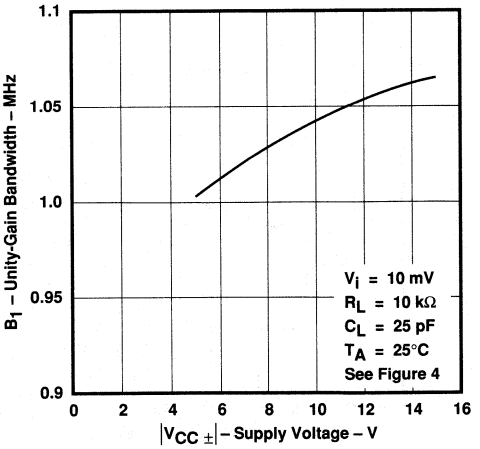


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

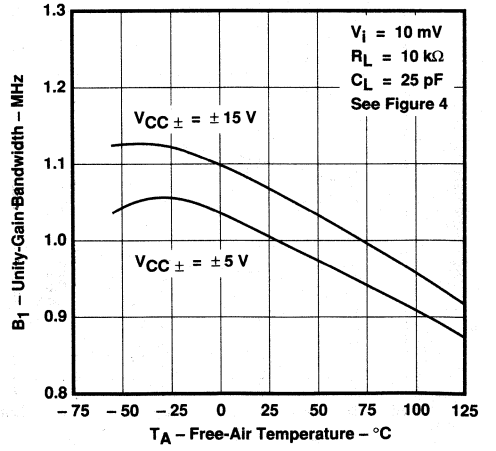


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

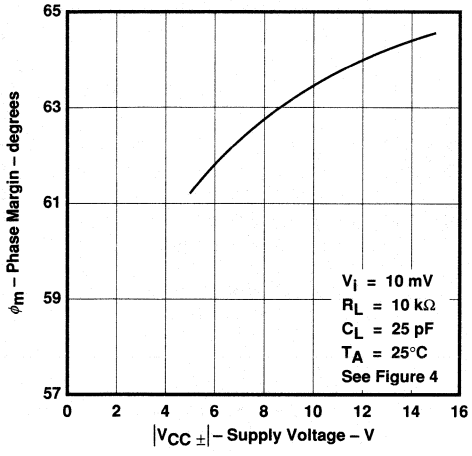


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

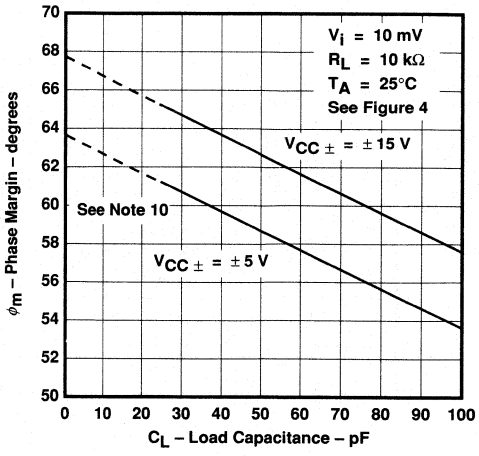


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

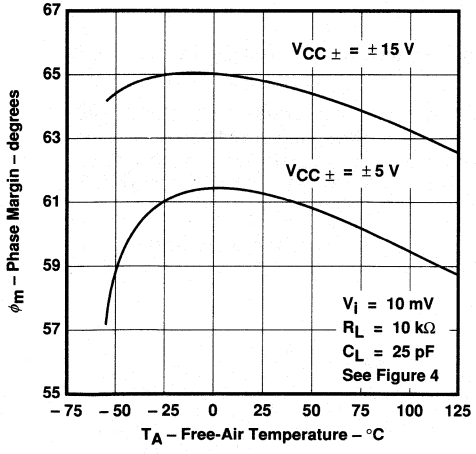


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

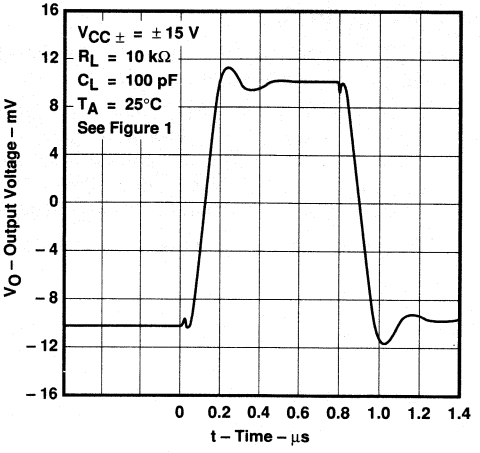


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

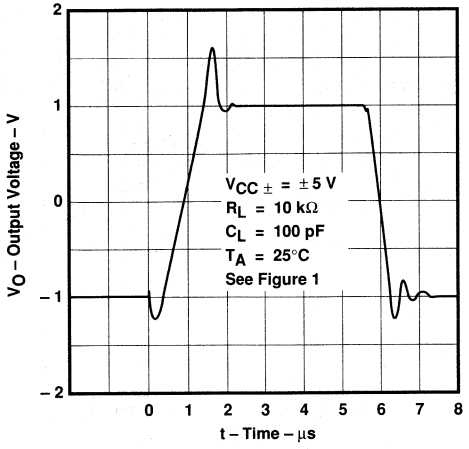


FIGURE 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

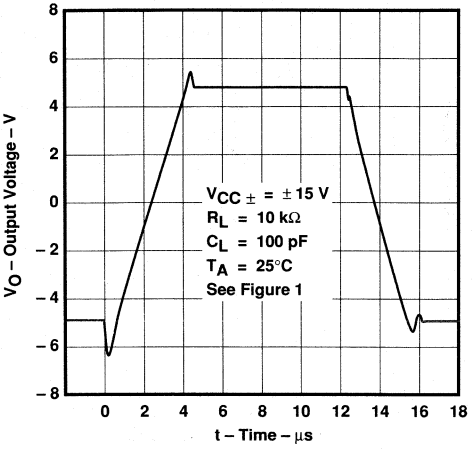


FIGURE 47

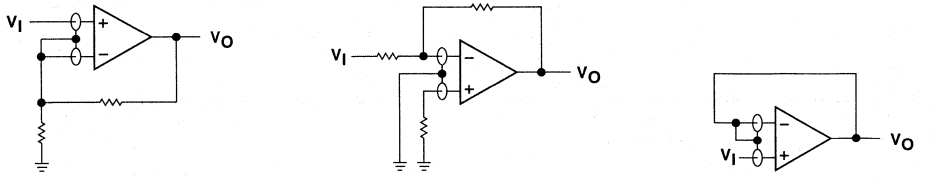
TYPICAL APPLICATION DATA

input characteristics

The TL032 and TL032A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL032 and TL032A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 48. USE OF GUARD RINGS

TEXAS INSTRUMENTS
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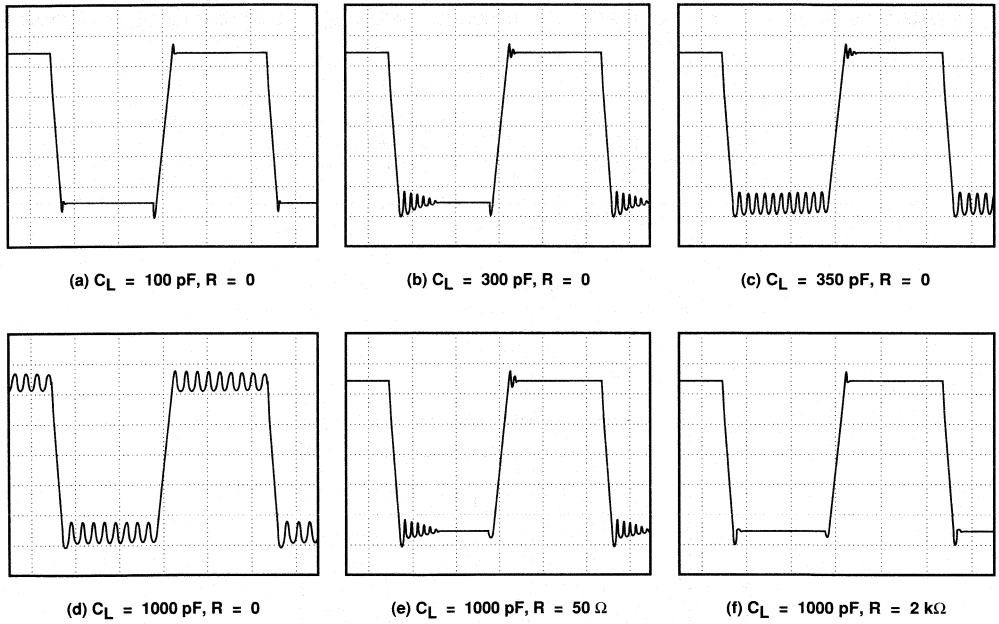
TYPICAL APPLICATION DATA

utput characteristics

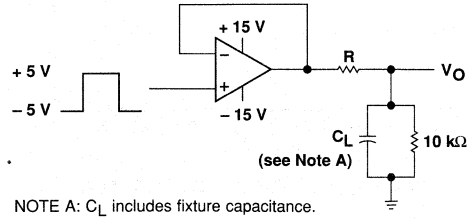
All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL032 and TL032A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

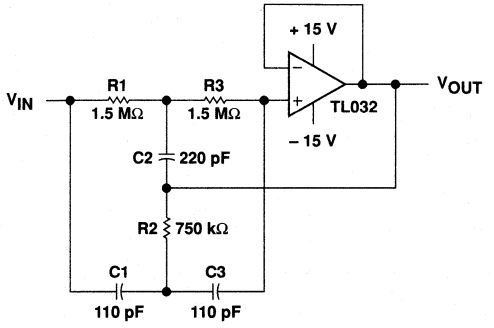
TYPICAL APPLICATION DATA

high-Q notch filter

In general, Texas Instruments enhanced JFET operational amplifiers serve as excellent filters. This circu provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that ar interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_O = \frac{1}{2\pi R1C1}$$

With the resistors and capacitors shown below, the center frequency is 1 kHz. Note that C1 = C3 = C2 ÷ and also that R1 = R3 = 2 × R2. The center frequency can be modified by varying these values. Whe adjusting the center frequency, be sure that the operational amplifier still has sufficient gain at the frequenc of interest.



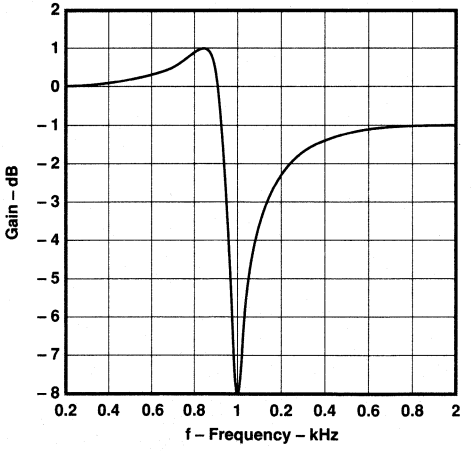


FIGURE 51. HIGH-Q NOTCH FILTER

TYPICAL APPLICATION DATA

2-wire 4- to 20-mA current loop

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuit benefits from the high input impedance of the TL032A since many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the TL032A's non-inverting input is zero, the following equation determines the output current:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\ V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_{IN} + 4\ mA$$

The current presently provides 4 to 20 mA output for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL032A was chosen:

$$I_O = V_{IN}\left(\frac{R3}{R1 \times R_S}\right) + 5\ V\left(\frac{R3}{R2 \times R_S}\right) - V_{IO}\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right) = 0.16 \times V_{IN} + 4\ mA - 0.17 \times V_{IO}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Thanks to the low-power consumption of the TL032A, this circuit has at least 2 mA available to drive the actual sensor from the 5-V reference node.

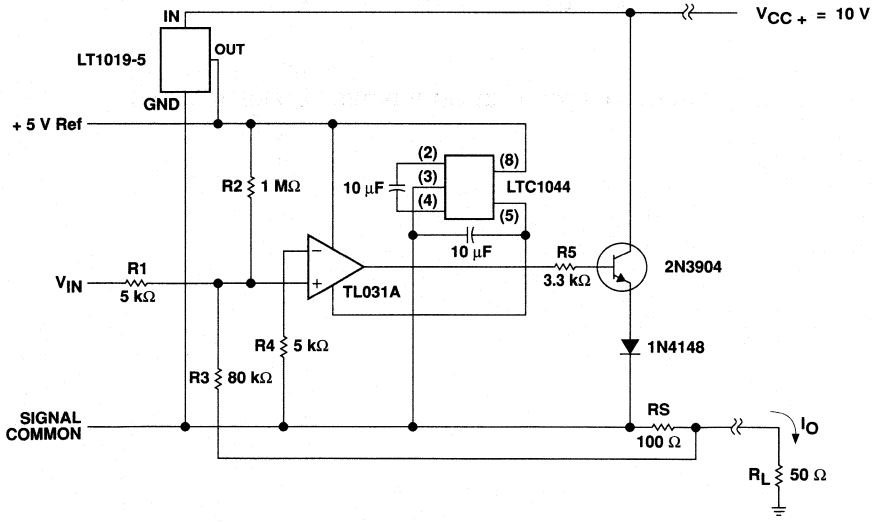


FIGURE 52. 2-WIRE 4- TO 20-mA CURRENT LOOP

TYPICAL APPLICATION DATA

low-level light detector preamplifier

Applications that need to detect small currents require high input impedance operational amplifiers; otherwise the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL032 allows even the smal currents resulting from low-level light to be detected.

In this circuit, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4l both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.

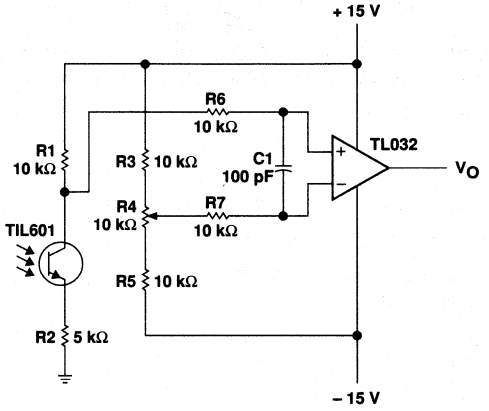


FIGURE 53. LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

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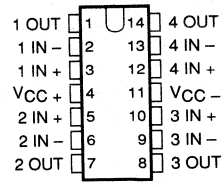
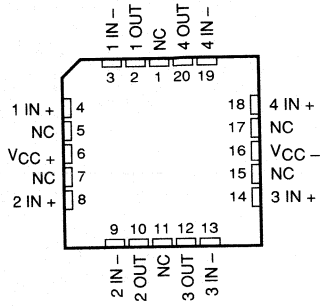
- **Maximum Offset Voltage . . . 1.5 mV**
- **High Slew Rate . . . 2.9 V/μs Typ**
- **Low Input Bias Current . . . 2 pA Typ**
- **Very Low Power Consumption . . . 26 mW Typ**
- **Output Short-Circuit Protection**
- **Monolithic Construction**

D, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

lescription

The TL034 and TL034A quadruple operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages, coupled with low power consumption, make the TL034 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL034 has been designed to be functionally compatible and pin compatible with the TL064.

Two offset voltage grades are available: TL034 (4 mV max) and TL034A (1.5 mV max).

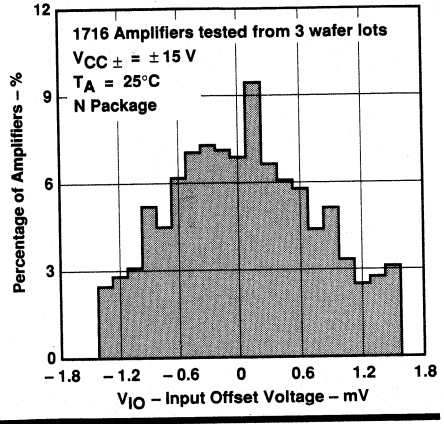
A variety of available packaging options includes small-outline and chip carrier versions for high density system applications.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	TL034ACD	—	TL034ACJ	TL034ACN
	4 mV	TL034CD	—	TL034CJ	TL034CN
– 40°C to 85°C	1.5 mV	TL034AID	—	TL034AIJ	TL034AIN
	4 mV	TL034ID	—	TL034IJ	TL034IN
– 55°C to 125°C	1.5 mV	TL034AMD	TL034AMFK	TL034AMJ	TL034AMN
	4 mV	TL034MD	TL034MFK	TL034MJ	TL034MN

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL034CDR).

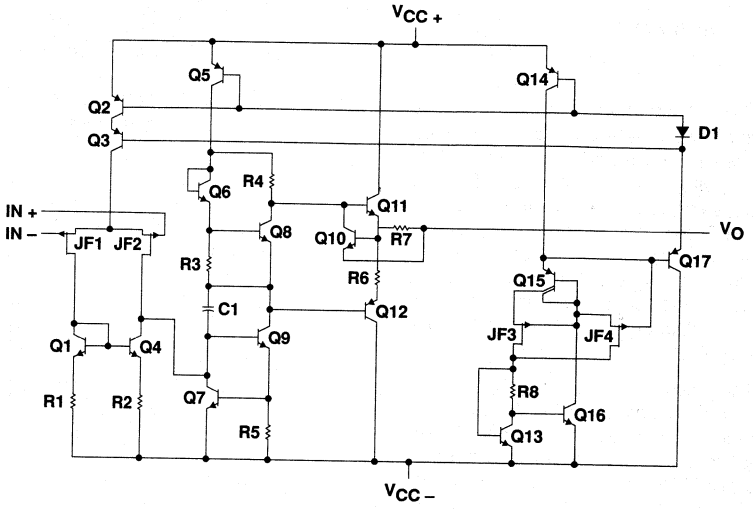
DISTRIBUTION OF TL034A
INPUT OFFSET VOLTAGE



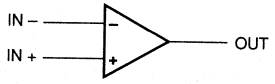
description (continued)

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C tc 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O (each output) . . . . . ± 40 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE TA = 25°C	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	– 1.5		4	– 1.5		4	– 1.5		4	V
	$V_{CC\pm}$ = ± 15 V	– 11.5		14	– 11.5		14	– 11.5		14	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL034M	25°C		0.91	6		0.78	4	mV
				Full range			11			9	
			TL034AM	25°C		0.7	3.5		0.58	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL034M	25°C to 125°C		10.6			10.9		μV/°C
			TL034AM	25°C to 125°C		10.6			10.9		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				125°C		0.2	10		0.2	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				125°C		7	20		8	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−55°C	3	4.1		13	14		
				125°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−55°C	−3	−4		−12.5	−13.8		
				125°C	−3	−4.3		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−55°C	3	7.1		4	10.4		
				125°C	3	12.9		4	15		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−55°C	70	87		70	94		
				125°C	70	87		70	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−55°C	75	95		75	95		
				125°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, V_O = 0		25°C		7.7	10		26	34	mW
				−55°C		4.6	10		18.7	34	
				125°C		7.1	10		23.6	34	
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		0.77	1		0.87	1.12	mA
				−55°C		0.46	1		0.62	1.12	
				125°C		0.71	1		0.79	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

operating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					−55°C		1.4		1.2	1.9		
					125°C		2.4		1.2	3.5		
SR−	Negative slew rate at unity gain				25°C		3.9		3	5.1		V/μs
					−55°C		3.2		2.5	4.6		
					125°C		4.1		2.5	4.7		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
t_f	Fall time				25°C		138			132		ns
					−55°C		142			123		
					125°C		166			158		
	Overshoot factor				25°C		11%			5%		
					−55°C		16%			6%		
					125°C		14%			8%		
V_n	Equivalent input noise voltage	TL034M	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AM		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43		
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−55°C		1			1.1		
					125°C		0.9			0.9		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−55°C		57°			64°		
					125°C		59°			62°		

NOTE 7: For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL034I	25°C		0.91	6		0.79	4	mV
				Full range			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL034I	25°C to 85°C		11.5			11.6		µV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				−40°C	3	4.1		13	14		
				85°C	3	4.4		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				−40°C	−3	−4.1		−12.5	−13.8		
				85°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				−40°C	3	8.4		4	11.6		
				85°C	4	13.5		5	15.3		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				−40°C	70	87		75	94		
				85°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				−40°C	75	96		75	96		
				85°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, V_O = 0		25°C		7.7	10		26	34	mW
				−40°C		5.8	10		21.7	34	
				85°C		7.4	10		24.8	34	
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		0.77	1		0.87	1.12	mA
				−40°C		0.58	1		0.72	1.12	
				85°C		0.74	1		0.83	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

8. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

perating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					−40°C		1.6		1.5	2.1		
					85°C		2.3		2	3.3		
$SR-$	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					−40°C		3.3		3.2	4.8		
					85°C		4.1		3.2	4.9		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
t_f	Fall time				25°C		138			132		ns
					−40°C		132			123		
					85°C		154			146		
	Overshoot factor				25°C		11%			5%		
					−40°C		12%			5%		
					85°C		13%			7%		
V_n	Equivalent input noise voltage (see Note 9)	TL034I	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AI		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					−40°C		1			1.1		
					85°C		0.9			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					−40°C		60°			65°		
					85°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL034C	25°C		0.91	6		0.79	4	mV
				Full range			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 8)		TL034C	25°C to 70°C		11.6			12		μV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		1	100		1	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		2	200		2	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.4		−11.5 to 14	−13.4 to 15.4		V
				Full range	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.3		13	14		V
				0°C	3	4.2		13	14		
				70°C	3	4.3		13	14		
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−3	−4.2		−12.5	−13.9		V
				0°C	−3	−4.1		−12.5	−13.9		
				70°C	−3	−4.2		−12.5	−14		
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6		25°C	4	12		5	14.3		V/mV
				0°C	3	11.1		4	13.5		
				70°C	4	13.3		5	15.2		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		5			4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	70	87		75	94		dB
				0°C	70	87		75	94		
				70°C	70	87		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	96		75	96		dB
				0°C	75	96		75	96		
				70°C	75	96		75	96		
P_D	Total power dissipation (four amplifiers)	No load, V_O = 0		25°C		7.7	10		26	34	mW
				0°C		7.4	10		25.3	34	
				70°C		7.6	10		25.2	34	
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		0.77	1		0.87	1.12	mA
				0°C		0.74	1		0.85	1.12	
				70°C		0.76	1		0.84	1.12	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. At $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

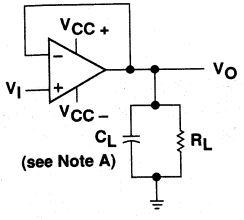
8. This parameter is tested on a sample basis for the TL034A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

perating characteristics

PARAMETER			TEST CONDITIONS		T_A	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain		R_L = 10 kΩ, C_L = 100 pF, See Figure 1, See Note 7		25°C		2		2	2.9		V/μs
					0°C		1.8		1.5	2.6		
					70°C		2.2		2	3.2		
SR−	Negative slew rate at unity gain				25°C		3.9		3.5	5.1		V/μs
					0°C		3.7		3.2	5.0		
					70°C		4		3.2	5.0		
t_r	Rise time		V_{IPP} = ±10 mV, R_L = 10 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
t_f	Fall time				25°C		138			132		ns
					0°C		134			127		
					70°C		150			142		
	Overshoot factor				25°C		11%			5%		
					0°C		10%			4%		
					70°C		12%			6%		
V_n	Equivalent input noise voltage (see Note 9)	TL034C	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		83			83		nV/√Hz
				f = 1 kHz			43			43		
		TL034AC		f = 10 Hz	25°C		83			83		
				f = 1 kHz			43			43	60	
I_n	Equivalent input noise current		f = 1 kHz		25°C		0.003			0.003		pA/√Hz
B1	Unity-gain bandwidth		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		1			1.1		MHz
					0°C		1			1.1		
					70°C		1			1		
ϕ_m	Phase margin at unity gain		V_i = 10 mV, R_L = 10 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			65°		
					0°C		61°			65°		
					70°C		60°			64°		

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

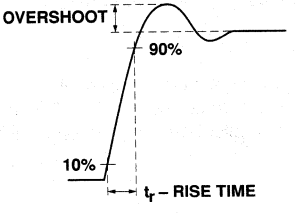


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

PARAMETER MEASUREMENT INFORMATION

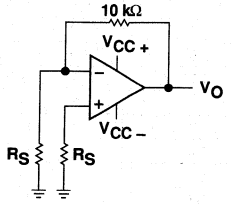
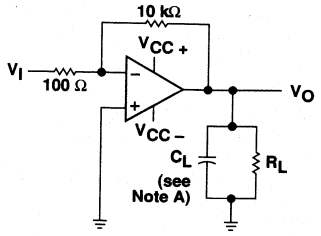


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

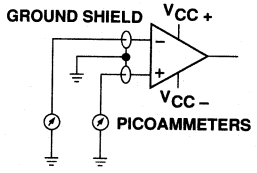


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TL034 and TL034A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

able of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	16, 17
		vs Frequency	15
		vs Temperature	18, 19
A_{VD}	Differential voltage amplification	vs R_L	20
		vs Frequency	21
		vs Temperature	22
z_o	Output impedance	vs Frequency	23
CMRR	Common-mode rejection ratio	vs Frequency	24, 25
		vs Temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	27
I_{OS}	Short-circuit output current	vs V_{CC}	28
		vs Time	29
		vs Temperature	30
I_{CC}	Supply current	vs V_{CC}	32
		vs Temperature	33
SR	Slew rate	vs R_L	34, 35
		vs Temperature	36, 37
	Overshoot factor	vs C_L	38
V_n	Equivalent input noise voltage	vs Frequency	31
THD	Total harmonic distortion	vs Frequency	39
B_1	Unity-gain bandwidth	vs V_{CC}	40
		vs Temperature	41
ϕ_m	Phase margin	vs V_{CC}	42
		vs C_L	43
		vs Temperature	44
	Phase shift	vs Frequency	21
	Pulse response	Small-signal	45
		Large-signal	46, 47

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE

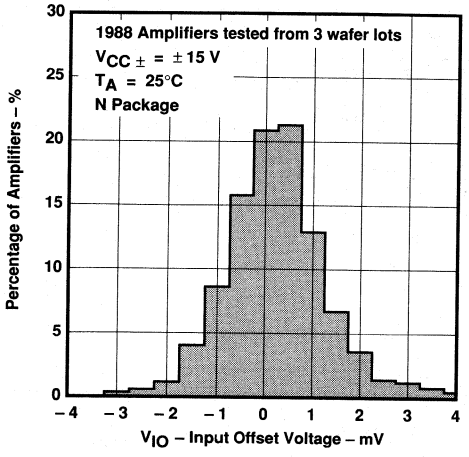


FIGURE 6

DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

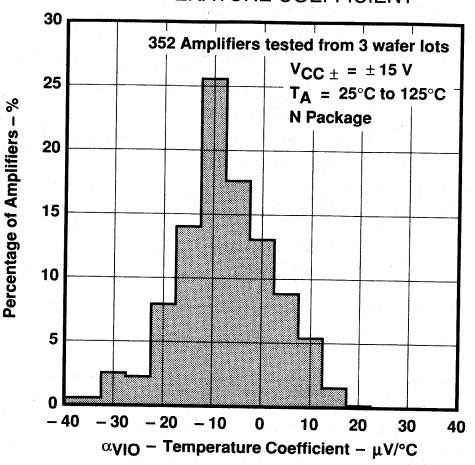


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

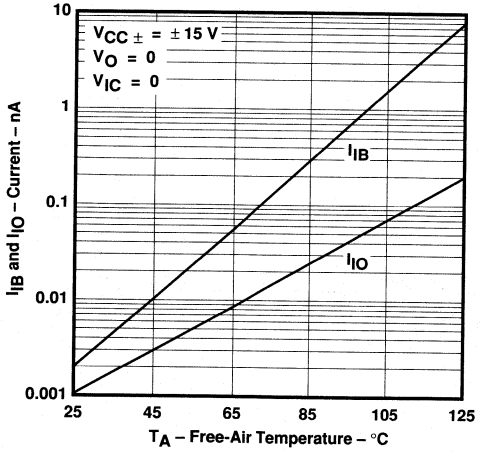


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

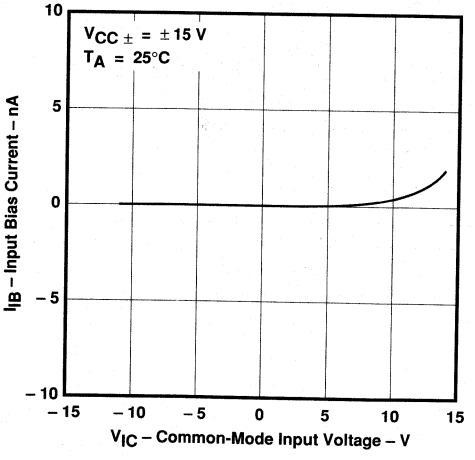


FIGURE 9

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TYPICAL CHARACTERISTICS

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

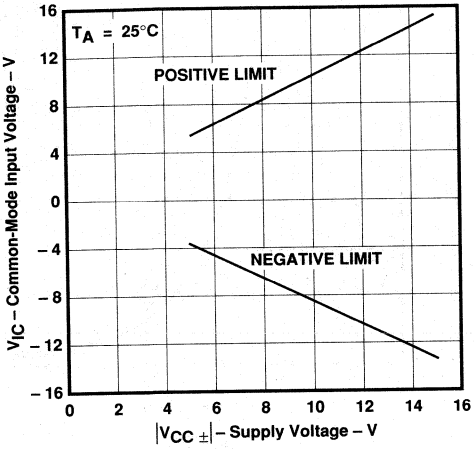

FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

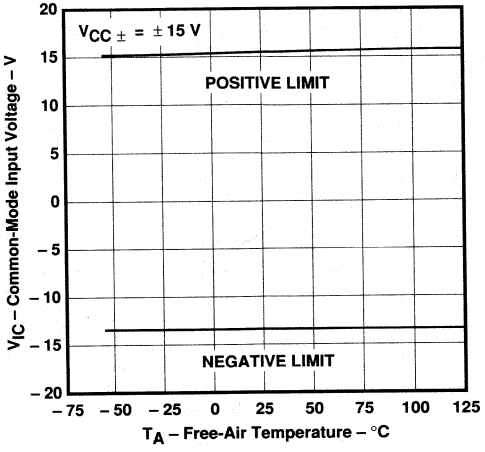

FIGURE 11

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

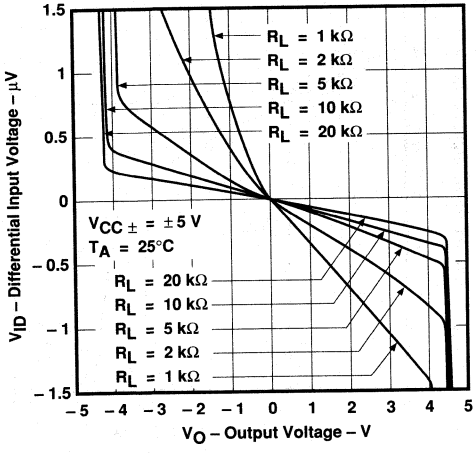

FIGURE 12

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

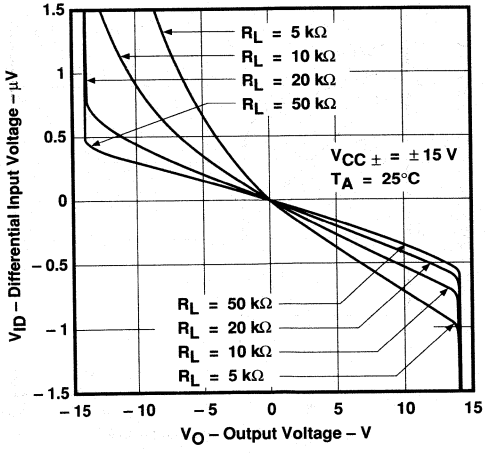

FIGURE 13

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

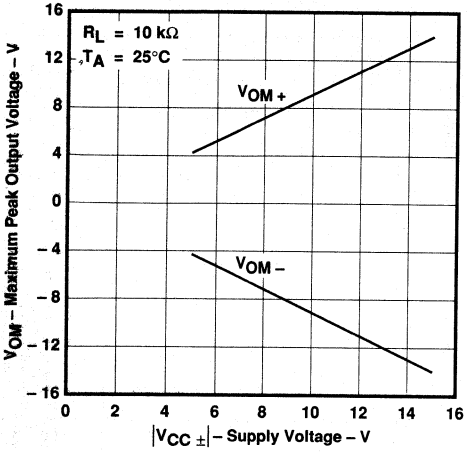

FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

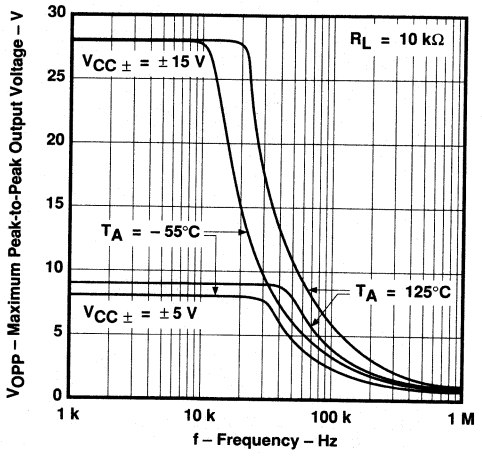

FIGURE 15

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

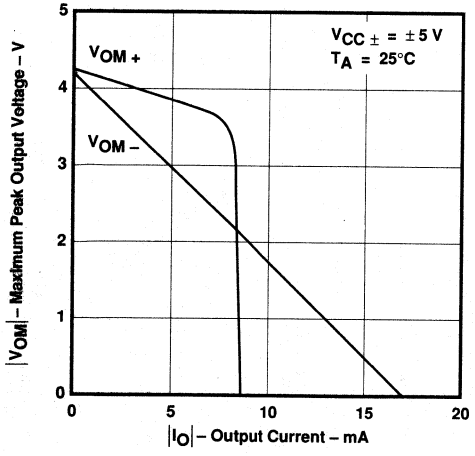

FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

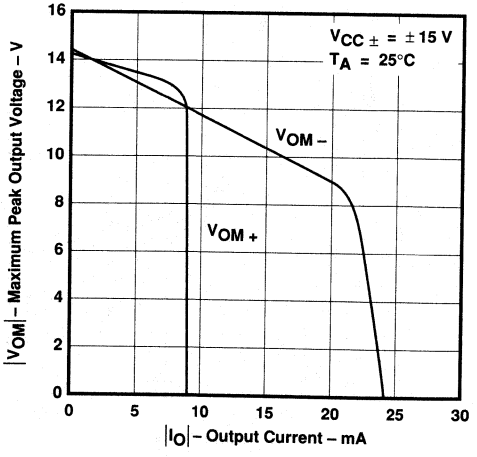

FIGURE 17

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

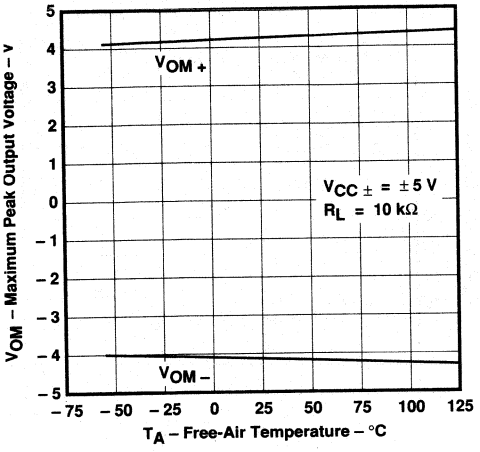

FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

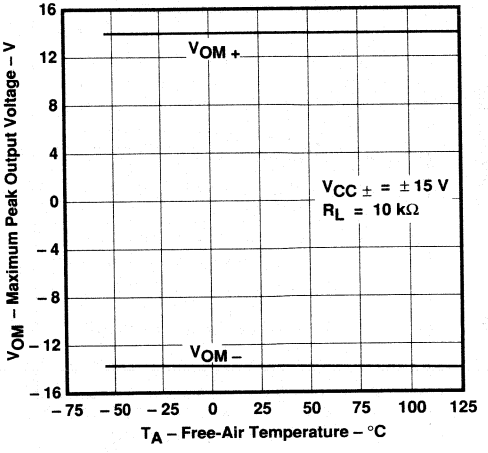

FIGURE 19

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

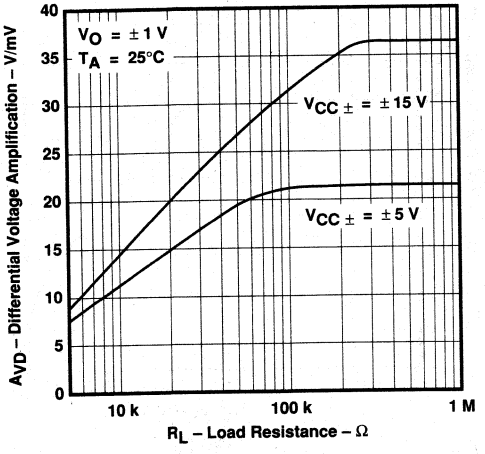

FIGURE 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

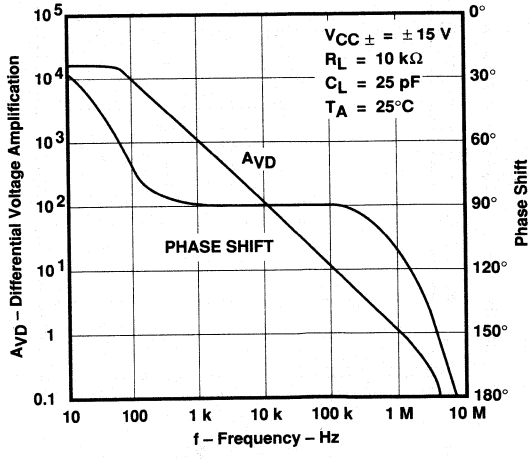

FIGURE 21

TYPICAL CHARACTERISTICS

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

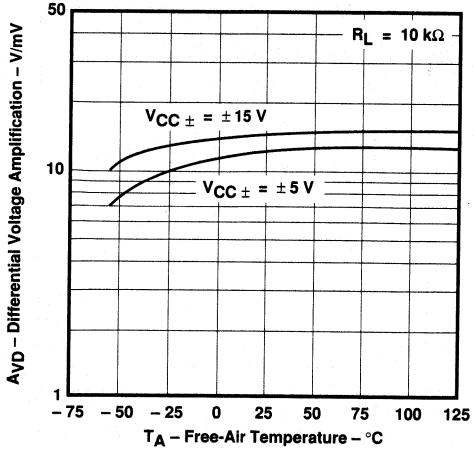

FIGURE 22

OUTPUT IMPEDANCE
vs
FREQUENCY

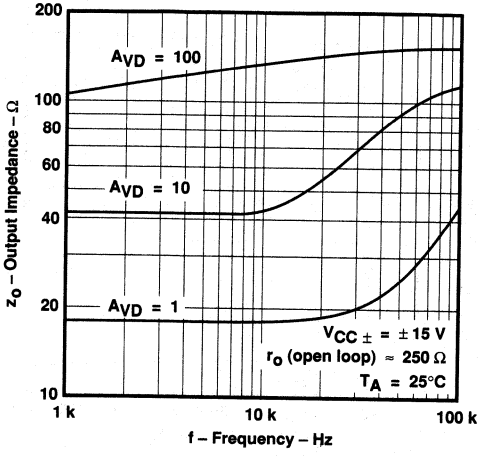

FIGURE 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

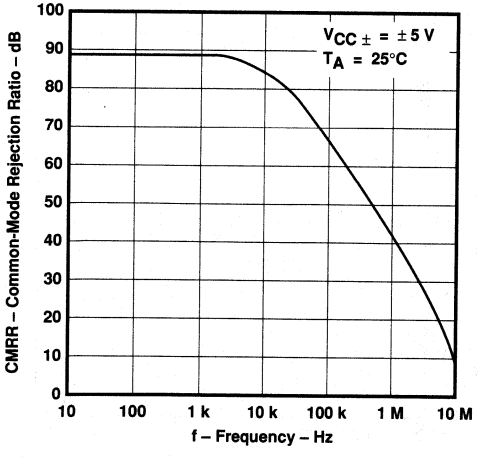

FIGURE 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

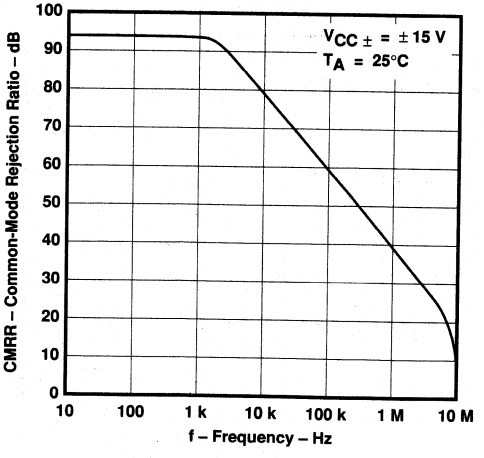

FIGURE 25

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

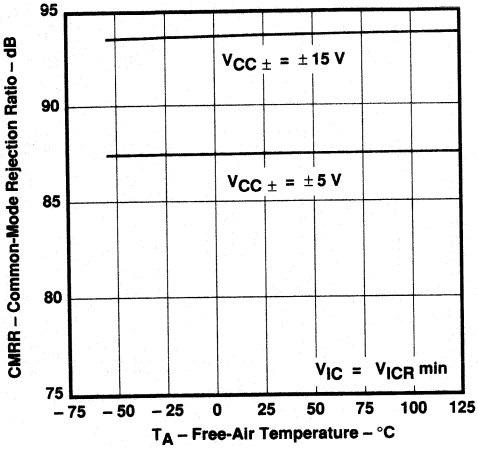

FIGURE 26

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

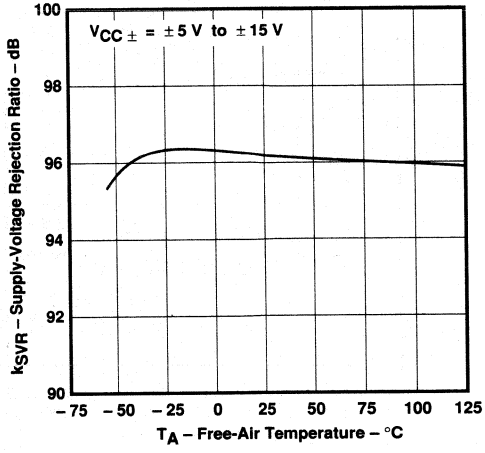

FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

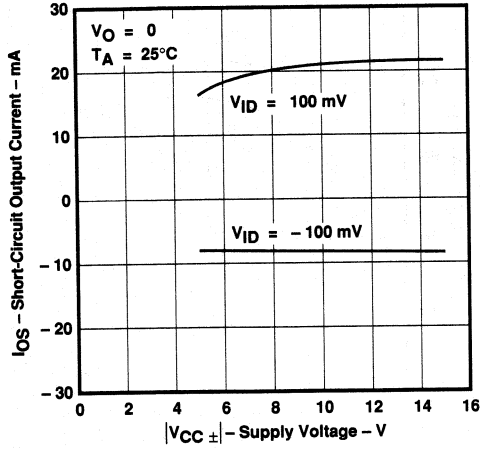

FIGURE 28

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

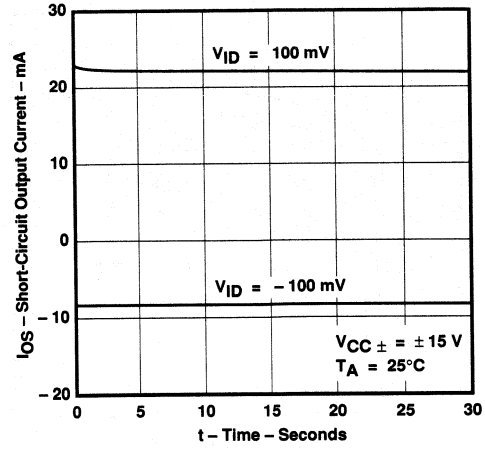

FIGURE 29

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

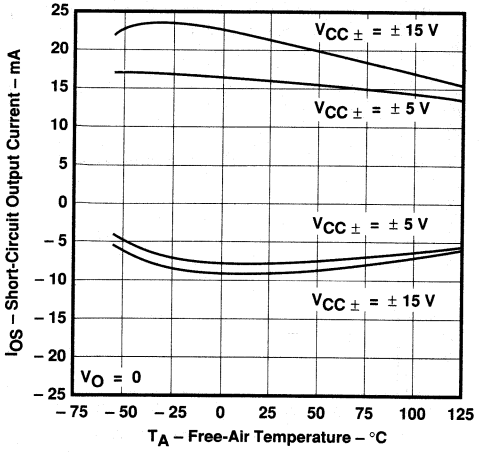

FIGURE 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

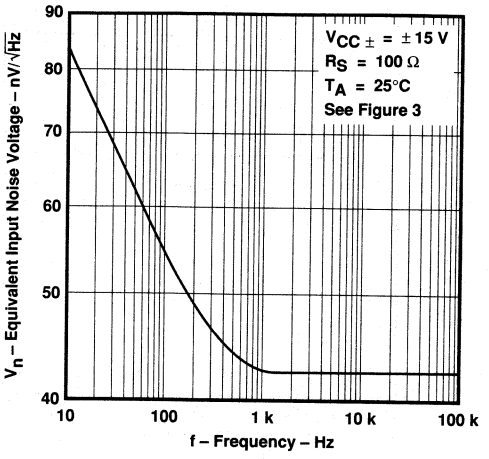

FIGURE 31

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

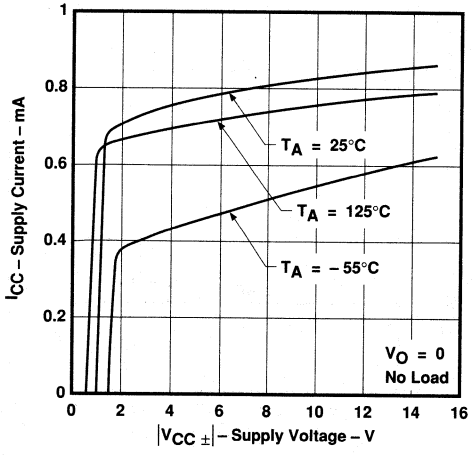

FIGURE 32

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

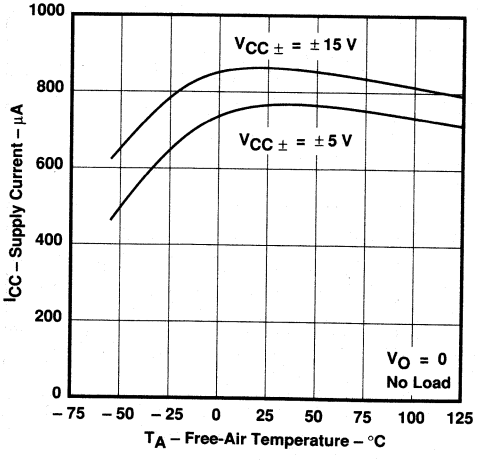

FIGURE 33

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD RESISTANCE

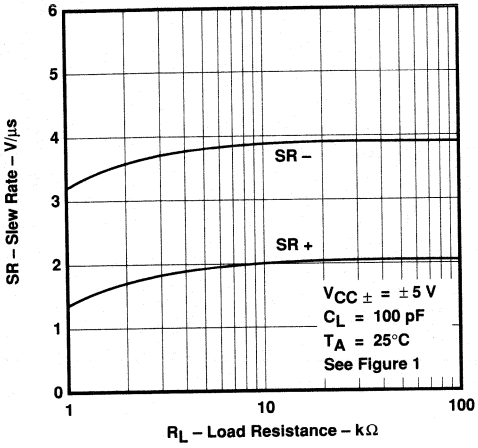


FIGURE 34

SLEW RATE
vs
LOAD RESISTANCE

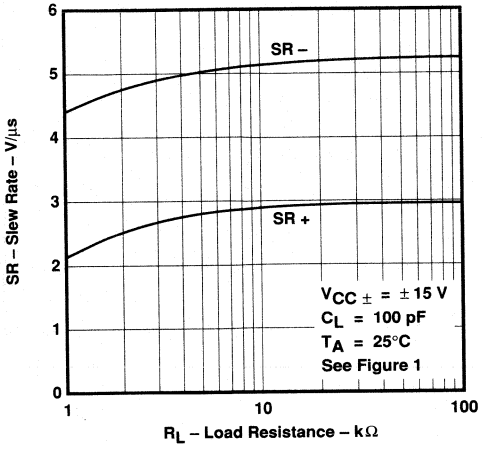


FIGURE 35

SLEW RATE
vs
FREE-AIR TEMPERATURE

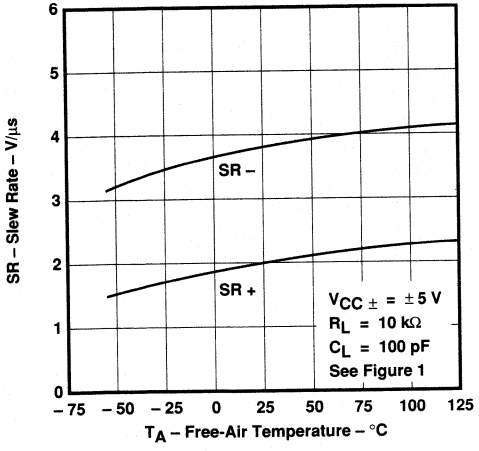


FIGURE 36

SLEW RATE
vs
FREE-AIR TEMPERATURE

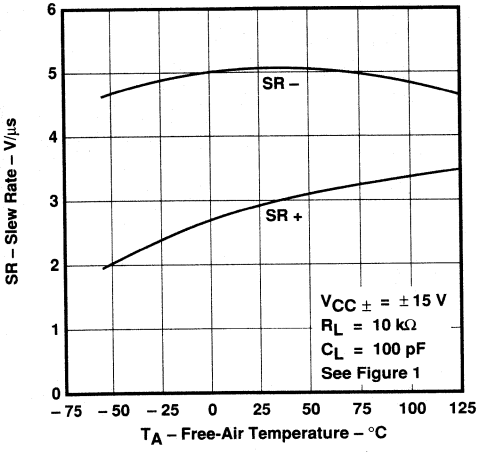


FIGURE 37

TYPICAL CHARACTERISTICS

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

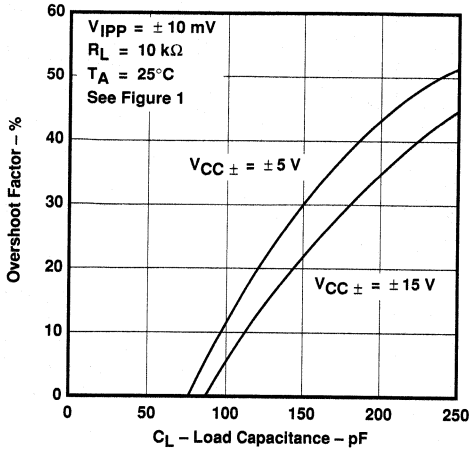


FIGURE 38

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

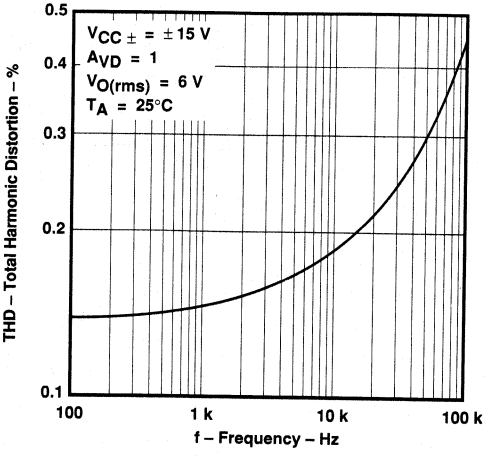


FIGURE 39

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

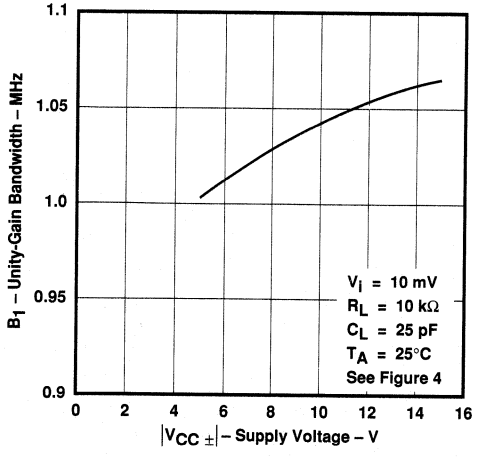


FIGURE 40

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

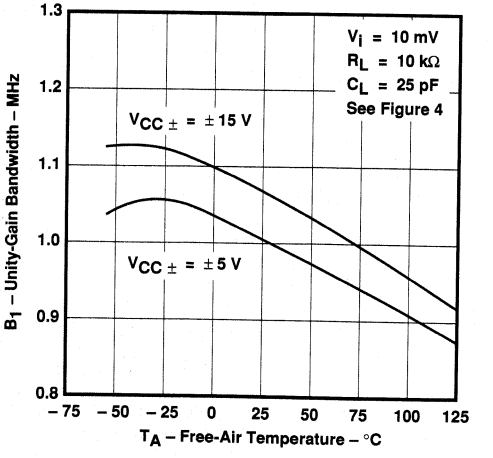


FIGURE 41

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

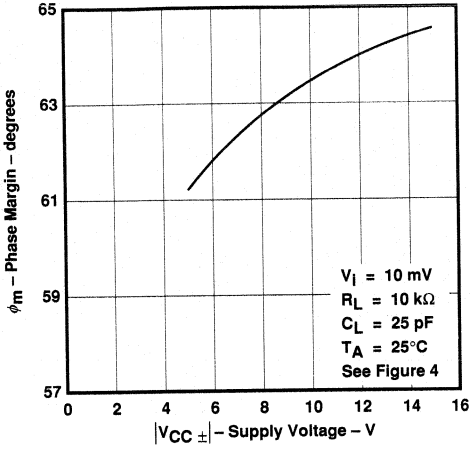


FIGURE 42

PHASE MARGIN
vs
LOAD CAPACITANCE

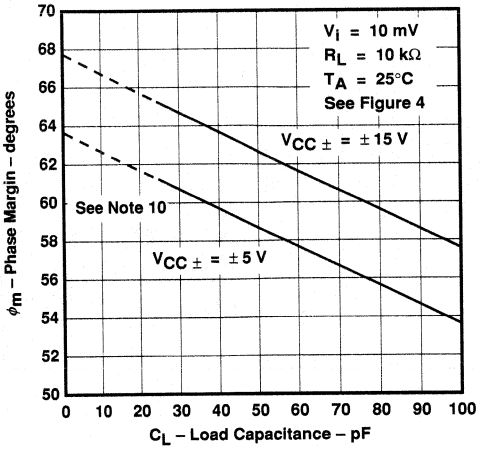


FIGURE 43

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

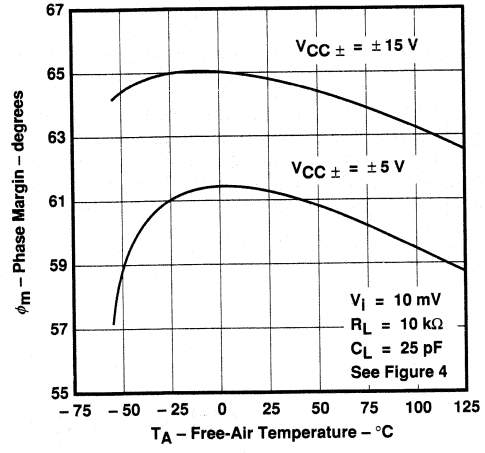


FIGURE 44

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

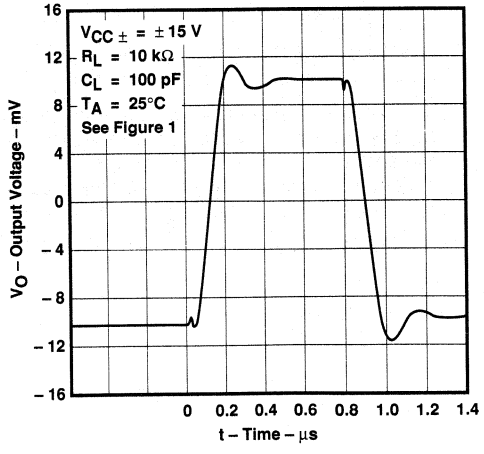


FIGURE 45

NOTE 10: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

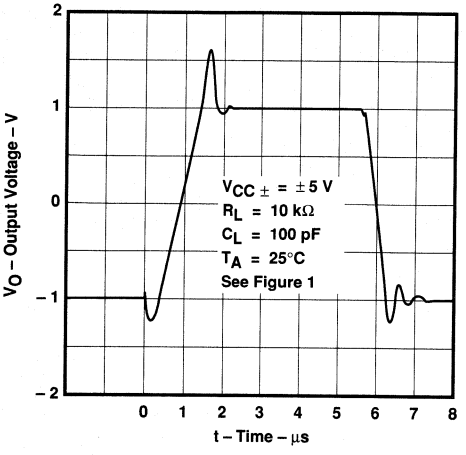


FIGURE 46

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

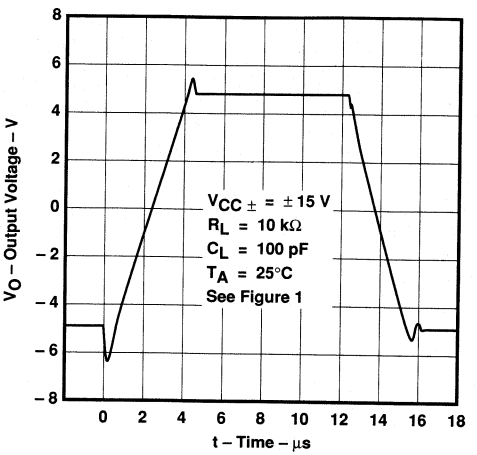


FIGURE 47

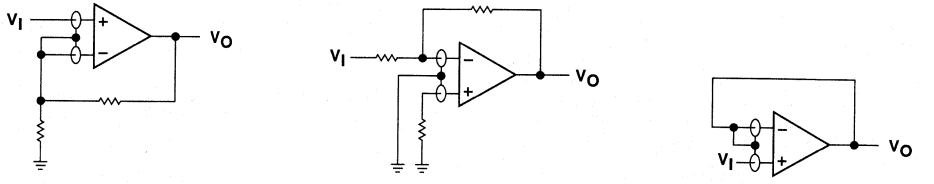
TYPICAL APPLICATION DATA

input characteristics

The TL034 and TL034A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL034 and TL034A are well-suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 48). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 48. USE OF GUARD RINGS

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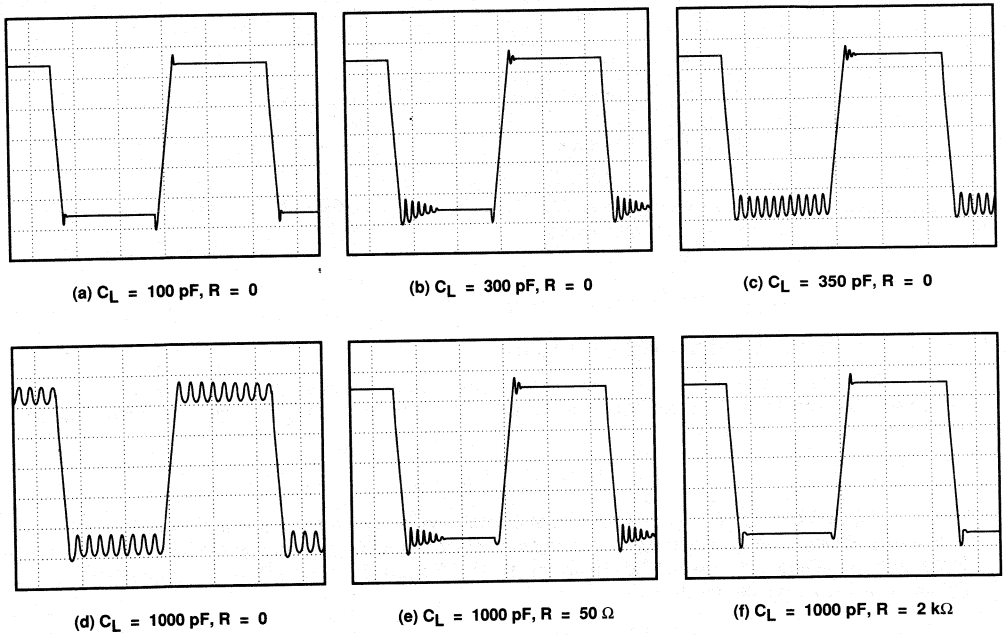
TYPICAL APPLICATION DATA

Output characteristics

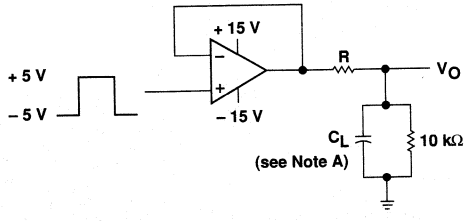
All operating characteristics (except bandwidth and phase margin) are specified with 100 pF load capacitance. The TL034 and TL034A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 49).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L = 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 49. EFFECT OF CAPACITIVE LOADS



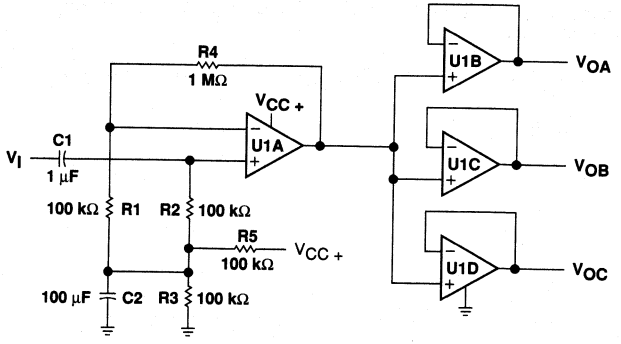
NOTE A: C_L includes fixture capacitance.

FIGURE 50. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

audio distribution amplifier

This audio distribution amplifier feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10 while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL034 allows quick response to the input signal while maintaining low power consumption.



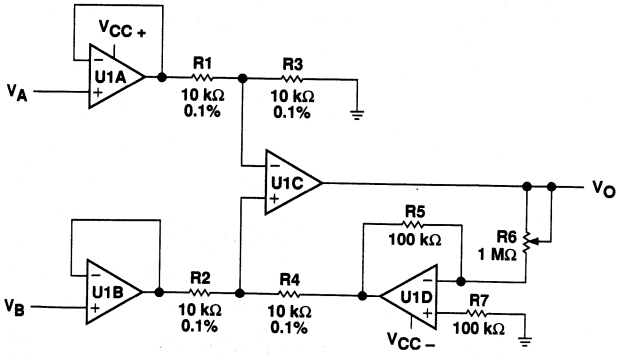
NOTE : U1A through U1D = TL034; V_{CC+} = 5 V.

instrumentation amplifier with linear gain adjust

The TL034 low-offset voltage and low-power consumption provides an accurate but inexpensive instrumentation amplifier. This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 should always be greater or equal to the value of R5 in order to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1% tolerance resistors.



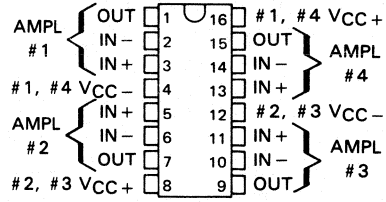
NOTE : U1A through U1D = TL034; $V_{CC\pm}$ = ±15 V.

D1662, SEPTEMBER 1973—REVISED JUNE 1988

- **Very Low Power Consumption**
- **Typical Power Dissipation with ±2-V Supplies . . . 340 μW**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Input Offset Voltage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Power Applied in Pairs**

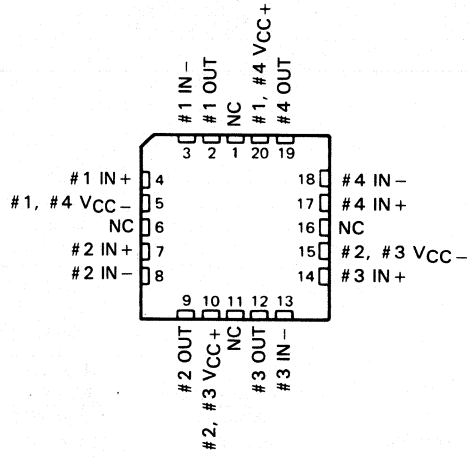
TL044M IS NOT RECOMMENDED FOR NEW DESIGNS.

TL044M . . . J OR W DUAL-IN-LINE PACKAGE
TL044C . . . J OR N PACKAGE
(TOP VIEW)



Pins 4 and 12 are internally connected together in the N package only.

TL044M . . . FK PACKAGE
(TOP VIEW)



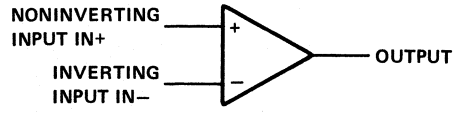
NC—No internal connection

description

The TL044 is a quad low-power operational amplifier designed to replace higher-power devices in many applications without sacrificing system performance. High input impedance, low supply currents, and low equivalent input noise voltage over a wide range of operating supply voltages result in an extremely versatile operational amplifier for use in a variety of analog applications including battery-operated circuits. Internal frequency compensation, absence of latch-up, high slew rate, and output short-circuit protection assure ease of use. Power may be applied separately to Section A (amplifiers 1 and 4) or Section B (amplifiers 2 and 3) while the other pair remains unpowered.

The TL044M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL044C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	FLAT PACK (W)
0°C to 70°C	5 mV	—	TL044CJ	TL044CN	—
−55°C to 125°C	5 mV	TL044MFK	TL044MJ	—	TL044MW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL044M	TL044C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage (any input, see Notes 1 and 3)		±15	±15	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	N package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the TL044M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 85°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	680 mW	11.0 mW/°C	88°C	680 mW	275 mW
J (TL044M)	680 mW	11.0 mW/°C	88°C	680 mW	275 mW
J (TL044C)	680 mW	8.2 mW/°C	67°C	656 mW	—
N	680 mW	N/A	N/A	680 mW	—
W	680 mW	8.0 mW/°C	65°C	640 mW	200 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		1	5		1	5	mV
			Full range			6			7.5	
I_{IO}	Input offset current	V_O = 0	25°C		5	40		15	80	nA
			Full range			100			200	
I_{IB}	Input bias current	V_O = 0	25°C		50	100		100	250	nA
			Full range			250			400	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ	25°C	20	26		20	26		V
		R_L ≥ 10 kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, V_O = ±10 V	25°C	72	86		60	80		dB
			Full range	66			60			
B_1	Unity-gain bandwidth		25°C		0.5			0.5		MHz
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω	25°C	60	72		60	72		dB
			Full range	60			60			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C		30	150		30	200	μV/V
			Full range			150			200	
V_n	Equivalent input noise voltage	A_{VD} = 20 dB, B = 1 Hz, f = 1 kHz	25°C		50			50		nV/√Hz
I_{OS}	Short-circuit output current		25°C		±6			±6		mA
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0 V	25°C		250	400		250	500	μA
			Full range			400			500	
P_D	Total dissipation (four amplifiers)	No load, V_O = 0 V	25°C		7.5	12		7.5	15	mW
			Full range			12			15	

†All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for TL044M is −55°C to 125°C and for TL044C is 0°C to 70°C.

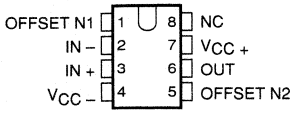
Operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TL044M			TL044C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.3			0.3		μs
	Overshoot factor				5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.5			0.5		V/μs

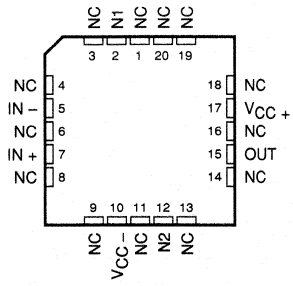
D3234, JUNE 1988 – REVISED FEBRUARY 1989

- **Maximum Offset Voltage . . . 800 μV (TL051A)**
- **High Slew Rate . . . 19.8 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 18 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE
(TOP VIEW)

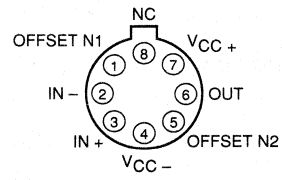


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 is in electrical contact with the case

description

The TL051 and TL051A operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

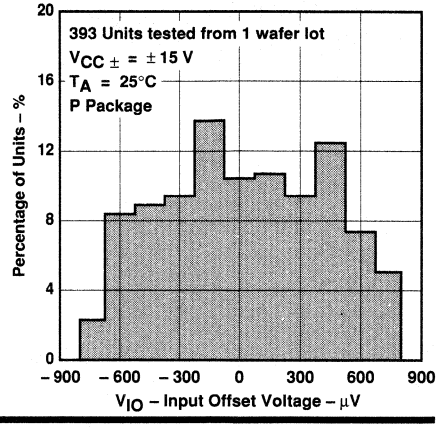
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL051 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL051 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 μV	TL051ACD	—	TL051ACJG	TL051ACL	TL051ACP
	1500 μV	TL051CD	—	TL051CJG	TL051CL	TL051CP
– 40°C to 85°C	800 μV	TL051AID	—	TL051AIJG	TL051AIL	TL051AIP
	1500 μV	TL051ID	—	TL051IJG	TL051IL	TL051IP
– 55°C to 125°C	800 μV	TL051AMD	TL051AMFK	TL051AMJG	TL051AML	TL051AMP
	1500 μV	TL051MD	TL051MFK	TL051MJG	TL051ML	TL051MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL051CDR).

DISTRIBUTION OF TL051A
INPUT OFFSET VOLTAGE



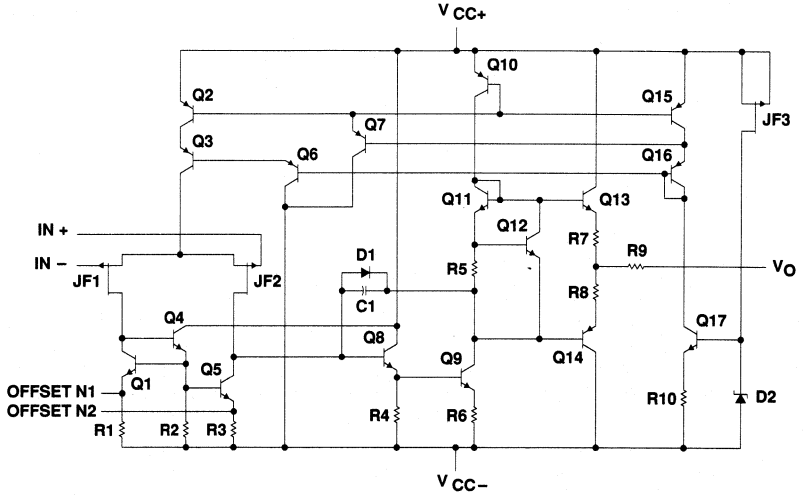
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL071 and TL081. Two offset voltage grades are available: TL051 (1.5 mV max) and TL051A (800 μV max).

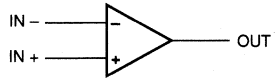
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O (each output) . . . . . ± 80 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm} = \pm 5$ V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm} = \pm 15$ V	– 11		11	– 11		11	– 11		11	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL051M	25°C		0.75	3.5		0.59	1.5	mV
				Full range			6.5			4.5	
			TL051AM	25°C		0.55	2.8		0.35	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL051M	25°C to 125°C		8			8		μV/°C
			TL051AM	25°C to 125°C		8			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		2.6	3.2		2.7	3.2	mA
				−55°C		2.3	3.2		2.4	3.2	
				125°C		2.4	3.2		2.5	3.2	

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/μs
				−55°C		17.5			20		
				125°C		15			21.2		
SR−	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				−55°C		15.1			17		
				125°C		14.8			18.2		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				−55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				−55°C		57°			61°		
				125°C		59°			62°		

† Full range is −55°C to 125°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL051I	25°C		0.75	3.5		0.59	1.5	mV
				Full range			5.3			3.3	
			TL051AI	25°C		0.55	2.8		0.35	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051I	25°C to 85°C		7			8		μV/°C
			TL051AI	25°C to 85°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		2.6	3.2		2.7	3.2	mA
				−40°C		2.4	3.2		2.6	3.2	
				85°C		2.5	3.2		2.6	3.2	

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/μs
				– 40°C		20.1		13	23		
				85°C		16.1		13	21.9		
$SR-$	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				– 40°C		16.6		13	19.4		
				85°C		15.7		13	19.1		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				– 40°C		3.5			3.6		
				85°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				– 40°C		58°			61°		
				85°C		59°			62°		

† Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL051C	25°C		0.75	3.5		0.59	1.5	mV
				Full range			4.5			2.5	
			TL051AC	25°C		0.55	2.8		0.35	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL051C	25°C to 70°C		8			8		μV/°C
			TL051AC	25°C to 70°C		8			8	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		2.6	3.2		2.7	3.2	mA
				0°C		2.7	3.2		2.8	3.2	
				70°C		2.6	3.2		2.7	3.2	

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

9. This parameter is tested on a sample basis for the TL051A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

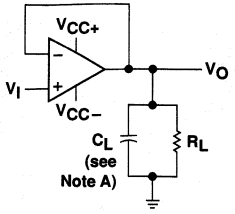
operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		18.2		15	23.7		V/μs
				0°C		19.5		13	24.1		
				70°C		16.4		13	22.6		
SR−	Negative slew rate at unity gain			25°C		16.5		15	19.8		
				0°C		16.8		13	19.9		
				70°C		16		13	19.3		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		18			18	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3.1		MHz
				0°C		3.2			3.3		
				70°C		2.7			2.8		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		59°			62°		
				0°C		58°			62°		
				70°C		59°			62°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

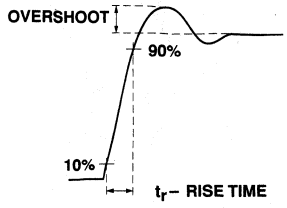


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

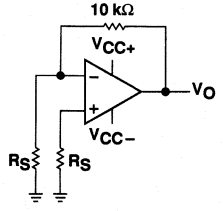
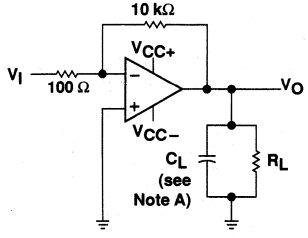


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

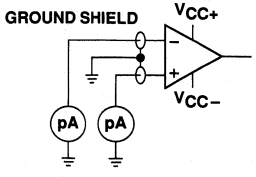


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp-bias-current level typical of the TL051 and TL051A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE

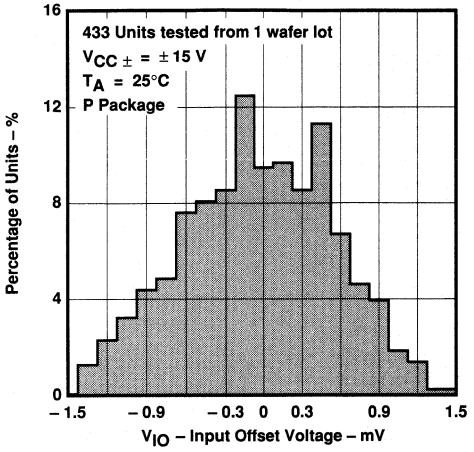


FIGURE 6

DISTRIBUTION OF TL051
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

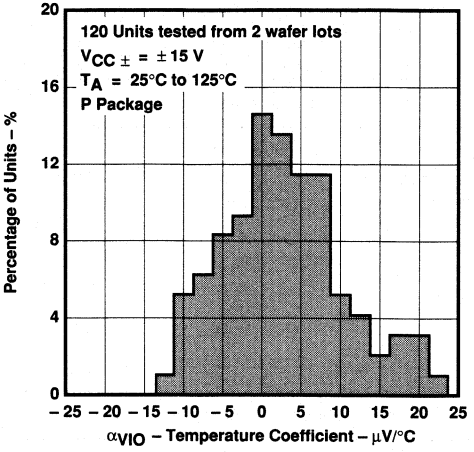


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

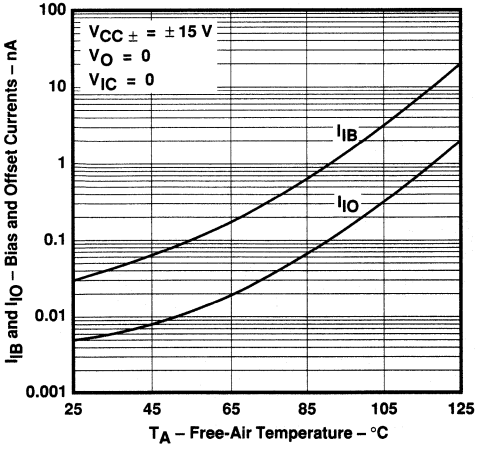


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

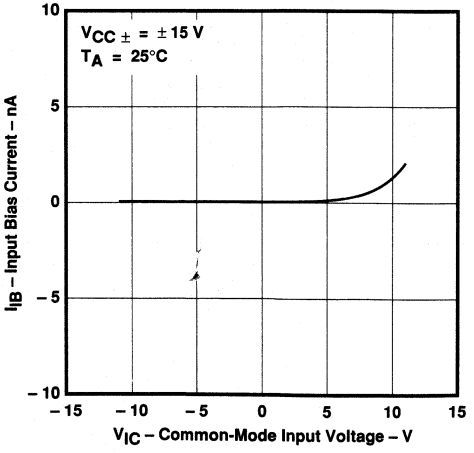


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

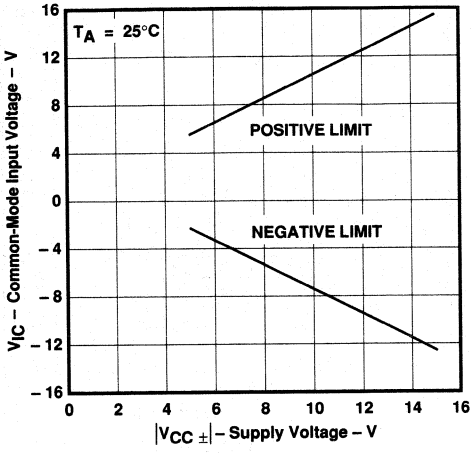


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

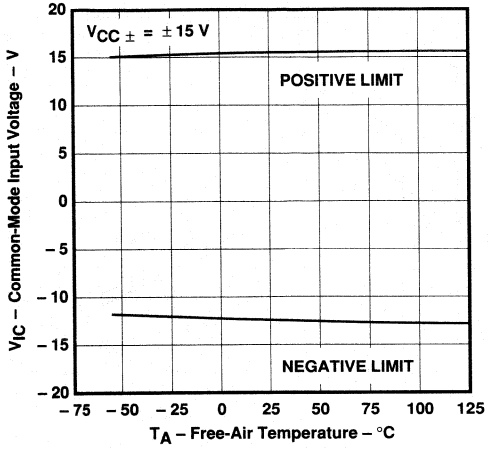


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

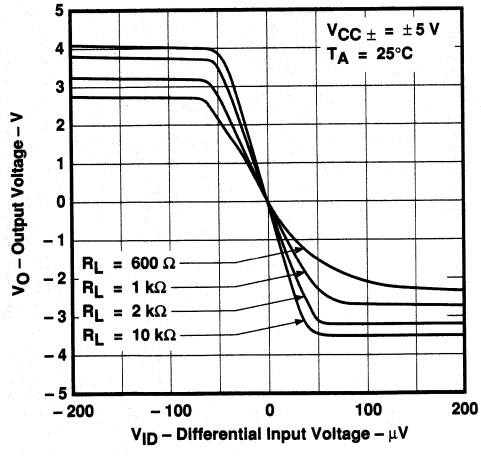


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

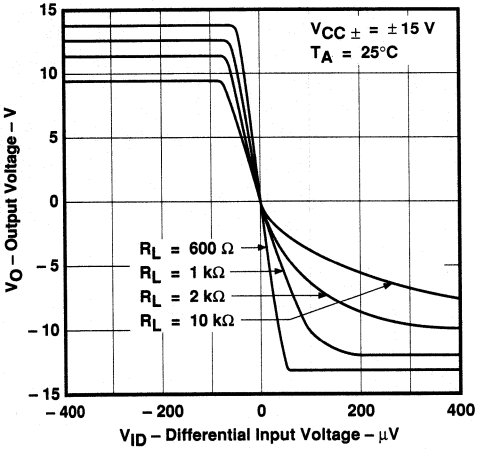


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

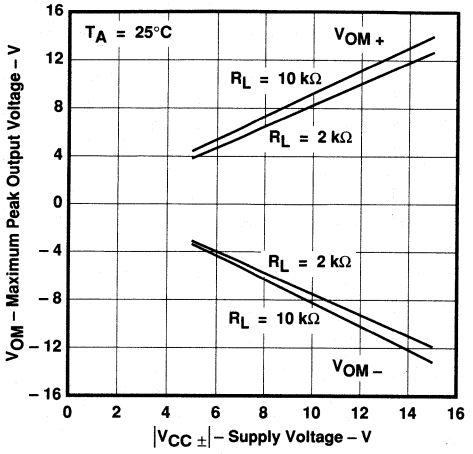


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

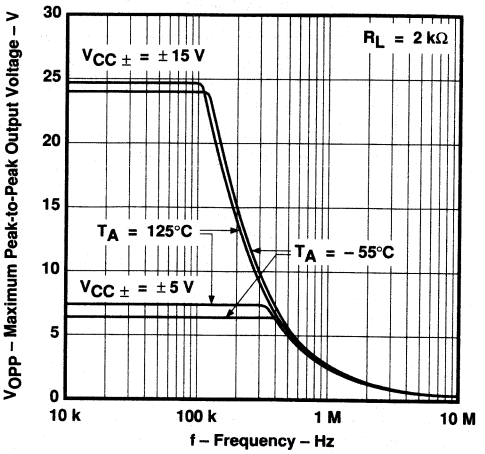


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

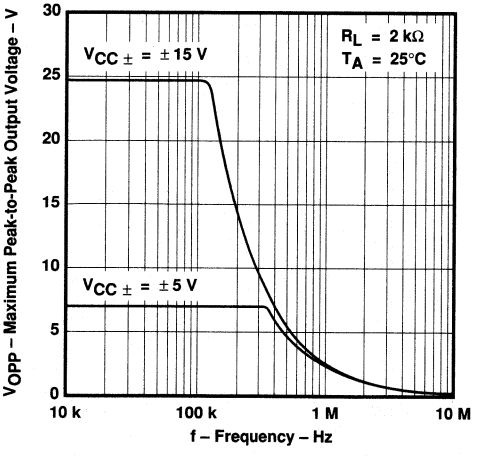


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

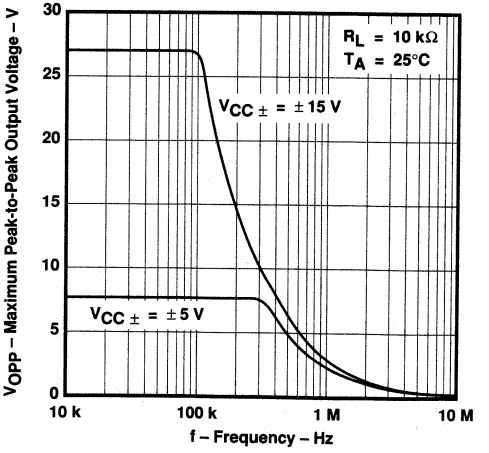


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

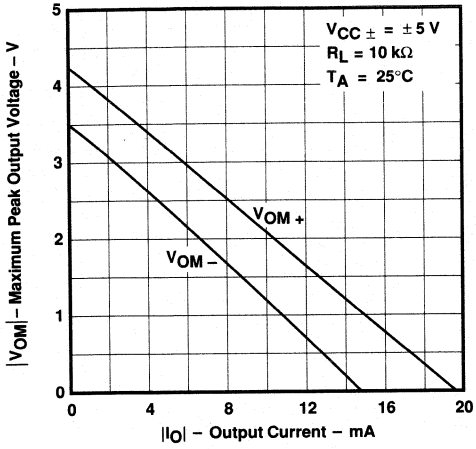


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

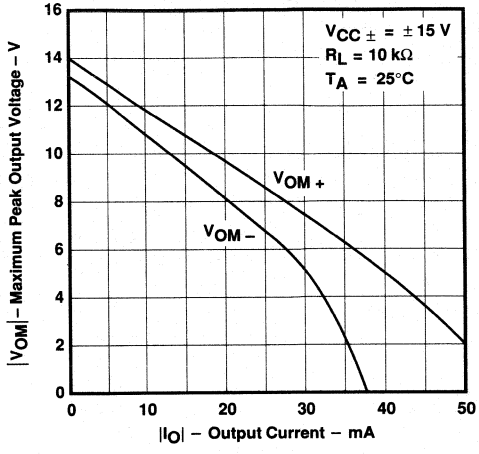


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

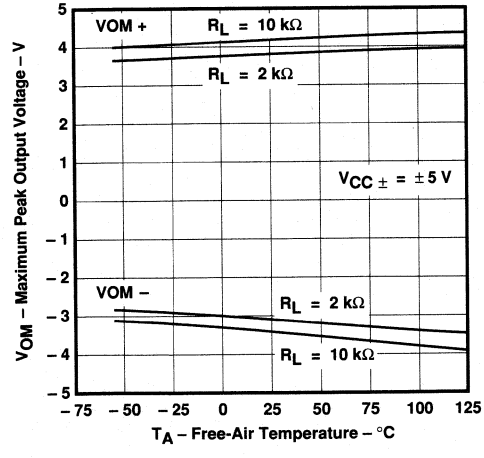


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

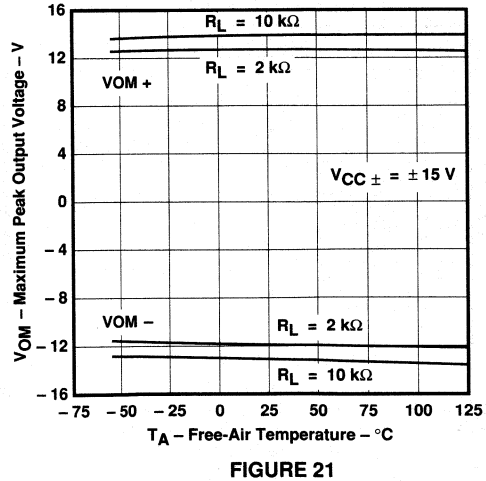


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

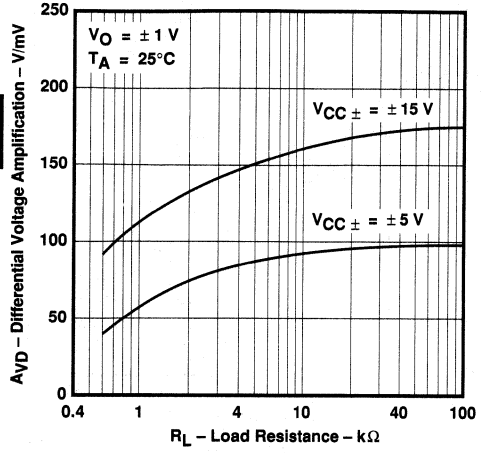


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

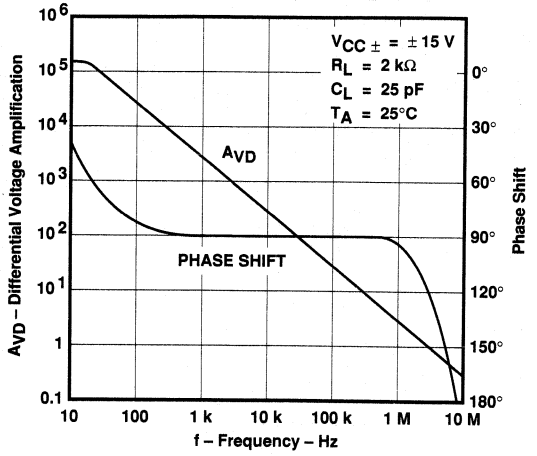


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

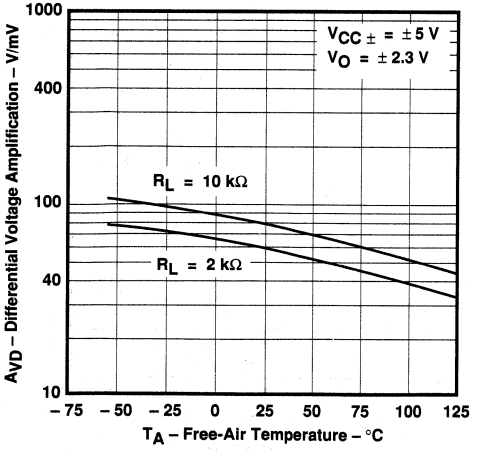


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

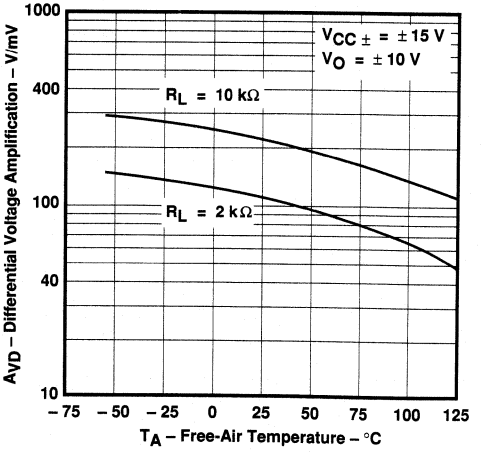


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

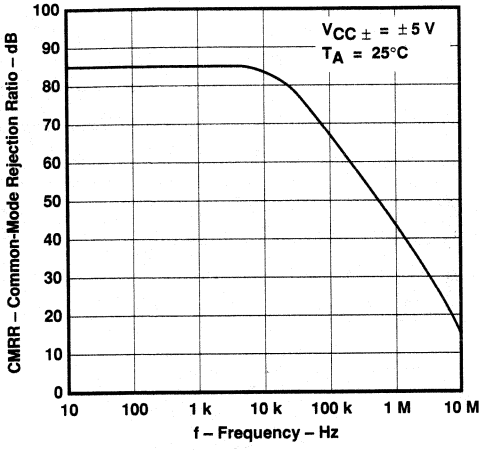


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

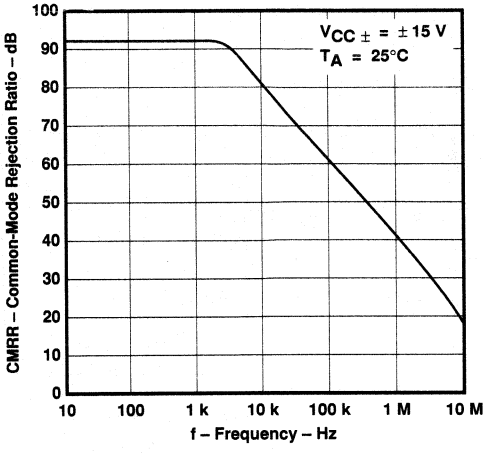


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

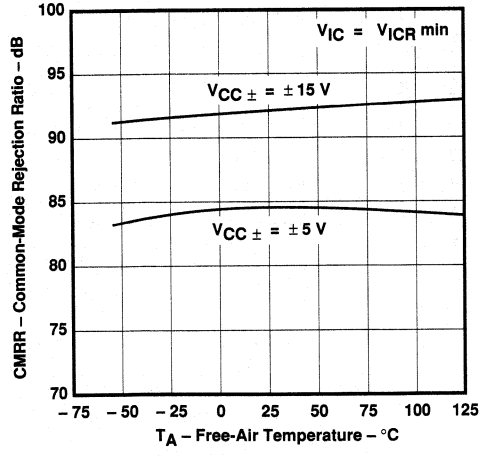


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

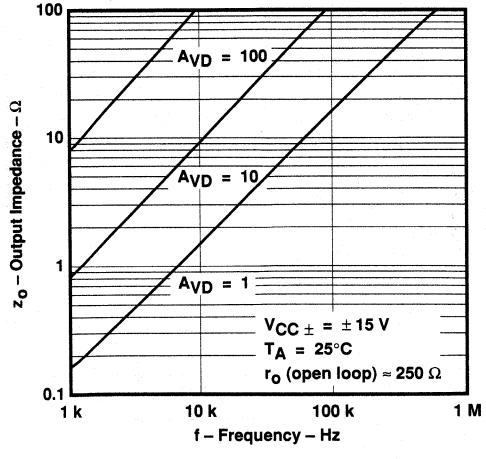


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

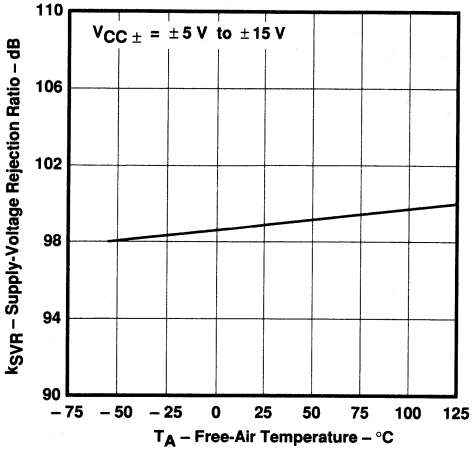


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

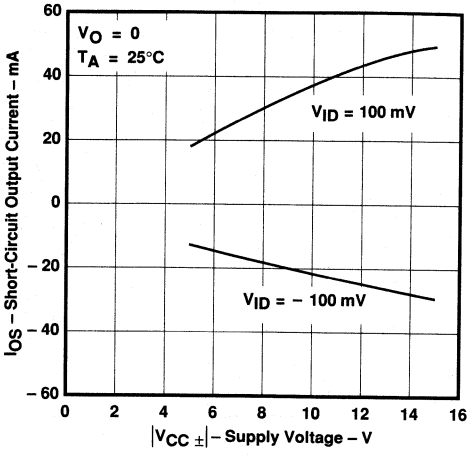


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

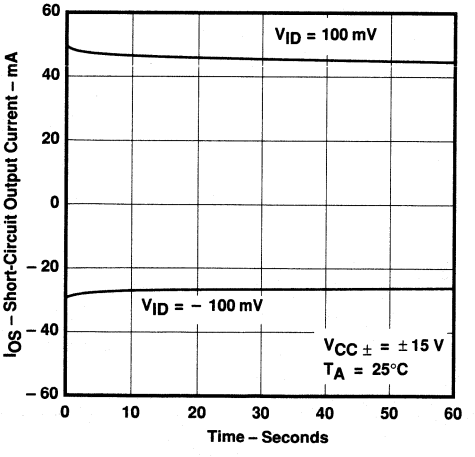


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

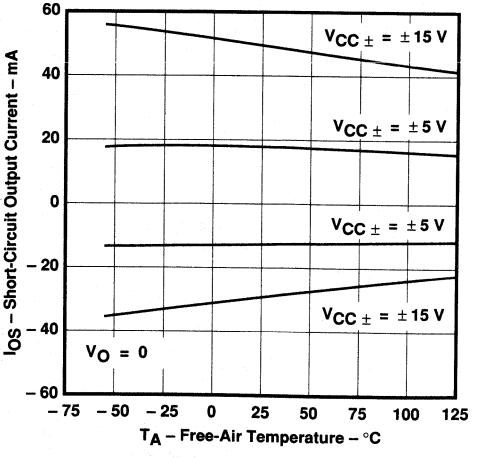


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

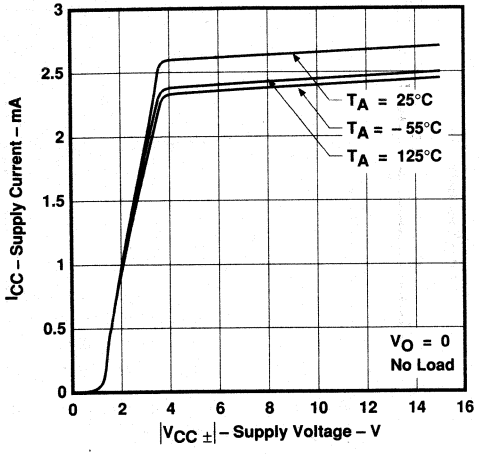


FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

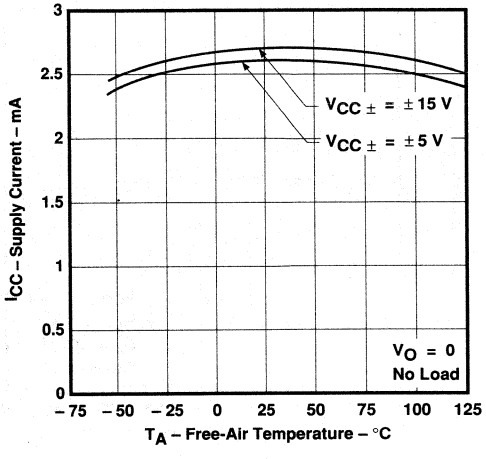


FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

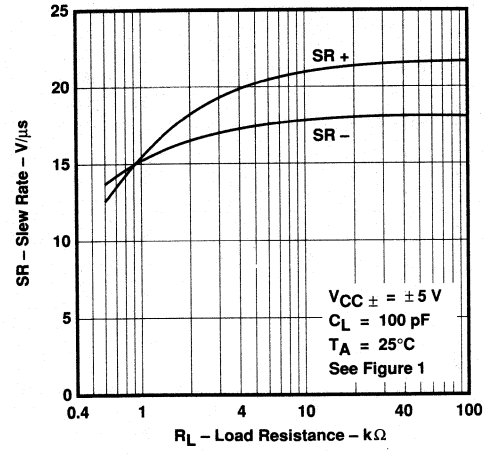


FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

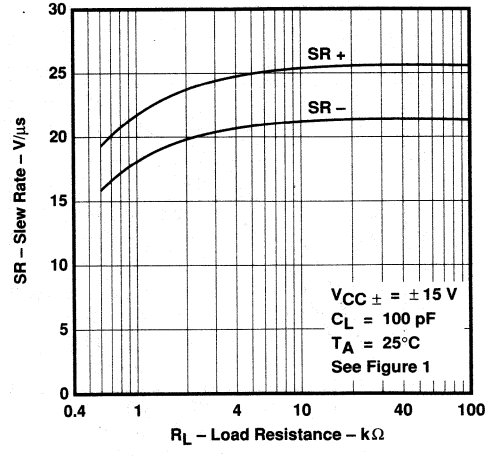


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

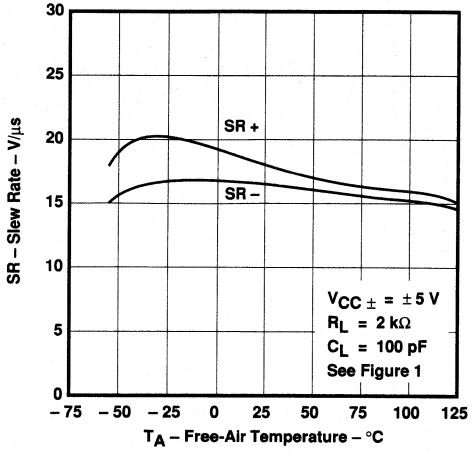


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

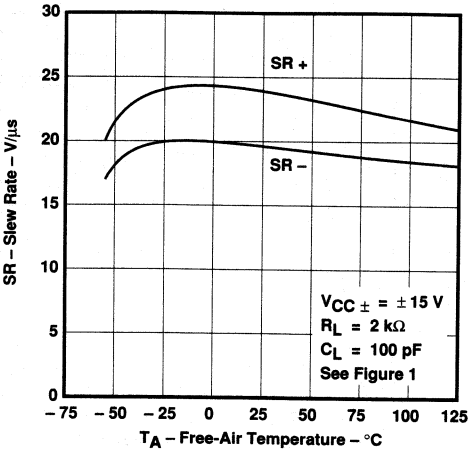


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

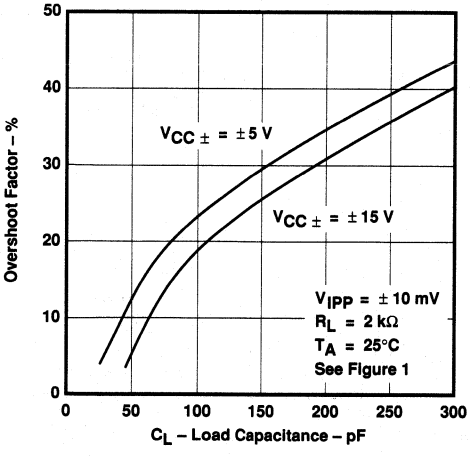


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

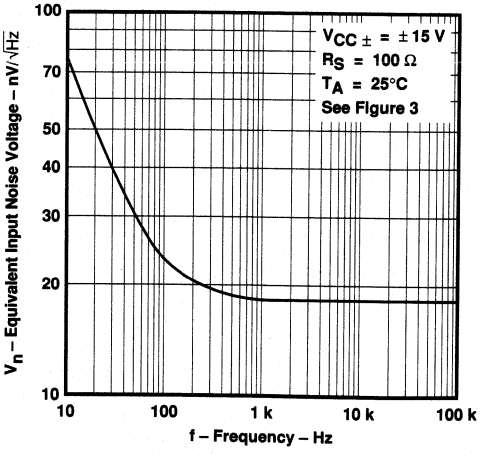


FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

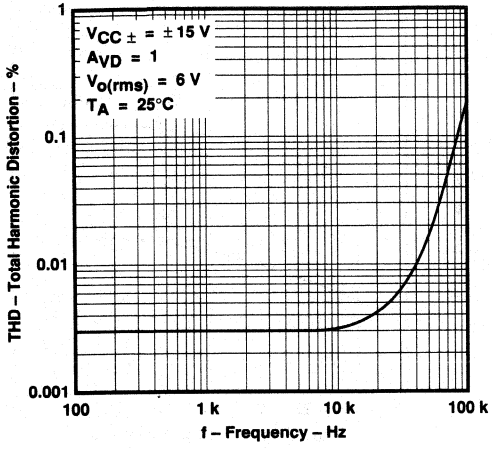


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

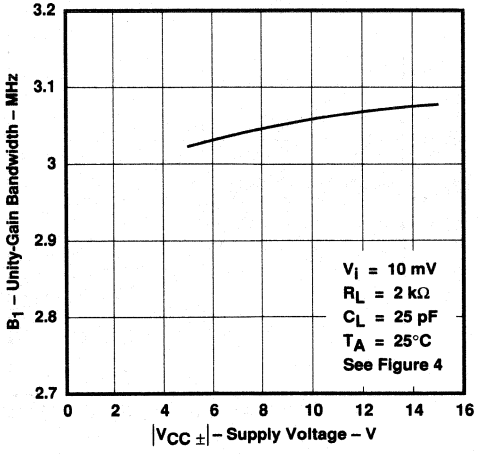


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

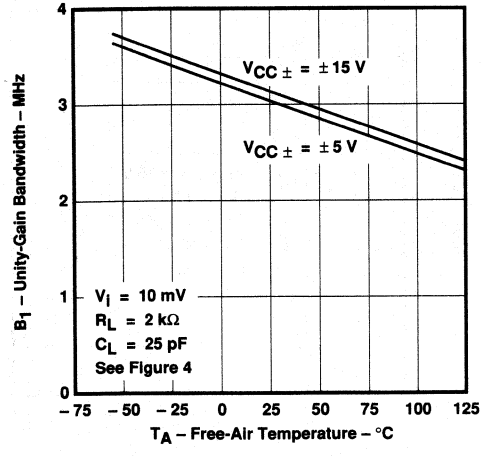


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

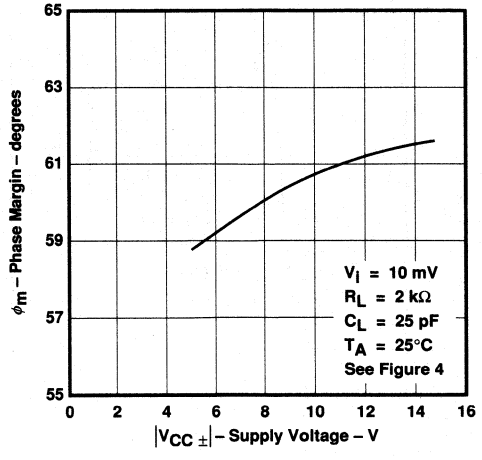


FIGURE 45

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

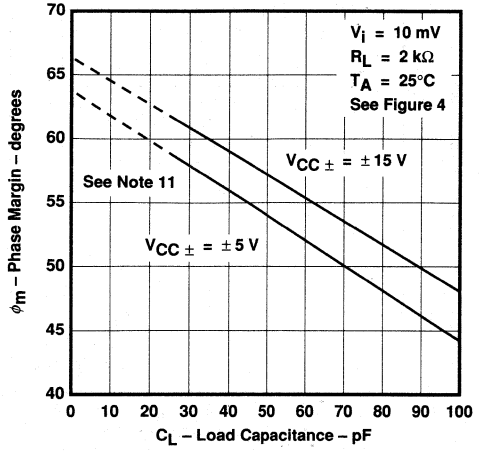


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

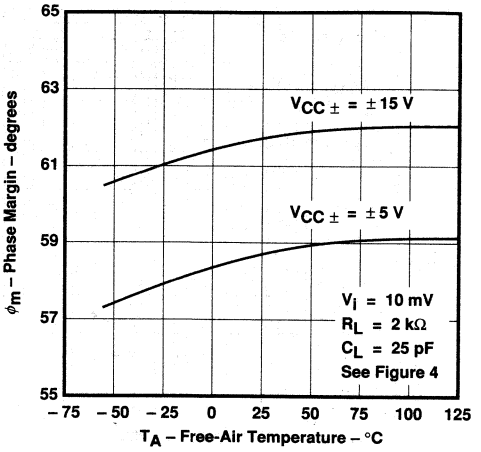


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

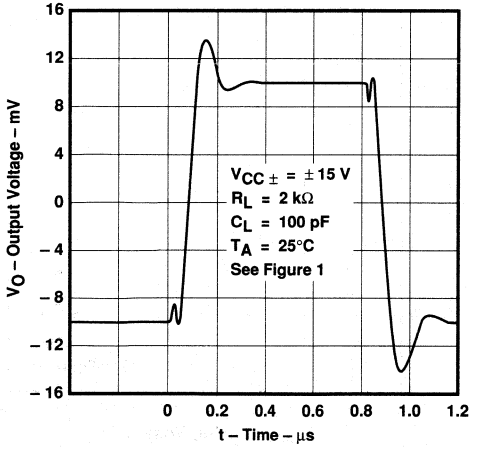


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

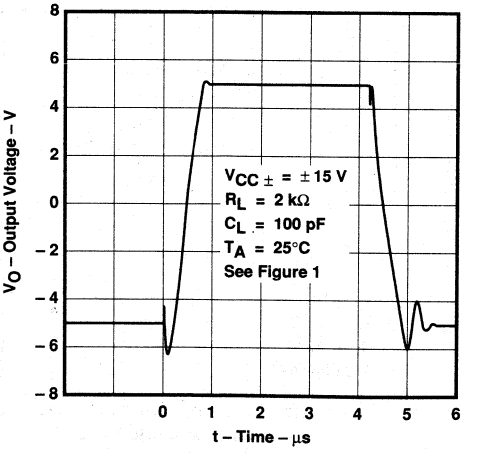


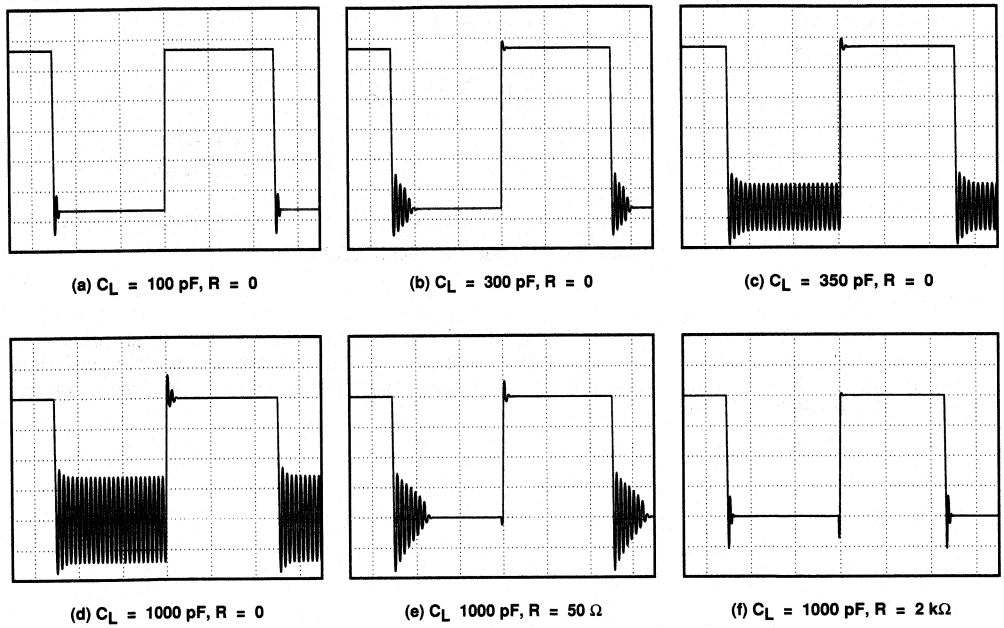
FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL APPLICATION DATA

output characteristics

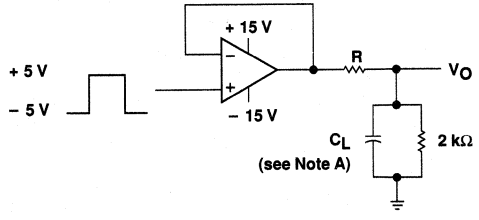
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL051 and TL051A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

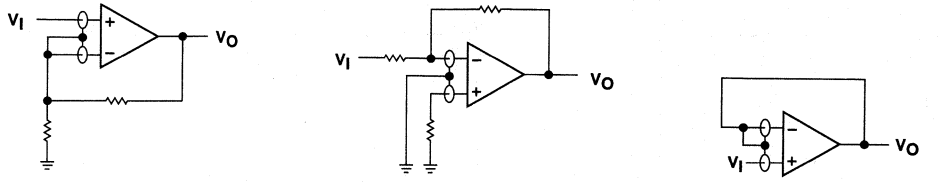
FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

TYPICAL APPLICATION DATA

input characteristics

The TL051 and TL051A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL051 and TL051A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL051 and TL051A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

TYPICAL APPLICATION DATA

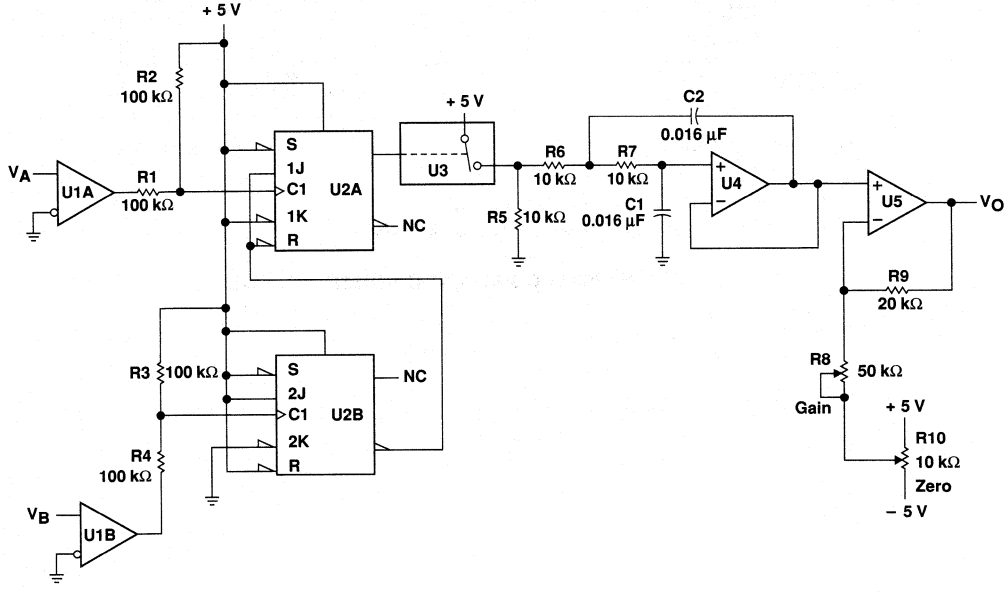
ɔhase meter

The phase meter in Figure 53 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5-V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flop.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL051 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U2A approximates a square wave, and U4 has an output of almost 2.5 V. U5 acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0- to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4,U5 = TL051; $V_{CC\pm}$ = ±5 V.

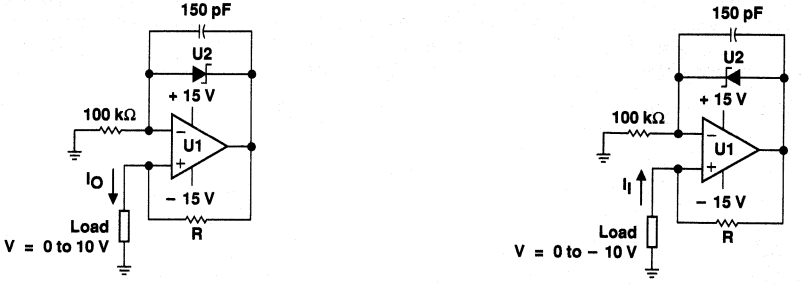
FIGURE 53. PHASE METER

TYPICAL APPLICATION DATA

precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL051. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) SOURCE CURRENT LOAD

(b) SINK CURRENT LOAD

NOTES: U1 = TL051.
U2 = LM385, LT1004, or LT1009 voltage reference.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

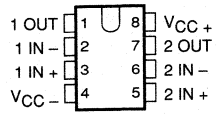
FIGURE 54. PRECISION CONSTANT-CURRENT SOURCE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

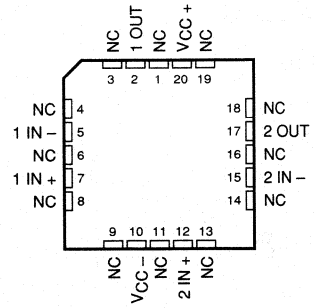
D3235, JUNE 1988 – REVISED FEBRUARY 1989

- **Maximum Offset Voltage . . . 800 μV (TL052A)**
- **High Slew Rate . . . 17.8 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 19 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**

D, JG, or P PACKAGE
(TOP VIEW)

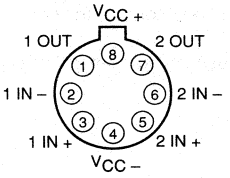


FK PACKAGE
(TOP VIEW)



NC – No internal connection

L PACKAGE
(TOP VIEW)



Pin 4 is in electrical contact with the case

Description

The TL052 and TL052A dual operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

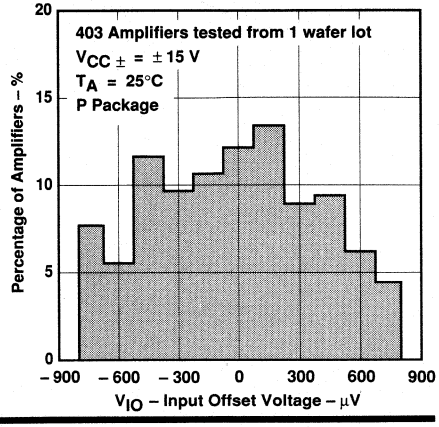
This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL052 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL052 has been

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE				
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	800 μV	TL052ACD	—	TL052ACJG	TL052ACL	TL052ACP
	1500 μV	TL052CD	—	TL052CJG	TL052CL	TL052CP
– 40°C to 85°C	800 μV	TL052AID	—	TL052AIJG	TL052AIL	TL052AIP
	1500 μV	TL052ID	—	TL052IJG	TL052IL	TL052IP
– 55°C to 125°C	800 μV	TL052AMD	TL052AMFK	TL052AMJG	TL052AML	TL052AMP
	1500 μV	TL052MD	TL052MFK	TL052MJG	TL052ML	TL052MP

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL052CDR).

DISTRIBUTION OF TL052A
INPUT OFFSET VOLTAGE



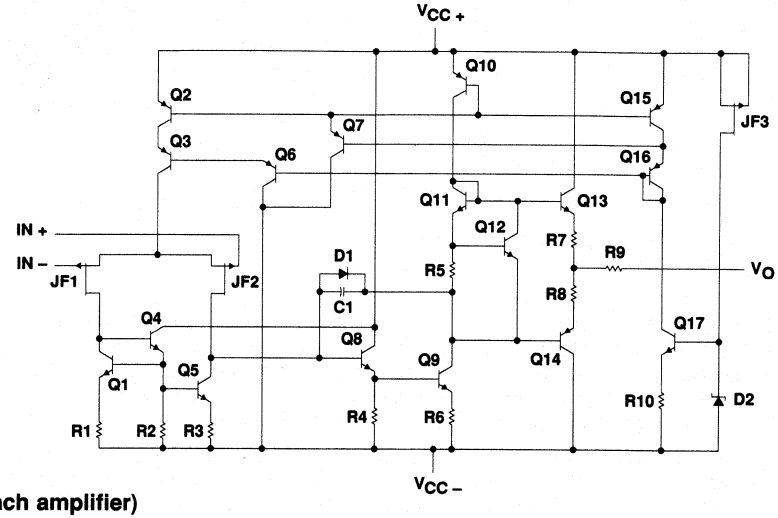
description (continued)

designed to be functionally compatible, as well as pin compatible, with the TL072 and TL082. Two offse voltage grades are available: TL052 (1.5 mV max) and TL052A (800 μV max).

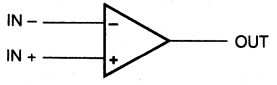
A variety of available packaging options includes small-outline and chip carrier versions for high-densit system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C t 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices ar characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



TEXAS INSTRUMENTS
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bsolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O (each output) . . . . . ± 80 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C

OTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	825 mW	6.6 mW/°C	528 mW	429 mW	165 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

ecommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			± 5	± 15		± 5	± 15		± 5	± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V		– 1	4		– 1	4		– 1	4	V
	$V_{CC\pm}$ = ± 15 V		– 11	11		– 11	11		– 11	11	
Operating free-air temperature, T_A			– 55	125		– 40	85		0	70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL052M	25°C		0.73	3.5		0.65	1.5	mV
				Full range			6.5			4.5	
			TL052AM	25°C		0.51	2.8		0.4	0.8	
				Full range			5.8			3.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL052M	25°C to 125°C		10			9		μV/°C
			TL052AM	25°C to 125°C		9			8		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				−55°C	30	76		60	149		
				125°C	10	32		15	49		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		4.6	5.6		4.8	5.6	mA
				−55°C		4.4	6.4		4.5	6.4	
				125°C		4.2	6.4		4.4	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

›perating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/μs
				−55°C		18.8			20.3		
				125°C		14.5			20.2		
SR−	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				−55°C		15.7			17.6		
				125°C		13.8			16.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				−55°C		3.6			3.7		
				125°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				−55°C		57°			61°		
				125°C		60°			63°		

Full range is −55°C to 125°C.

OTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL052I	25°C		0.73	3.5		0.65	1.5	mV
				Full range			5.3			3.3	
			TL052AI	25°C		0.51	2.8		0.4	0.8	
				Full range			4.6			2.6	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052I	25°C to 85°C		7			6		μV/°C
			TL052AI	25°C to 85°C		6			6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				−40°C	30	74		60	145		
				85°C	20	43		30	76		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				−40°C	65	83		75	90		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−40°C	75	98		75	98		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		4.6	5.6		4.8	5.6	mA
				−40°C		4.5	6.4		4.7	6.4	
				85°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/μs
				– 40°C		18.8		11	20.6		
				85°C		16		11	20.7		
$SR-$	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				– 40°C		16		11	17.8		
				85°C		14.5		11	17.2		
t_r	Rise time	V_{IPP} = ± 10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				– 40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				– 40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				– 40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				– 40°C		3.5			3.6		
				85°C		2.5			2.6		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				– 40°C		58°			61°		
				85°C		60°			63°		

Full range is – 40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL052C	25°C		0.73	3.5		0.65	1.5	mV
				Full range			4.5			2.5	
			TL052AC	25°C		0.51	2.8		0.4	0.8	
				Full range			3.8			1.8	
α_{VIO}	Temperature coefficient of input offset voltage (see Note 9)		TL052C	25°C to 70°C		8			8		µV/°C
			TL052AC	25°C to 70°C		8			6	25	
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	59		50	105		V/mV
				0°C	30	65		60	129		
				70°C	20	46		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	85		75	93		dB
				0°C	65	84		75	92		
				70°C	65	84		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				0°C	75	98		75	98		
				70°C	75	97		75	97		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		4.6	5.6		4.8	5.6	mA
				0°C		4.7	6.4		4.8	6.4	
				70°C		4.4	6.4		4.6	6.4	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolate to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

9. This parameter is tested on a sample basis for the TL052A. For other test requirements, please contact the factory. This statemer has no bearing on testing or nontesting of other parameters.

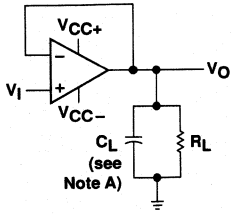
operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		17.8		13	20.7		V/μs
				0°C		18.5		11	20.9		
				70°C		16.5		11	20.8		
SR−	Negative slew rate at unity gain			25°C		15.4		13	17.8		
				0°C		15.7		11	18.5		
				70°C		14.7		11	16.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 10)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		71			71		nV/√Hz
			f = 1 kHz	25°C		19			19	30	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		3			3		MHz
				0°C		3.2			3.2		
				70°C		2.6			2.7		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		60°			63°		
				0°C		59°			63°		
				70°C		60°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{O(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{O(rms)}$ = 6 V.
10. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

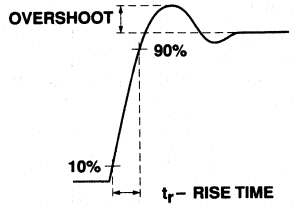


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

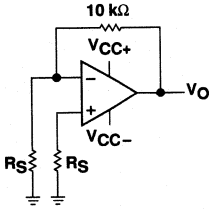
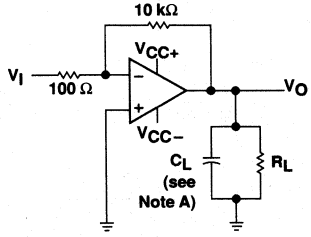


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

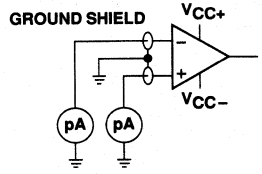


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp-bias-current level typical of the TL052 and TL052A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

ıble of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE

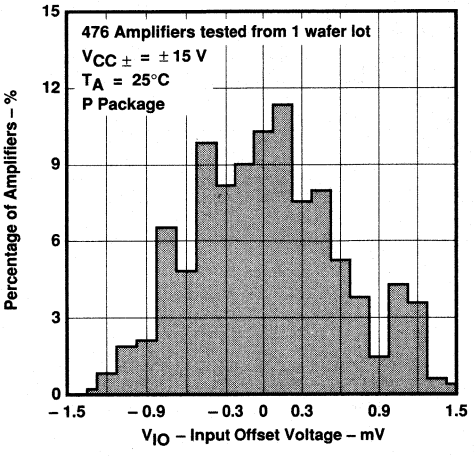


FIGURE 6

DISTRIBUTION OF TL052
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

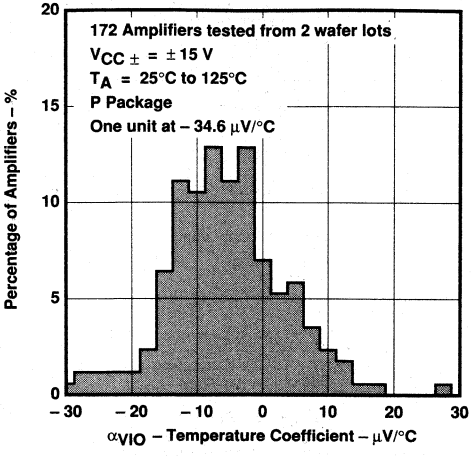


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

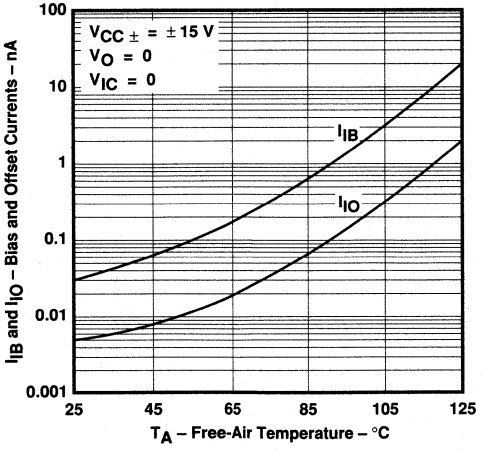


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

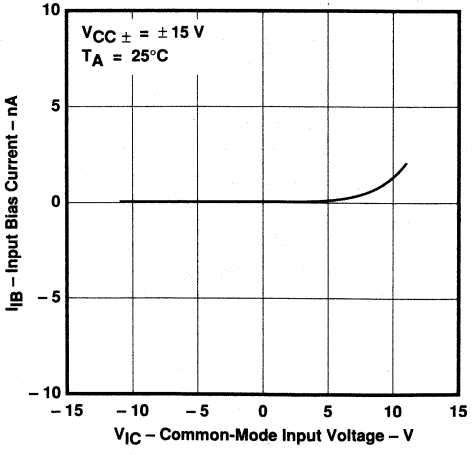


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

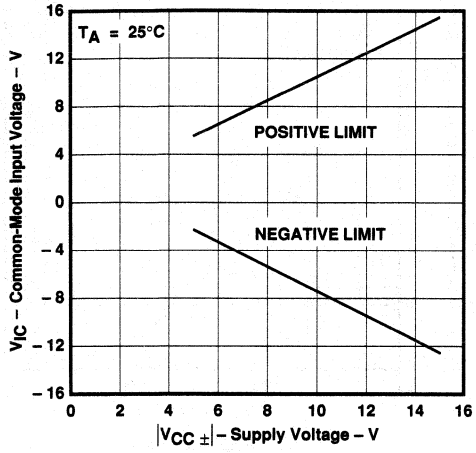


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

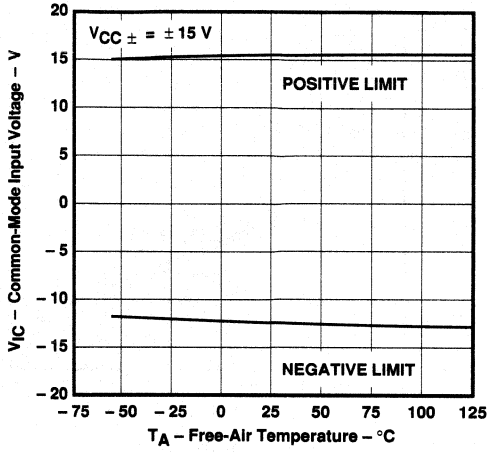


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

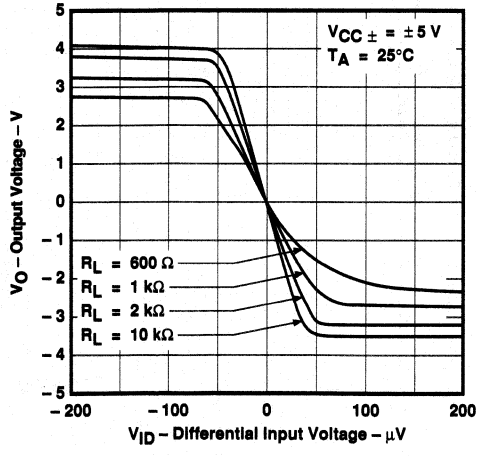


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

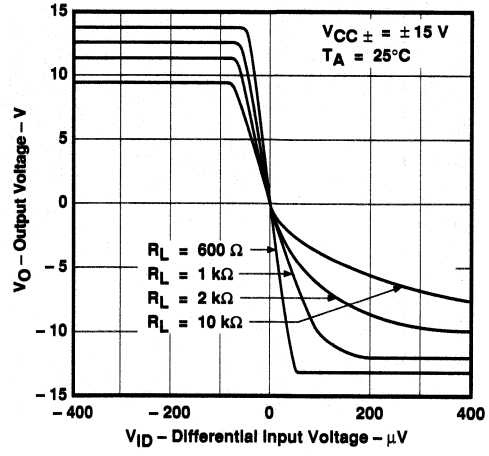


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

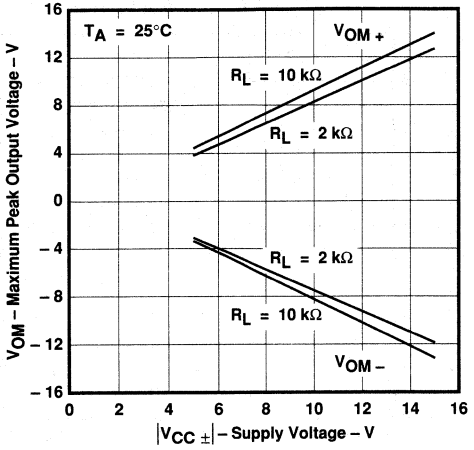


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

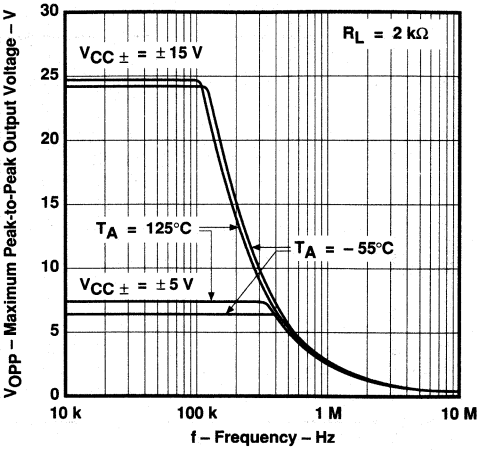


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

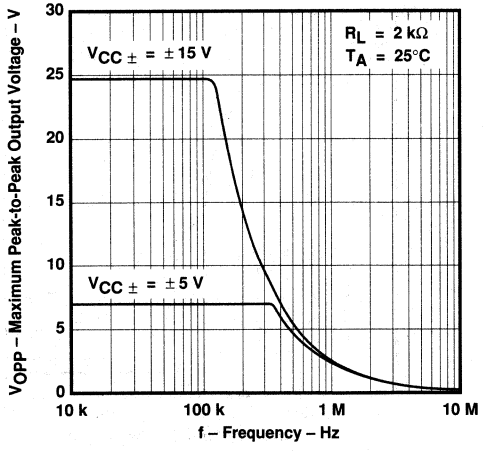


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

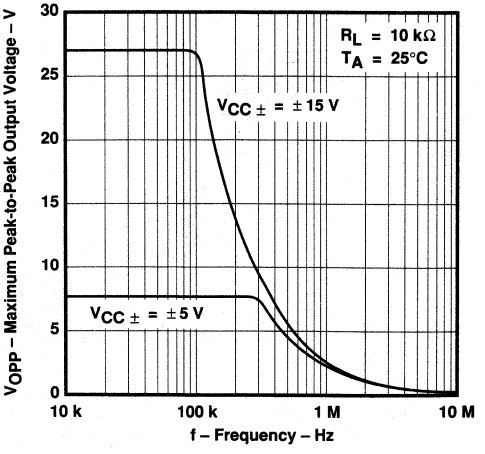


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

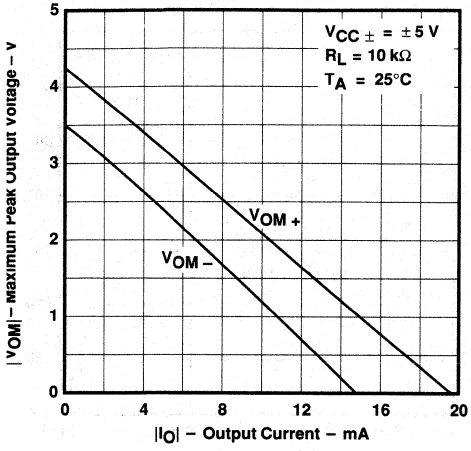


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

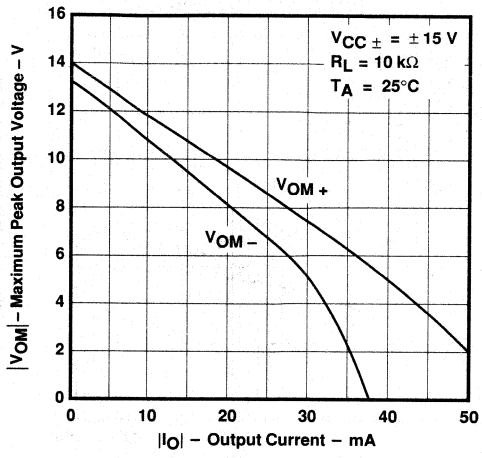


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

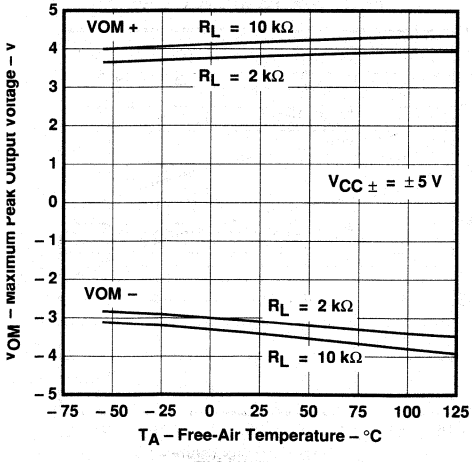


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

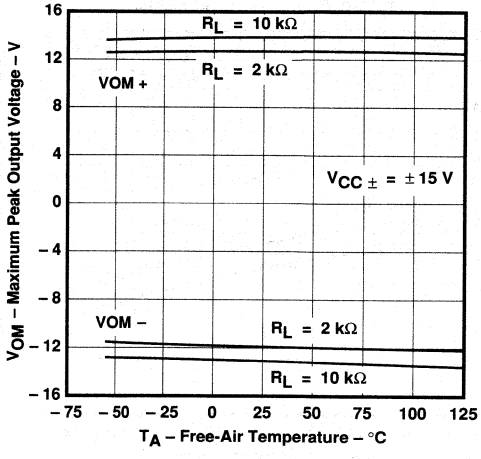


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

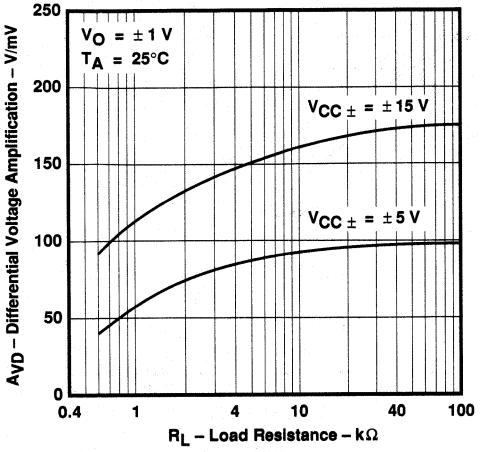


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

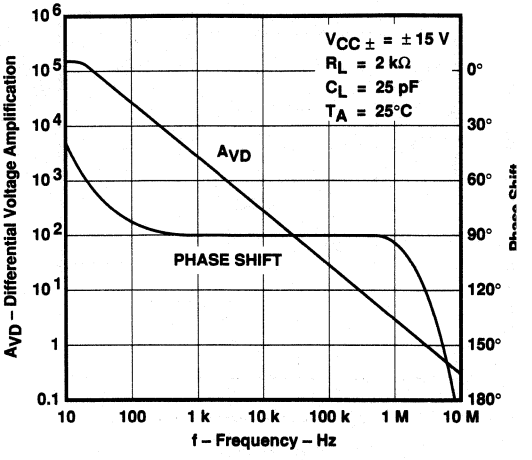


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

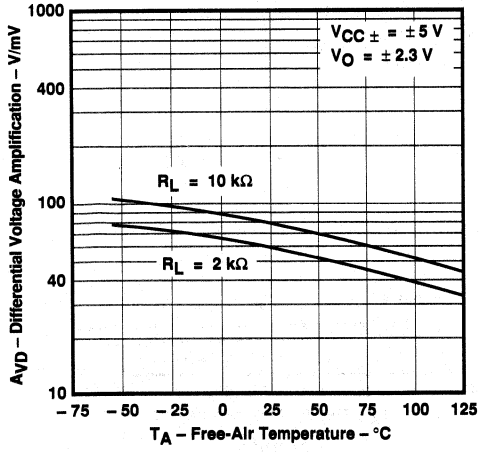


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

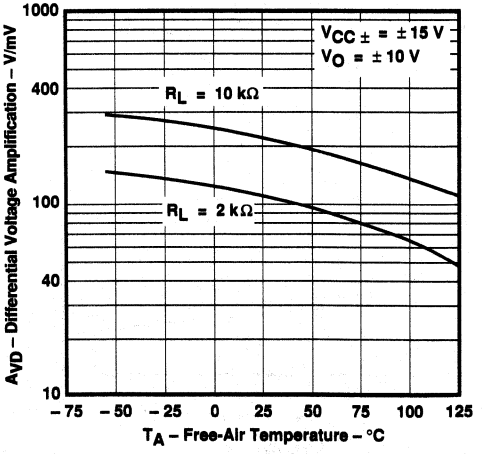


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

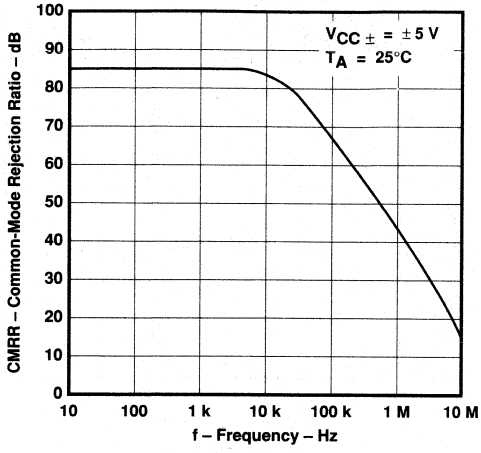

FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

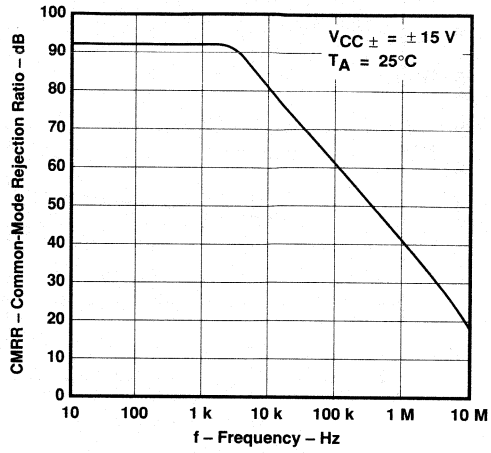

FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

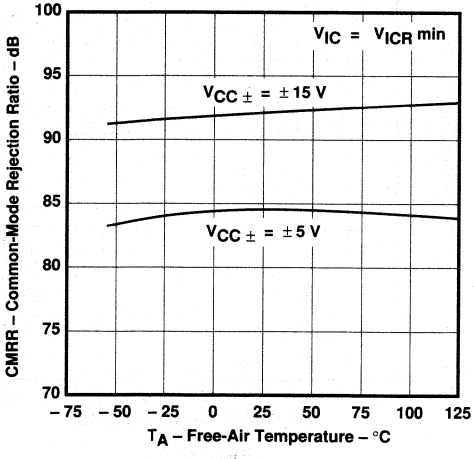

FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

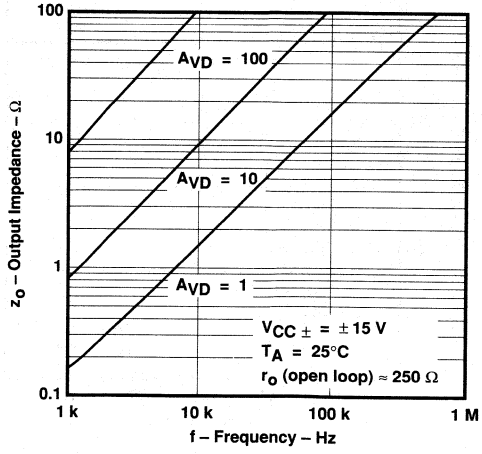

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

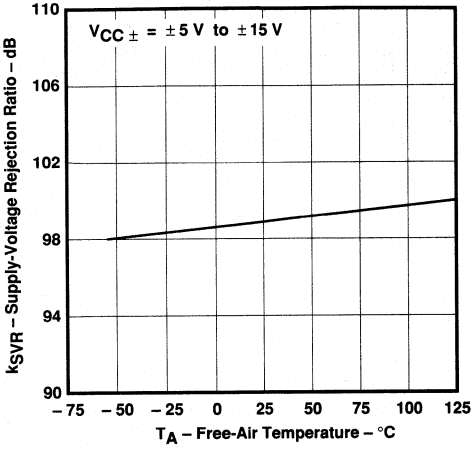

FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

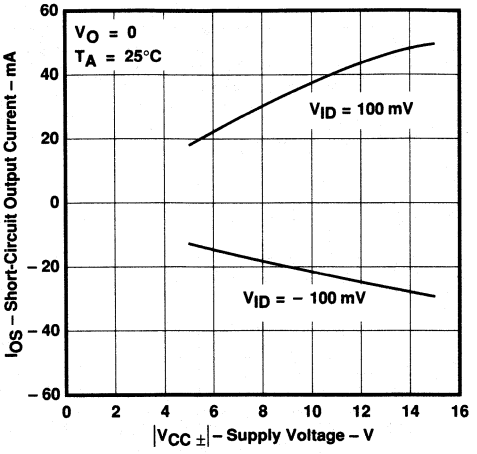

FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

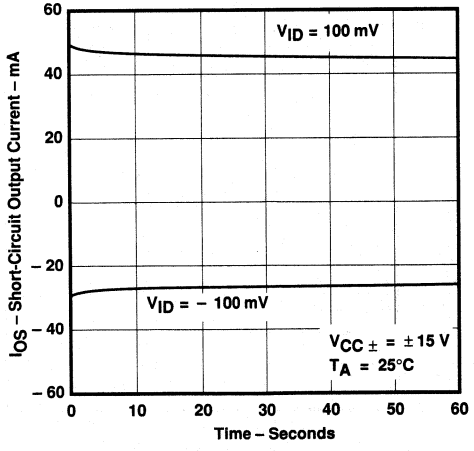

FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

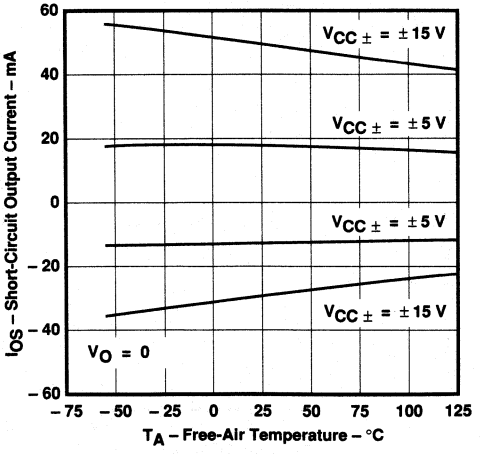

FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

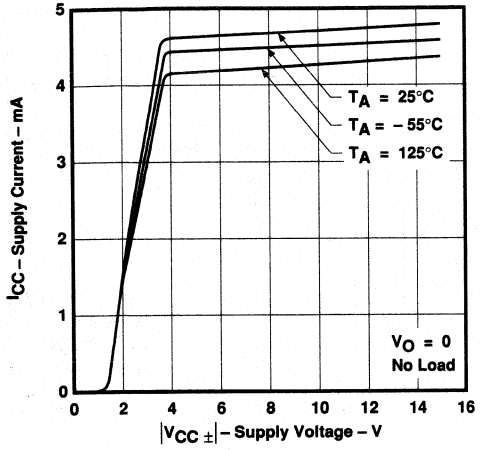

FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

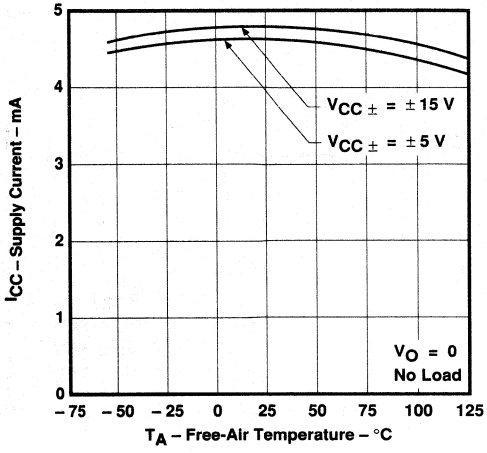

FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

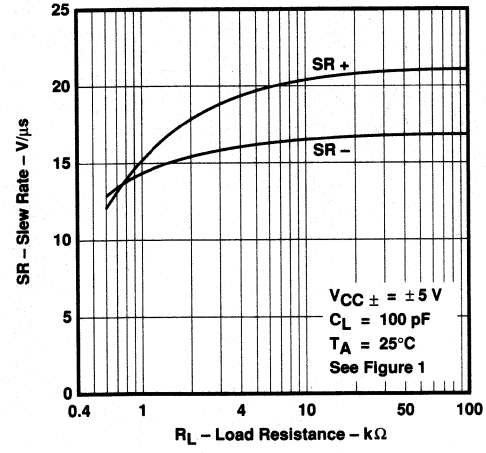

FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

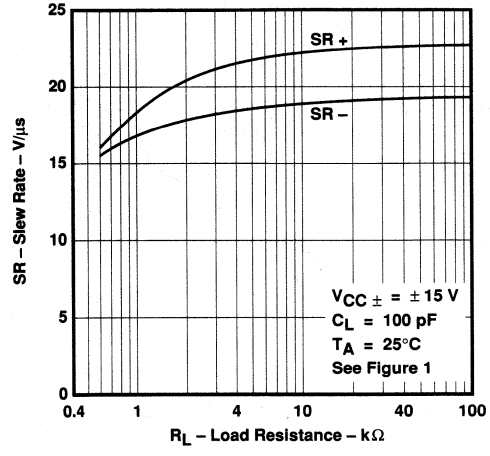

FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

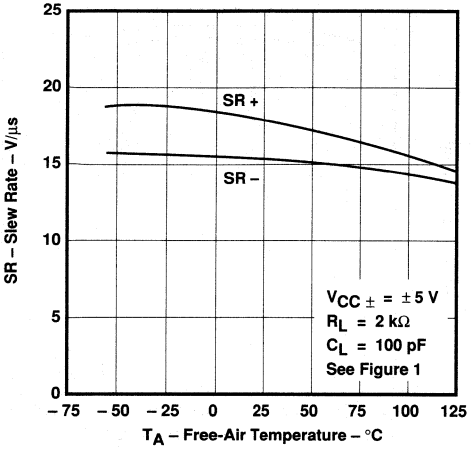

FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

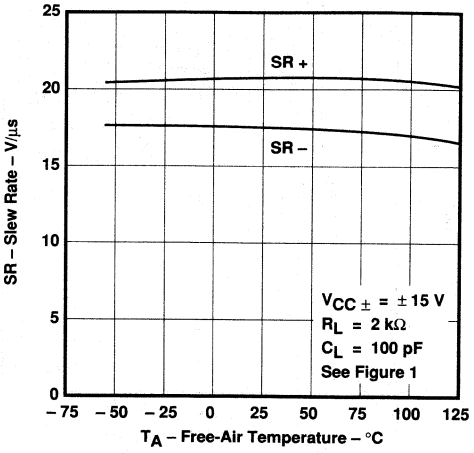

FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

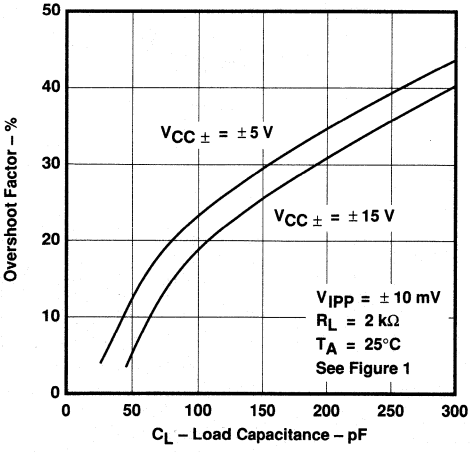

FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

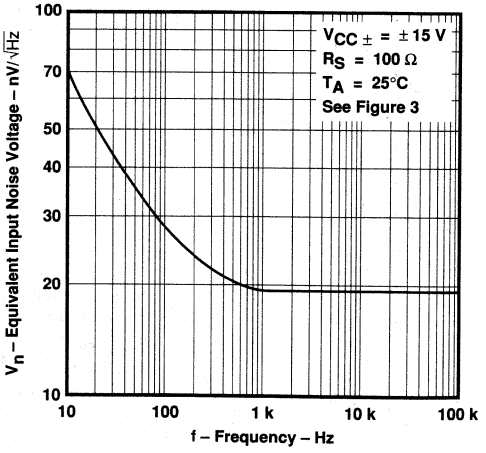

FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

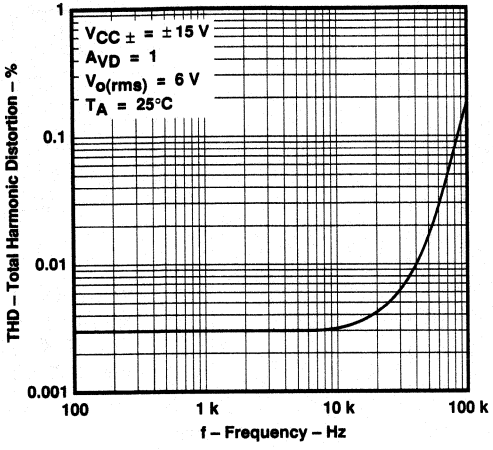

FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

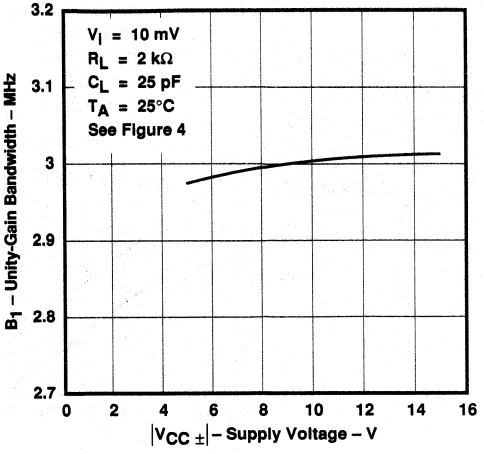

FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

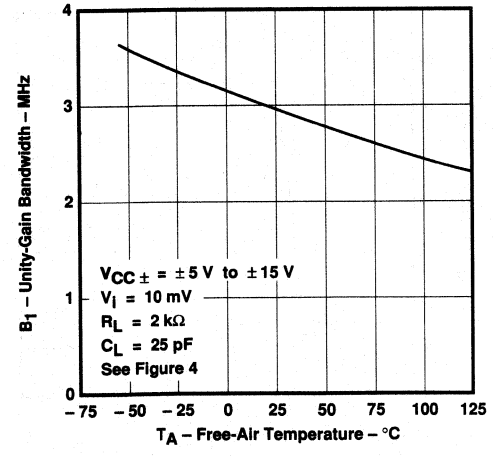

FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

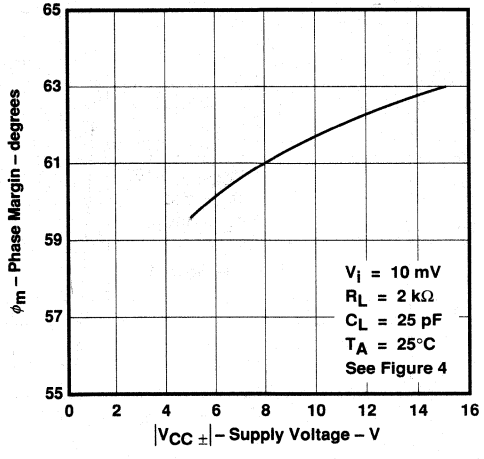

FIGURE 45

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

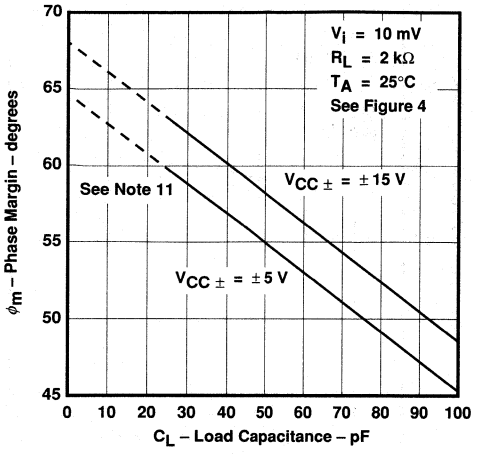

FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

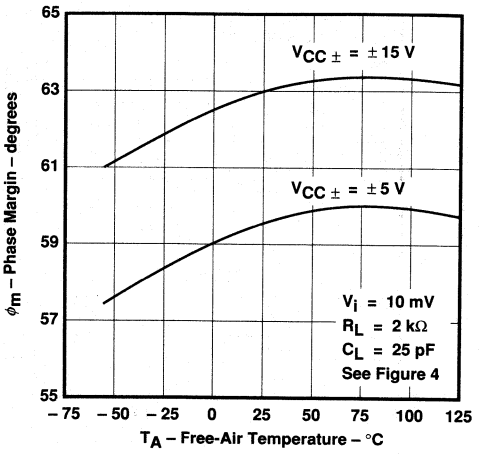

FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

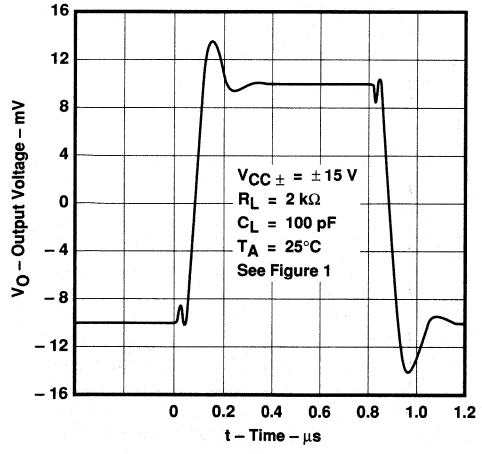

FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

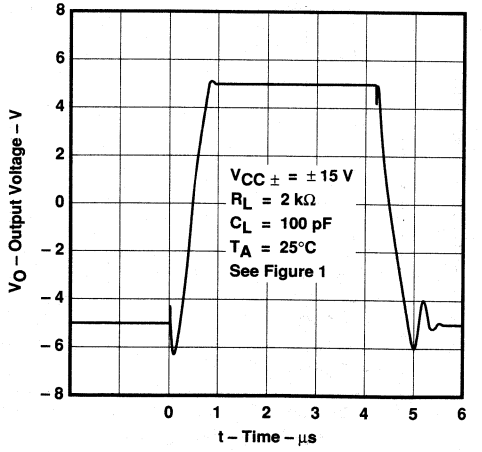

FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TEXAS INSTRUMENTS
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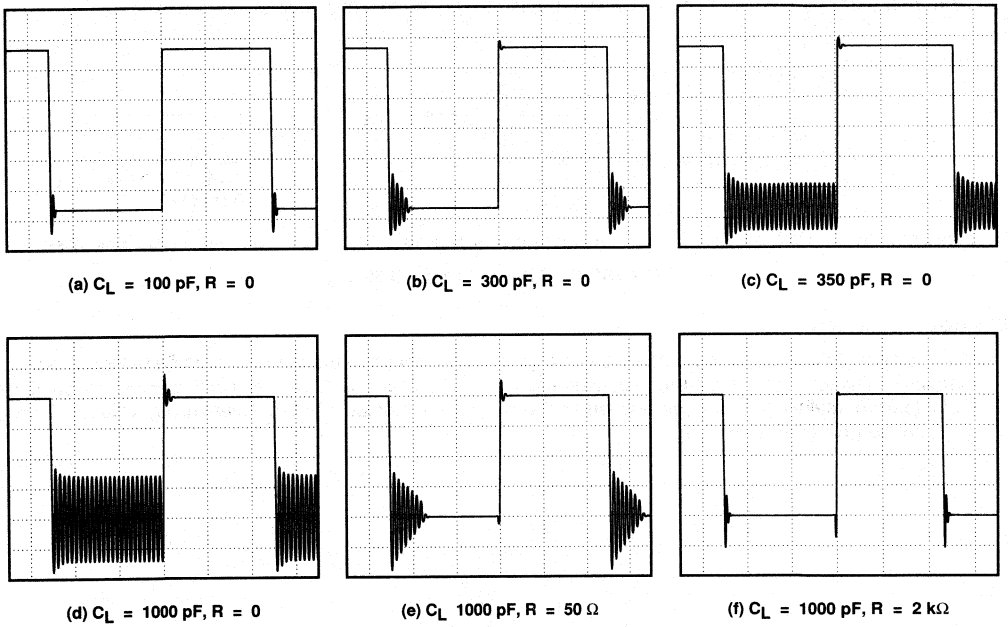
TYPICAL APPLICATION DATA

Output characteristics

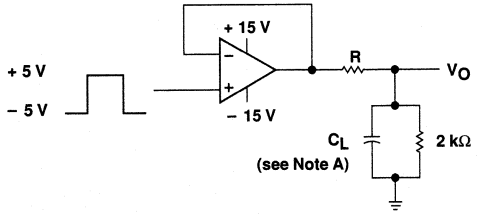
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL052 and TL052A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

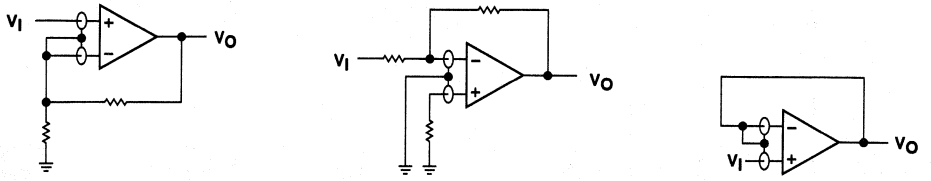
TYPICAL APPLICATION DATA

input characteristics

The TL052 and TL052A are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL052 and TL052A are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from a low impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TL052 and TL052A result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

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TYPICAL APPLICATION DATA

ıstrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL052A. Amplifiers U1A, U1B, and U2A form the actual instrumentation amplifier, while U2B provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

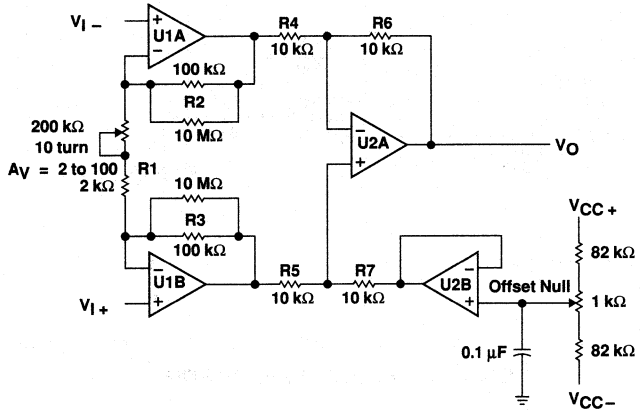
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U2B is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL052A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE: U1A through U2B = TL052A; $V_{CC\pm}$ = ± 15 V.

FIGURE 53. INSTRUMENTATION AMPLIFIER

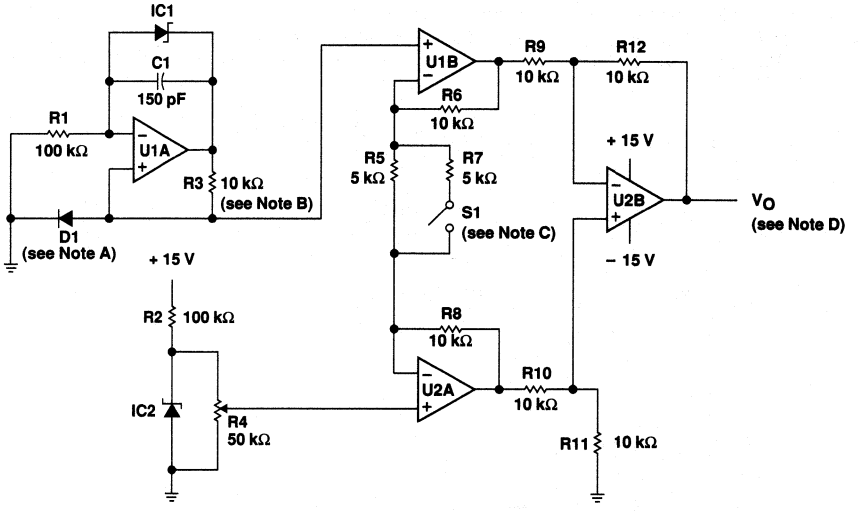
TYPICAL APPLICATION DATA

analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precis analog thermometer can be built (see Figure 54). Amplifier U1A and IC1 establish a constant current throug the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL052 must use sp supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference s by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperatur Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remair constant.

Amplifiers U1B, U2A, and U2B form the instrumentation amplifier that converts the difference between th diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifi gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, th amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degre (C or F).



NOTES: A. Temperature sensing diode ≈ (– 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. V_O ∝ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A through U2B = TL052. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 54. ANALOG THERMOMETER

TYPICAL APPLICATION DATA

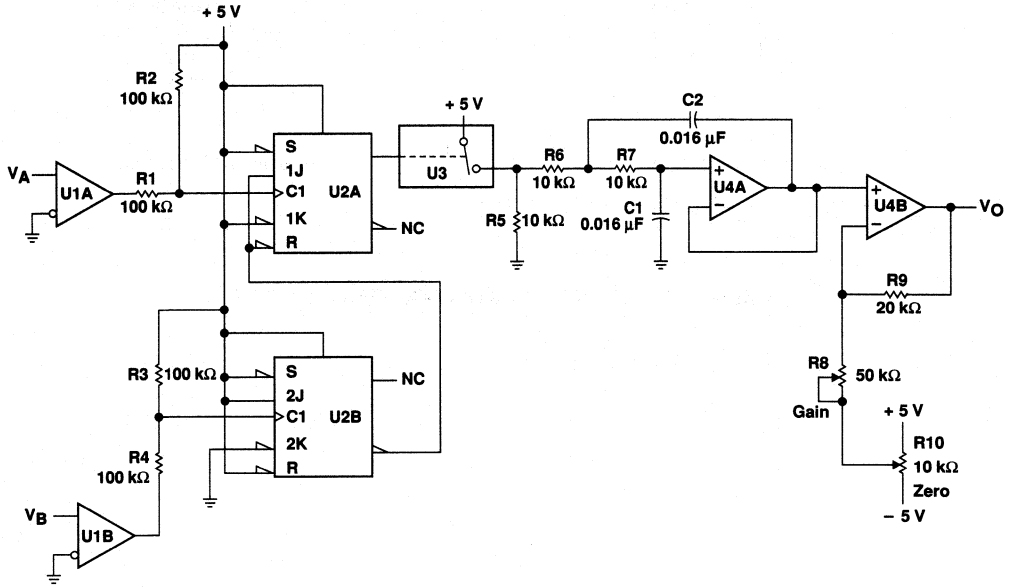
phase meter

The phase meter in Figure 55 produces an output voltage of 10 mV per degree of phase delay between the two input signals V_A and V_B. The reference signal V_A must be the same frequency as V_B. The TLC3702 comparators (U1) convert these two input sine waves into ± 5 V square waves. Then R1 and R4 provide level shifting prior to the SN74HC109 dual J-K flip flops.

Flip-flop U2B is connected as a toggle flip-flop and generates a square wave at half the frequency of V_B. Flip-flop U2A also produces a square wave at half the input frequency. The pulse duration of U2A varies from zero to half the period, where zero corresponds to zero phase delay between V_A and V_B, and half the period corresponds to V_B lagging V_A by 360 degrees.

The output pulse from U2A causes the TLC4066 (U3) switch to charge the TL052 (U4) integrator capacitors C1 and C2. As the phase delay approaches 360 degrees, the output of U4A approximates a square wave, and U2A has an output of almost 2.5 V. U4B acts as a noninverting amplifier with a gain of 1.44 in order to scale the 0- to 2.5-V integrator output to a 0-to 3.6-V output range.

R8 and R10 provide output gain and zero-level calibration. This circuit operates over a 100-Hz to 10-kHz frequency range.



NOTES: U1 = TLC3702; $V_{CC\pm}$ = ±5 V.
U2 = SN74HC109.
U3 = TLC4066.
U4 = TL052; $V_{CC\pm}$ = ±5 V.

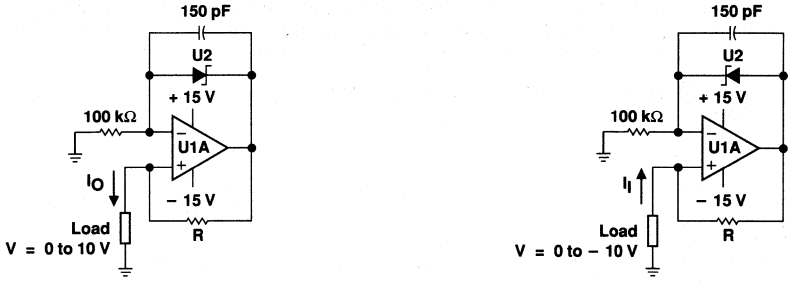
FIGURE 55. PHASE METER

TYPICAL APPLICATION DATA

precision constant-current source over temperature

A precision current source benefits from the high input impedance and stability of Texas Instruments enhanced JFET process. A low-current shunt regulator maintains 2.5 V between the inverting input and the output of the TL052. The negative feedback then forces 2.5 V across the current setting resistor R; therefore, the current to the load is simply 2.5 V divided by R.

Possible choices for the shunt regulator include the LT1004, LT1009, and LM385. Note that if the regulator's cathode connects to the op amp output, this circuit will source load current. Similarly, if the cathode connects to the inverting input, the circuit will sink current from the load. To minimize output current change with temperature, R should be a metal film resistor with a low temperature coefficient. Also, this circuit must be operated with split voltage supplies.



(a) SOURCE CURRENT LOAD

(b) SINK CURRENT LOAD

NOTES: IC1 = LM385, LT1004, or LT1009 voltage reference.
U1A = TL052.
$I = \frac{2.5\ V}{R}$, R = Low temperature coefficient metal film resistor.

FIGURE 56. PRECISION CONSTANT-CURRENT SOURCE

- **Maximum Offset Voltage . . . 1.5 mV (TL054A)**
- **High Slew Rate . . . 15.9 V/μs Typ at 25°C**
- **Low Total Harmonic Distortion . . . 0.003% Typ at R_L = 2 kΩ**
- **Low Noise Voltage . . . 21 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Currents . . . 30 pA Typ**
- **Monolithic Construction**

description

The TL054 and TL054A quad operational amplifiers incorporate well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. These devices offer the significant advantages of Texas Instruments new enhanced JFET process. This process affords not only low initial offset voltage due to the on-chip zener trim capability but also stable offset voltage over time and temperature. In comparison, traditional JFET processes are plagued by significant offset voltage drift.

This new enhanced process still maintains the traditional JFET advantages of fast slew rates and low input bias and offset currents. These advantages coupled with low noise and low harmonic distortion make the TL054 well-suited for new state-of-the-art designs as well as existing design upgrades. The TL054 has been designed to be functionally compatible, as well as pin compatible, with the TL074 and TL084.

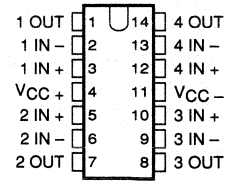
Two offset voltage grades are available: TL054 (4 mV max) and TL054A (1.5 mV max).

AVAILABLE OPTIONS

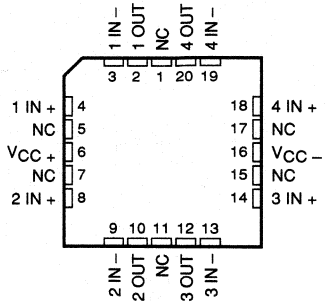
T_A	V_{IO} max AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	1.5 mV	TL054ACD	—	TL054ACJ	TL054ACN
	4 mV	TL054CD	—	TL054CJ	TL054CN
– 40°C to 85°C	1.5 mV	TL054AID	—	TL054AIJ	TL054AIN
	4 mV	TL054ID	—	TL054IJ	TL054IN
– 55°C to 125°C	1.5 mV	TL054AMD	TL054AMFK	TL054AMJ	TL054AMN
	4 mV	TL054MD	TL054MFK	TL054MJ	TL054MN

D packages are available taped-and-reeled. Add "R" suffix to device type (e.g., TL054CDR).

D, J, or N PACKAGE
(TOP VIEW)

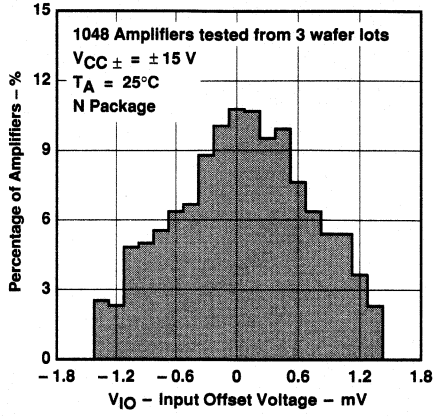


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TL054A
INPUT OFFSET VOLTAGE

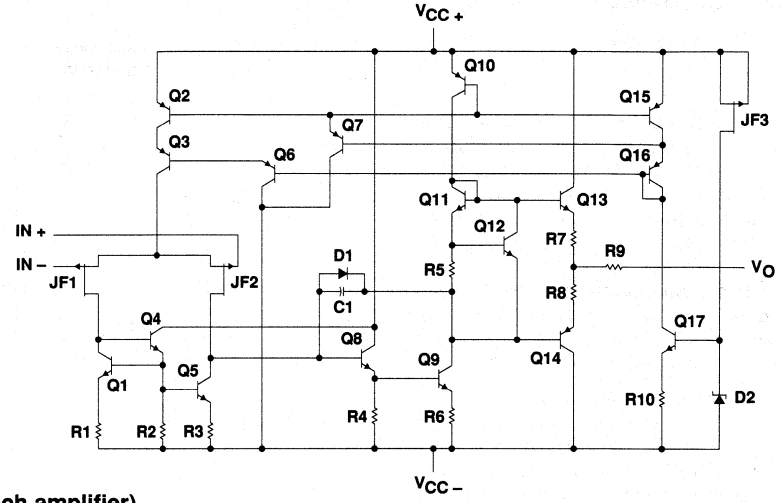


description (continued)

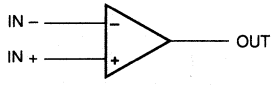
A variety of available packaging options includes small-outline and chip carrier versions for high-density system applications.

The M-suffix devices are characterized for operation over the full military temperature range of – 55°C to 125°C. The I-suffix devices are characterized for operation from – 40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



symbol (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . – 18 V
Differential input voltage (see Note 2) . . . . . ± 30 V
Input voltage range, V_I (any input, see Notes 1 and 3) . . . . . ± 15 V
Input current, I_I (each input) . . . . . ± 1 mA
Output current, I_O (each output) . . . . . ± 80 mA
Total current into V_{CC+} terminal . . . . . 160 mA
Total current out of V_{CC-} terminal . . . . . 160 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . – 55°C to 125°C
I-suffix . . . . . – 40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE TA = 25°C	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	230 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		± 5		± 15	± 5		± 15	± 5		± 15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ± 5 V	– 1		4	– 1		4	– 1		4	V
	$V_{CC\pm}$ = ± 15 V	– 11		11	– 11		11	– 11		11	
Operating free-air temperature, T_A		– 55		125	– 40		85	0		70	°C

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL054M	25°C		0.64	5.5		0.56	4	mV
				Full range			10.5			9	
			TL054AM	25°C		0.57	3.5		0.5	1.5	
				Full range			8.5			6.5	
α_{VIO}	Temperature coefficient of input offset voltage		TL054M	25°C to 125°C		21			20		μV/°C
			TL054AM	25°C to 125°C		21			20		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				125°C		1	20		2	20	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				125°C		10	50		20	50	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	72		50	133		V/mV
				−55°C	30	99		60	209		
				125°C	10	35		15	35		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	84		75	92		dB
				−55°C	65	83		75	92		
				125°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−55°C	75	98		75	98		
				125°C	75	100		75	100		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		8.1	11.2		8.4	11.2	mA
				−55°C		7.8	12.8		8.1	12.8	
				125°C		7.1	11.2		7.5	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −55°C to 125°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				−55°C		16.7			18.3		
				125°C		12.9			16.7		
SR−	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				−55°C		14.7			16.3		
				125°C		12.2			14.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−55°C		51			52		
				125°C		68			68		
t_f	Fall time			25°C		55			57		
				−55°C		51			52		
				125°C		68			69		
	Overshoot factor			25°C		24%			19%		
				−55°C		25%			19%		
				125°C		25%			19%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21		
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				−55°C		3.4			3.4		
				125°C		2.1			2.1		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				−55°C		58°			62°		
				125°C		60°			64°		

† Full range is −55°C to 125°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL054I	25°C		0.64	5.5		0.56	4	mV
				Full range			8.8			7.3	
			TL054AI	25°C		0.57	3.5		0.5	1.5	
				Full range			6.8			4.8	
α_{VIO}	Temperature coefficient of input offset voltage		TL054I	25°C to 85°C		25			24		μV/°C
			TL054AI	25°C to 85°C		25			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				85°C		0.06	10		0.07	10	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				85°C		0.6	20		0.7	20	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	72		50	133		V/mV
				−40°C	30	101		60	212		
				85°C	20	50		30	70		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	84		75	92		dB
				−40°C	65	83		75	92		
				85°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				−40°C	75	98		75	99		
				85°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		8.1	11.2		8.4	11.2	mA
				−40°C		7.9	12.8		8.2	12.8	
				85°C		7.6	11.2		7.9	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is −40°C to 85°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$SR+$	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				−40°C		16.4		8	18		
				85°C		14		8	17.3		
$SR-$	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				−40°C		14.7		8	16.1		
				85°C		13		8	15.3		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				−40°C		52			53		
				85°C		64			65		
t_f	Fall time			25°C		55			57		
				−40°C		51			53		
				85°C		64			65		
	Overshoot factor			25°C		24%			19%		
				−40°C		24%			19%		
				85°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				−40°C		3.3			3.3		
				85°C		2.3			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				−40°C		59°			62°		
				85°C		61°			64°		

† Full range is −40°C to 85°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50 Ω	TL054C	25°C		0.64	5.5		0.56	4	mV
				Full range			7.7			6.2	
			TL054AC	25°C		0.57	3.5		0.5	1.5	
				Full range			5.7			3.7	
α_{VIO}	Temperature coefficient of input offset voltage		TL054C	25°C to 70°C		25			23		μV/°C
			TL054AC	25°C to 70°C		24			23		
	Input offset voltage long-term drift (see Note 5)			25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		4	100		5	100	pA
				70°C		0.02	1		0.025	1	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0, See Figure 5		25°C		20	200		30	200	pA
				70°C		0.15	4		0.2	4	nA
V_{ICR}	Common-mode input voltage range			25°C	−1 to 4	−2.3 to 5.6		−11 to 11	−12.3 to 15.6		V
				Full range	−1 to 4			−11 to 11			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ		25°C	3	4.2		13	13.9		V
				Full range	3			13			
		R_L = 2 kΩ		25°C	2.5	3.8		11.5	12.7		
				Full range	2.5			11.5			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ		25°C	−2.5	−3.5		−12	−13.2		V
				Full range	−2.5			−12			
		R_L = 2 kΩ		25°C	−2.3	−3.2		−11	−12		
				Full range	−2.3			−11			
A_{VD}	Large-signal differential voltage amplification	R_L = 2 kΩ, See Note 6		25°C	25	72		50	133		V/mV
				0°C	30	88		60	173		
				70°C	20	57		30	85		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
C_i	Input capacitance			25°C		10			12		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω		25°C	65	84		75	92		dB
				0°C	65	84		75	92		
				70°C	65	84		75	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5 V to ±15 V, V_O = 0, R_S = 50 Ω		25°C	75	99		75	99		dB
				0°C	75	99		75	99		
				70°C	75	99		75	99		
I_{CC}	Supply current (four amplifiers)	No load, V_O = 0		25°C		8.1	11.2		8.4	11.2	mA
				0°C		8.2	12.8		8.5	12.8	
				70°C		7.9	11.2		8.2	11.2	
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100		25°C		120			120		dB

† Full range is 0°C to 70°C.

NOTES: 5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6. For $V_{CC\pm}$ = ±5 V, V_O = ±2.3 V; at $V_{CC\pm}$ = ±15 V, V_O = ±10 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

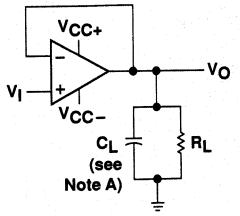
operating characteristics

PARAMETER		TEST CONDITIONS		T_A†	$V_{CC\pm}$ = ±5 V			$V_{CC\pm}$ = ±15 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	R_L = 2 kΩ, C_L = 100 pF, See Figure 1 and Note 7		25°C		15.4		10	17.8		V/μs
				0°C		15.7		8	17.9		
				70°C		14.4		8	17.5		
SR−	Negative slew rate at unity gain			25°C		13.9		10	15.9		
				0°C		14.3		8	16.1		
				70°C		13.3		8	15.5		
t_r	Rise time	V_{IPP} = ±10 mV, R_L = 2 kΩ, C_L = 100 pF, See Figures 1 and 2		25°C		55			56		ns
				0°C		54			55		
				70°C		63			63		
t_f	Fall time			25°C		55			57		
				0°C		54			56		
				70°C		62			64		
	Overshoot factor			25°C		24%			19%		
				0°C		24%			19%		
				70°C		24%			19%		
V_n	Equivalent input noise voltage (see Note 9)	R_S = 100 Ω, See Figure 3	f = 10 Hz	25°C		75			75		nV/√Hz
			f = 1 kHz	25°C		21			21	45	
V_{NPP}	Peak-to-peak equivalent input noise voltage		f = 10 Hz to 10 kHz	25°C		4			4		μV
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	R_S = 1 kΩ, R_L = 2 kΩ, f = 1 kHz, See Note 8		25°C		0.003%			0.003%		
B_1	Unity-gain bandwidth	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		2.7			2.7		MHz
				0°C		3			3		
				70°C		2.4			2.4		
ϕ_m	Phase margin at unity gain	V_i = 10 mV, R_L = 2 kΩ, C_L = 25 pF, See Figure 4		25°C		61°			64°		
				0°C		60°			64°		
				70°C		61°			63°		

† Full range is 0°C to 70°C.

NOTES: 7. For $V_{CC\pm}$ = ±5 V, V_{IPP} = ±1 V; for $V_{CC\pm}$ = ±15 V, V_{IPP} = ±5 V.
8. For $V_{CC\pm}$ = ±5 V, $V_{o(rms)}$ = 1 V; for $V_{CC\pm}$ = ±15 V, $V_{o(rms)}$ = 6 V.
9. This parameter is tested on a sample basis. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

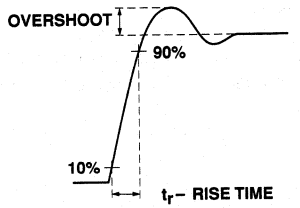


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

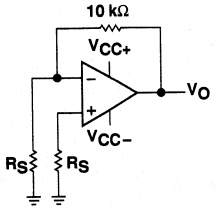
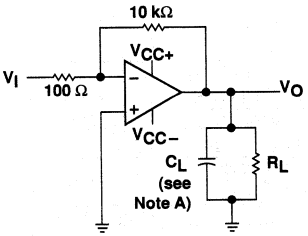


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

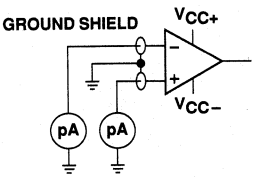


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp-bias-current level typical of the TL054 and TL054A, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Because of the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is sample-tested at f = 1 kHz. Texas Instruments also has additional noise testing capability to meet specific application requirements. Please contact the factory for details.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	6
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Input voltage range	vs V_{CC}	10
		vs Temperature	11
V_O	Output voltage	vs Differential input voltage	12, 13
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	14
		vs Output current	18, 19
		vs Frequency	15, 16, 17
		vs Temperature	20, 21
A_{VD}	Differential voltage amplification	vs R_L	22
		vs Frequency	23
		vs Temperature	24, 25
z_o	Output impedance	vs Frequency	29
CMRR	Common-mode rejection ratio	vs Frequency	26, 27
		vs Temperature	28
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	30
I_{OS}	Short-circuit output current	vs V_{CC}	31
		vs Time	32
		vs Temperature	33
I_{CC}	Supply current	vs V_{CC}	34
		vs Temperature	35
SR	Slew rate	vs R_L	36, 37
		vs Temperature	38, 39
	Overshoot factor	vs C_L	40
V_n	Equivalent input noise voltage	vs Frequency	41
THD	Total harmonic distortion	vs Frequency	42
B_1	Unity-gain bandwidth	vs V_{CC}	43
		vs Temperature	44
ϕ_m	Phase margin	vs V_{CC}	45
		vs C_L	46
		vs Temperature	47
	Phase shift	vs Frequency	23
	Pulse response	Small-signal	48
		Large-signal	49

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE

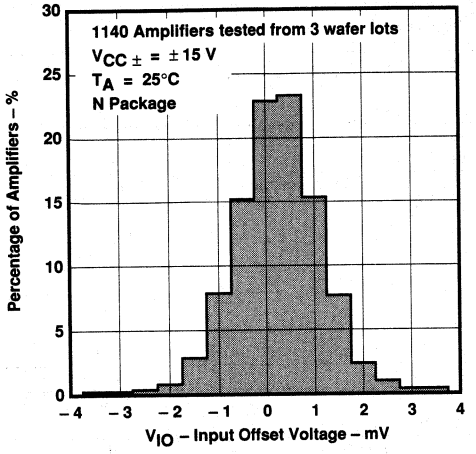


FIGURE 6

DISTRIBUTION OF TL054
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

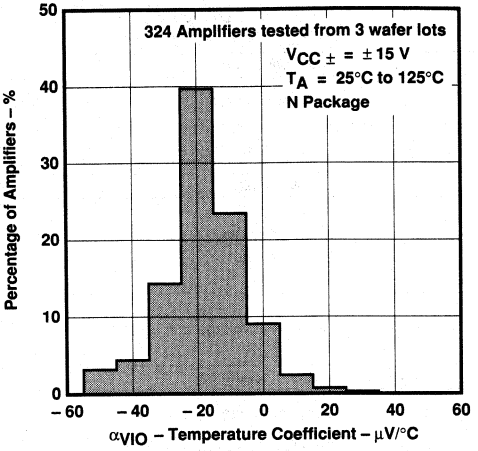


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

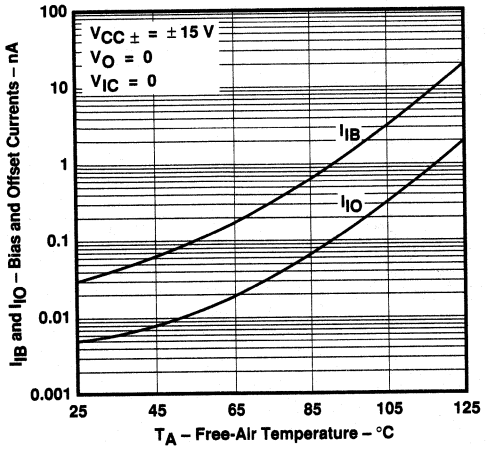


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

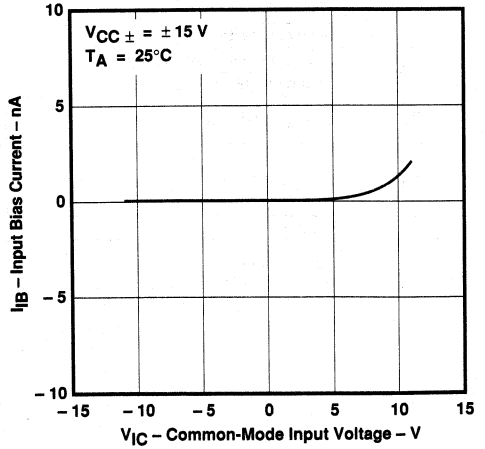


FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

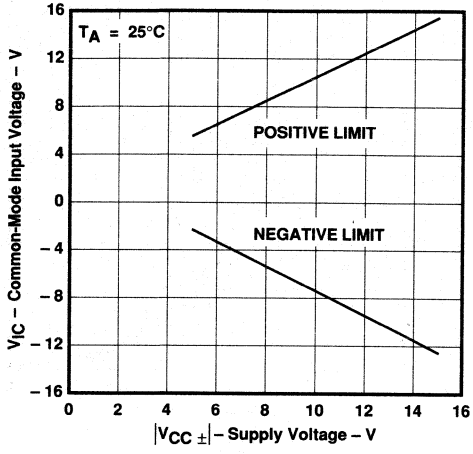


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

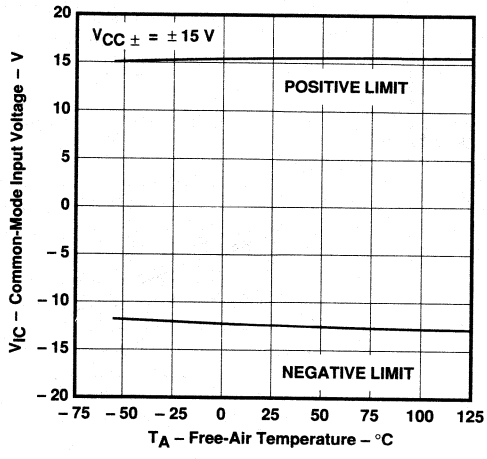


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

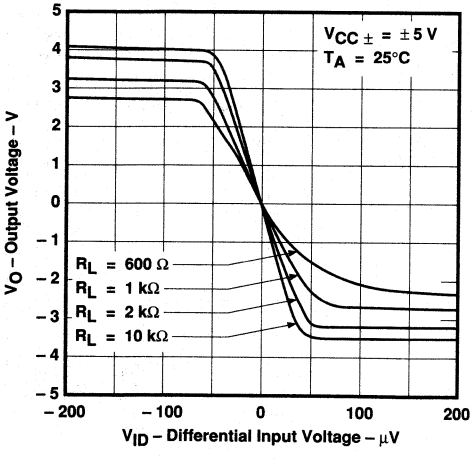


FIGURE 12

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

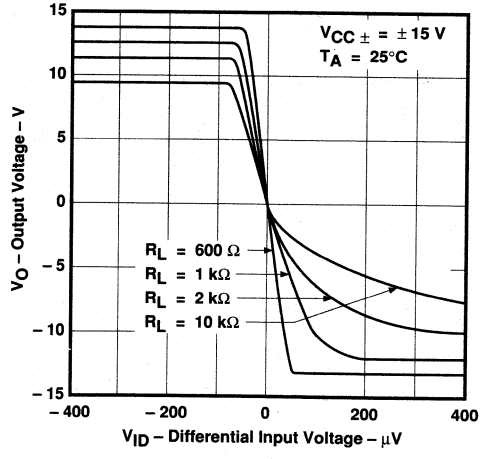


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

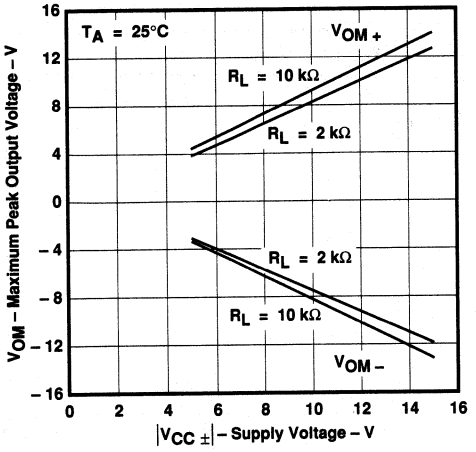


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

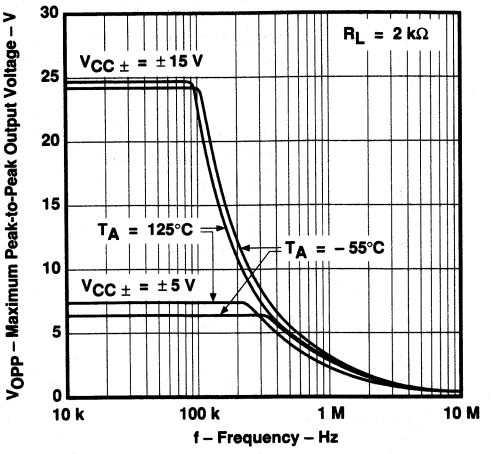


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

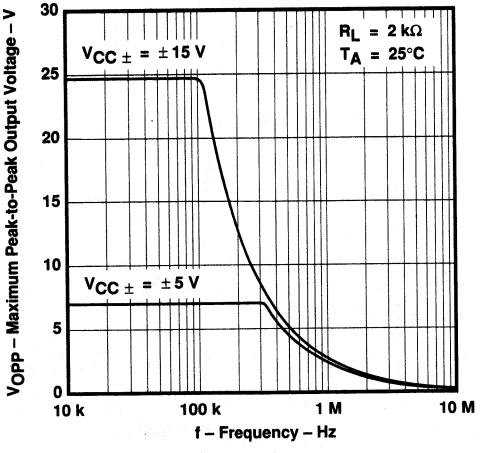


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

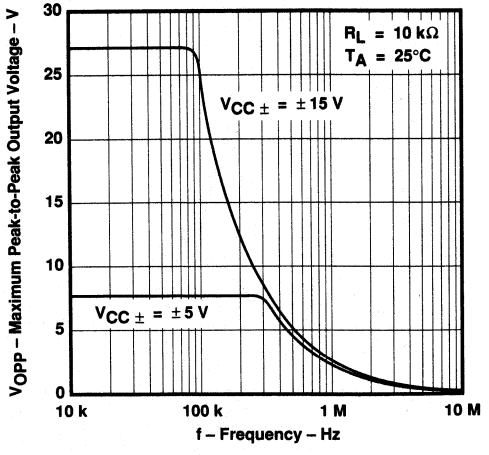


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

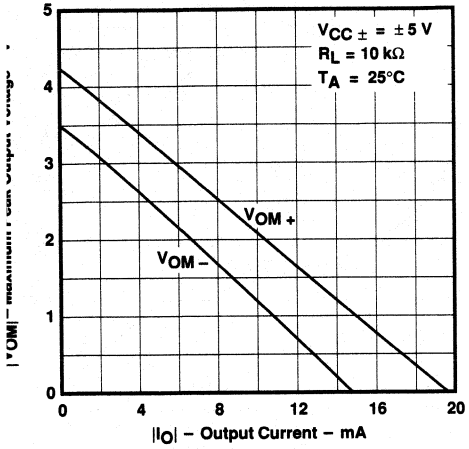


FIGURE 18

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

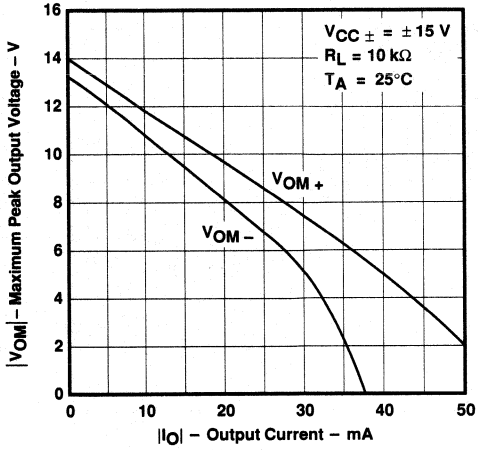


FIGURE 19

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

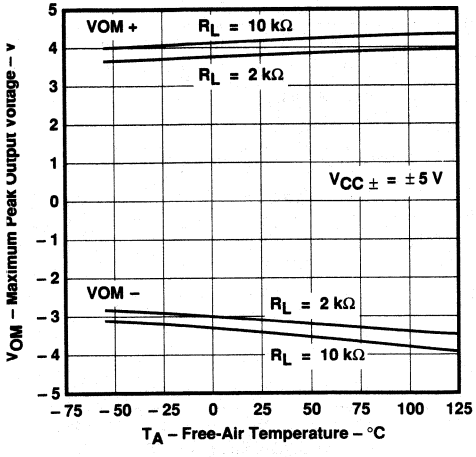


FIGURE 20

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

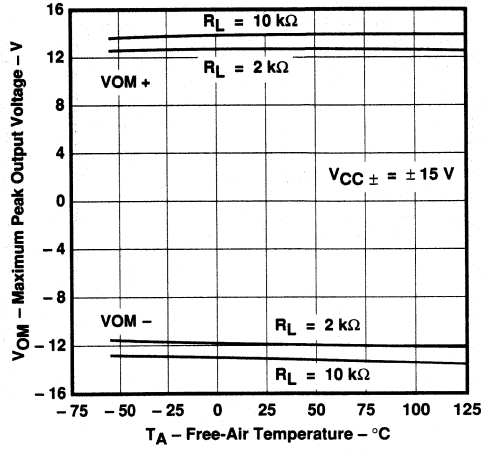


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

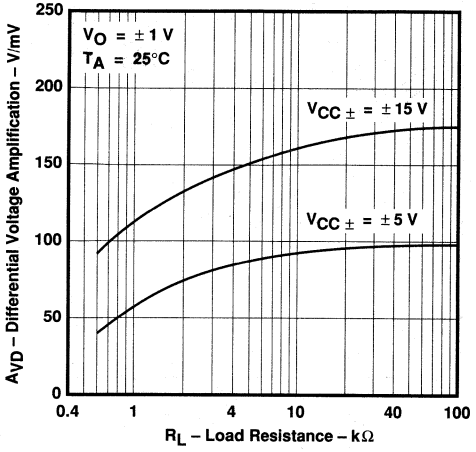


FIGURE 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

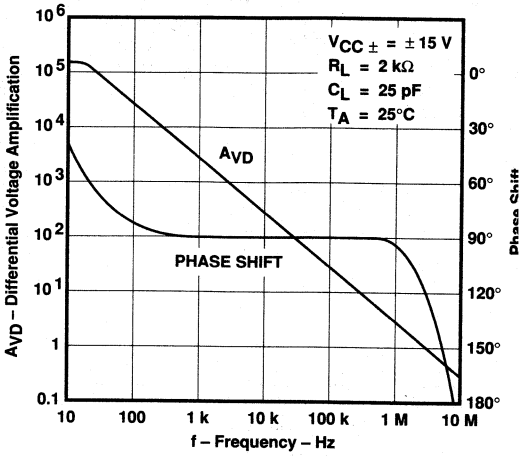


FIGURE 23

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

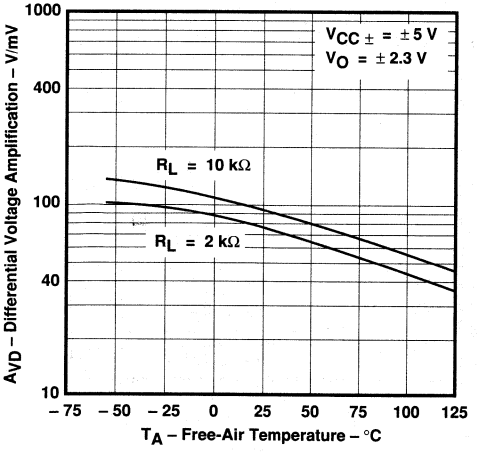


FIGURE 24

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

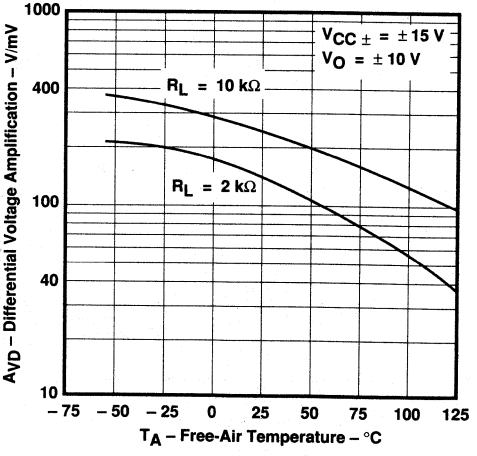


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

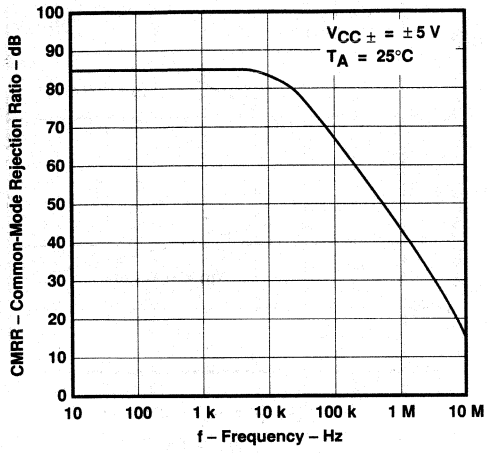


FIGURE 26

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

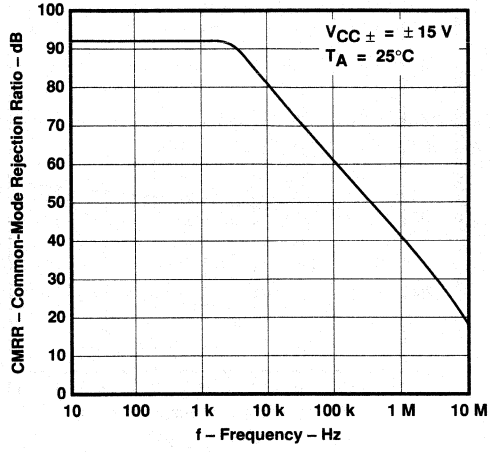


FIGURE 27

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

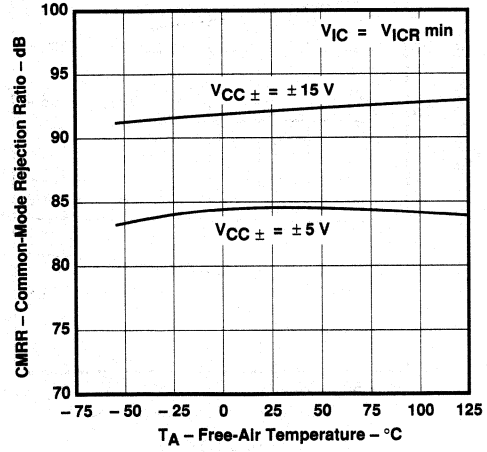


FIGURE 28

OUTPUT IMPEDANCE
vs
FREQUENCY

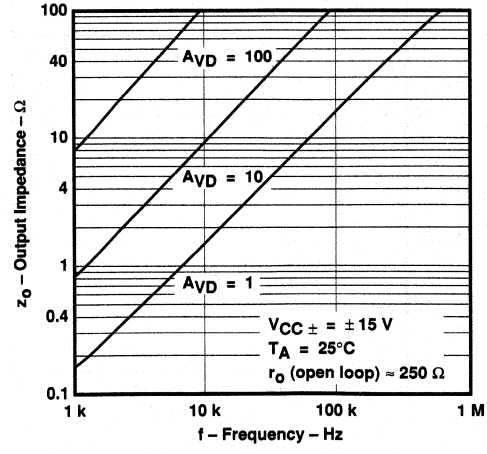


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

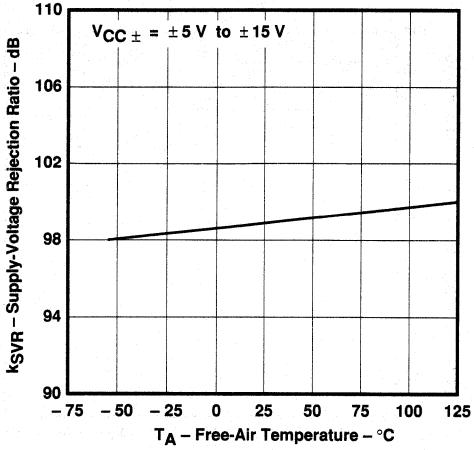


FIGURE 30

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

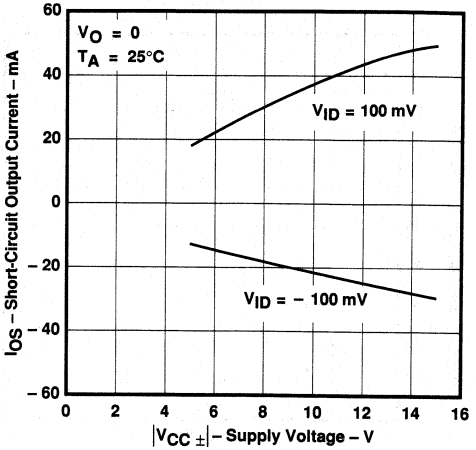


FIGURE 31

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

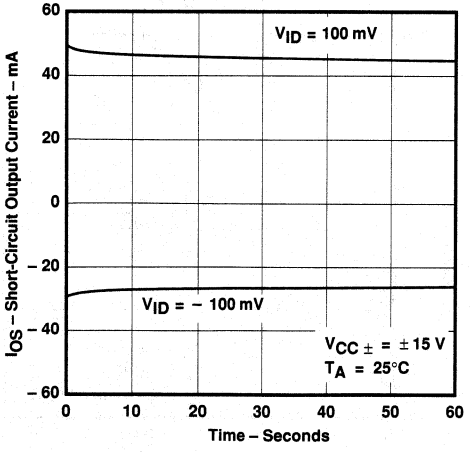


FIGURE 32

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

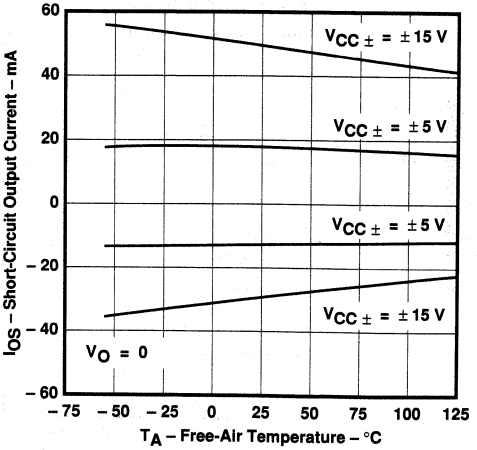


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

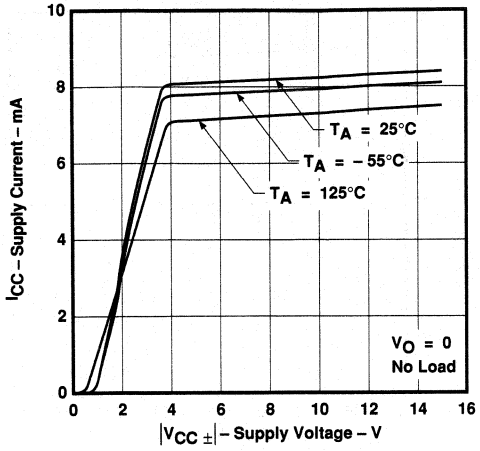


FIGURE 34

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

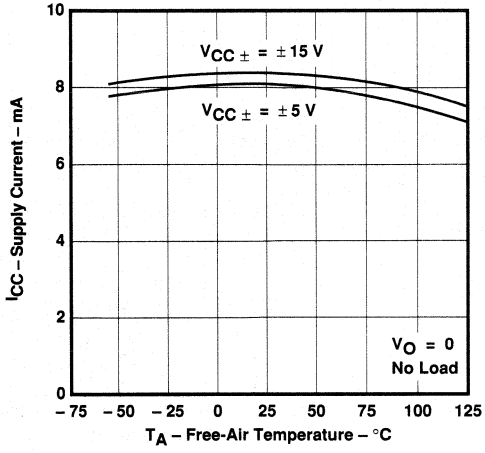


FIGURE 35

SLEW RATE
vs
LOAD RESISTANCE

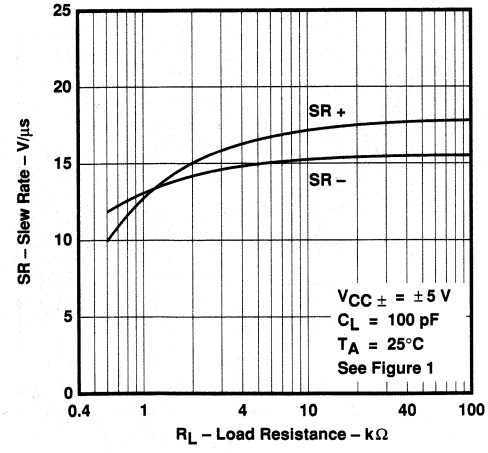


FIGURE 36

SLEW RATE
vs
LOAD RESISTANCE

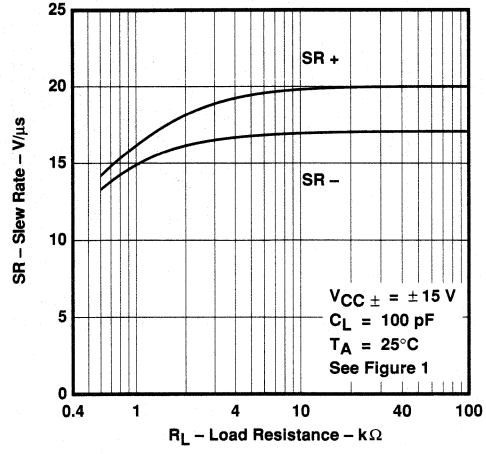


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
FREE-AIR TEMPERATURE

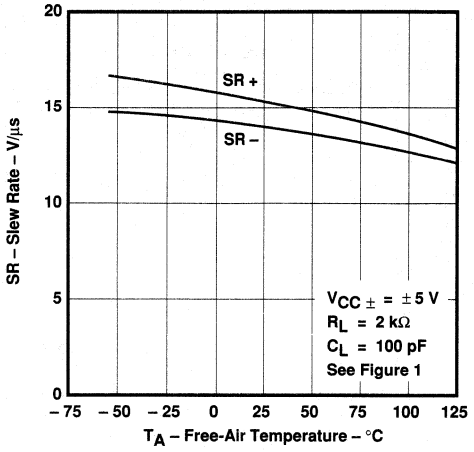


FIGURE 38

SLEW RATE
vs
FREE-AIR TEMPERATURE

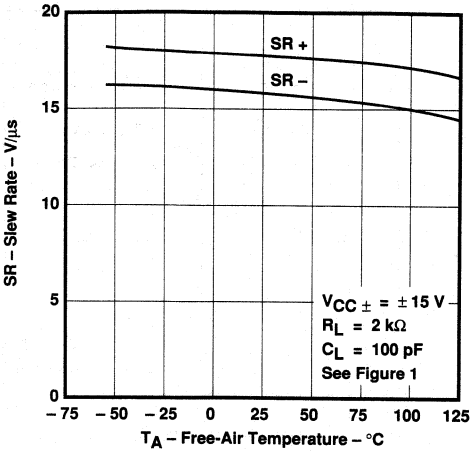


FIGURE 39

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

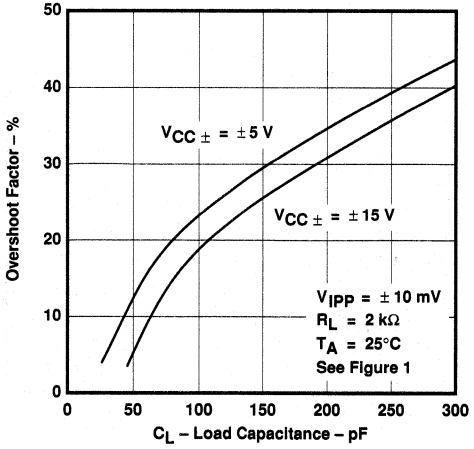


FIGURE 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

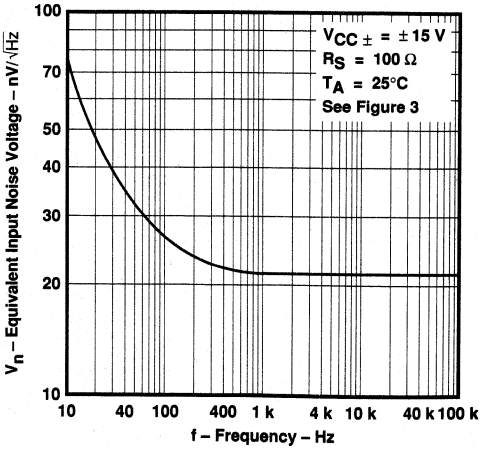


FIGURE 41

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

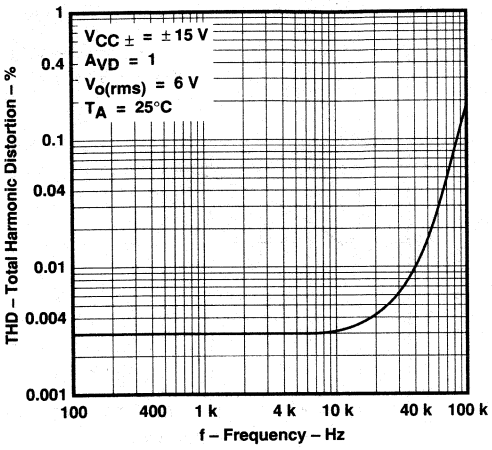


FIGURE 42

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

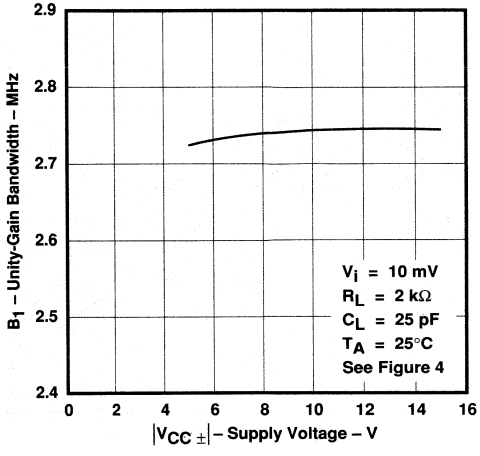


FIGURE 43

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

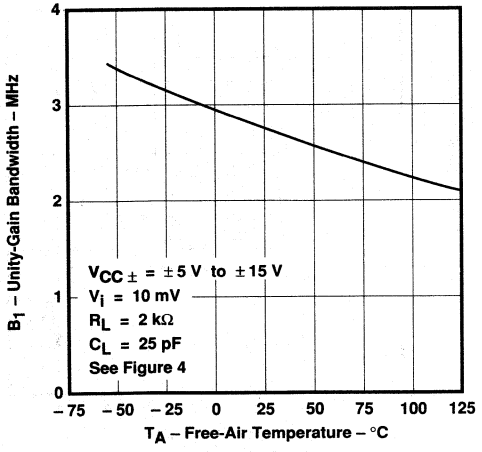


FIGURE 44

PHASE MARGIN
vs
SUPPLY VOLTAGE

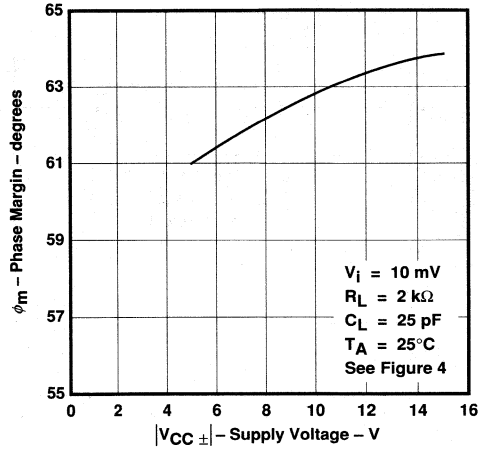


FIGURE 45

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
LOAD CAPACITANCE

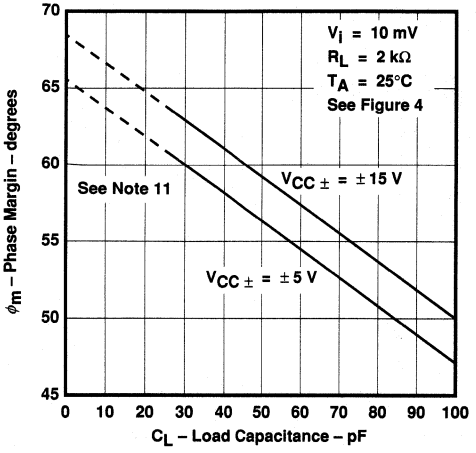


FIGURE 46

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

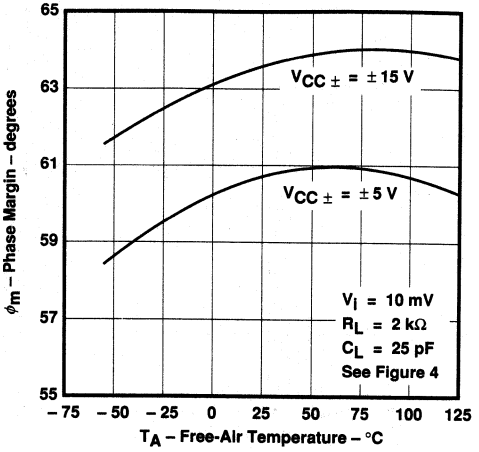


FIGURE 47

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

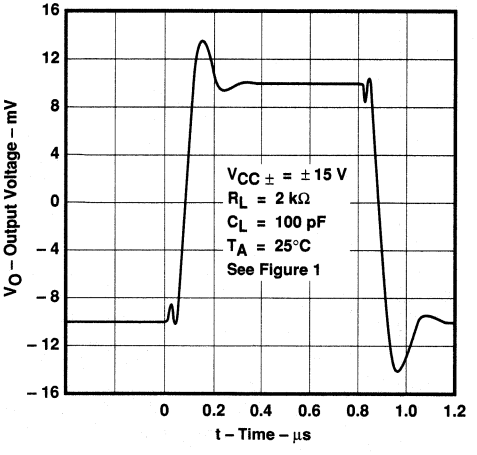


FIGURE 48

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

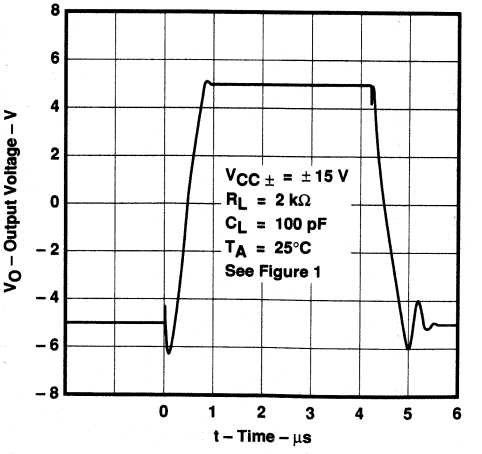


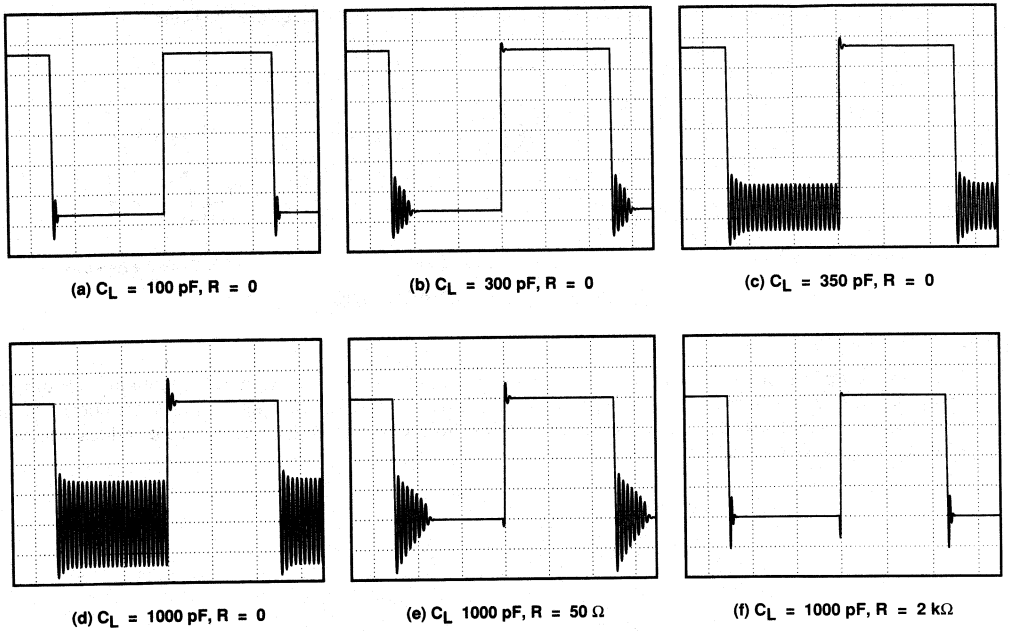
FIGURE 49

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 11: Values of phase margin below a load capacitance of 25 pF were estimated.

TYPICAL APPLICATION DATA

Output characteristics

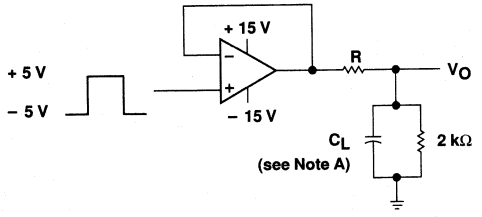
All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL054 and TL054A will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 50).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 50. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 51. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

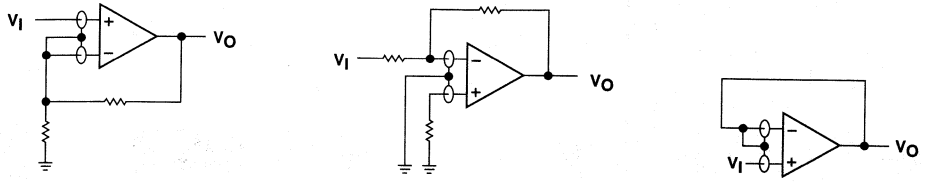
TYPICAL APPLICATION DATA

input characteristics

The TL054 and TL054A are specified with a minimum and a maximum input voltage that, if exceeded at eith input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, the TL054 an TL054A are well suited for low-level signal processing; however, leakage currents on printed circuit boards an sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 52). These guards should be driven from low-impedance source at the same voltage level as the common-mode input.

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 52. USE OF GUARD RINGS

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differentia amplifier. The low input bias current requirements of the TL054 and TL054A result in very low current noise This feature makes the devices especially favorable over bipolar devices when using values of circui impedance greater than 50 kΩ.

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

instrumentation amplifier with adjustable gain/null

The instrumentation amplifier in Figure 53 benefits greatly from the high input impedance and stable input offset voltage of the TL054A. Amplifiers U1A, U1B, and U1C form the actual instrumentation amplifier, while U1D provides offset null. Potentiometer R1 provides gain adjust. With R1 = 2 kΩ, the circuit gain equals 100, while with R1 = 200 kΩ, the circuit gain equals two. The following equation shows the instrumentation amplifier gain as a function of R1:

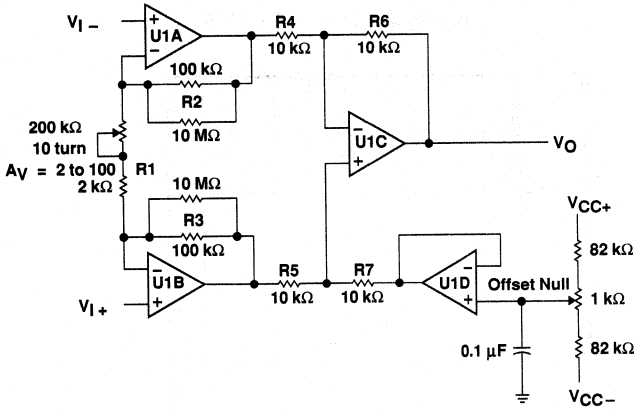
$$A_V = 1 + \left(\frac{R2 + R3}{R1}\right)$$

Readjusting the offset null is necessary whenever the circuit gain is changed. Note that if U1D is needed for another application, R7 can be terminated at ground. The low input offset voltage of the TL054A minimizes the dc error of the circuit. For best matching, all resistors should be one percent tolerance. The matching between R4, R5, R6, and R7 controls the CMRR of this application.

The following equation shows the output voltages when the input voltage equals zero. This dc error can be nulled by adjusting the offset null potentiometer; however, any change in offset voltage over time or temperature also creates an error. To calculate the error from changes in offset, consider the three offset components in the equation as delta offsets rather than initial offsets. The improved stability of Texas Instruments enhanced JFETs minimizes the error resulting from change in input offset voltage with time. Assuming V_{IN} equals zero, V_O can be shown as a function of the offset voltage:

$$V_O = V_{IO2}\left[\left(1 + \frac{R3}{R1}\right)\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R2}{R1}\left(\frac{R6}{R4}\right)\right]$$

$$- V_{IO1}\left[\frac{R3}{R1}\left(\frac{R7}{R5 + R7}\right)\left(1 + \frac{R6}{R4}\right) + \frac{R6}{R4}\left(1 + \frac{R2}{R1}\right)\right] + V_{IO3}\left(1 + \frac{R6}{R4}\right)$$



NOTE A: U1A through U1D = TL054A; $V_{CC\pm}$ = ± 15 V.

FIGURE 53. INSTRUMENTATION AMPLIFIER

TYPICAL APPLICATION DATA

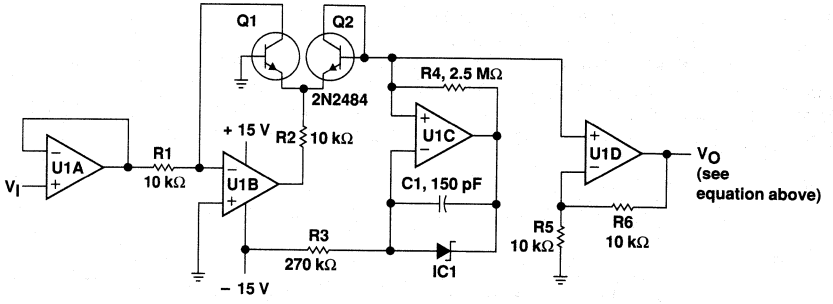
high input impedance log amplifier

The low input offset voltage and high input impedance of the TL054A create a precision log amplifier (see figure 54). IC1 is a 2.5-V, low-current precision, shunt regulator. Transistors Q1 and Q2 must be a closely matched NPN pair. For best performance over temperature, R4 should be a metal film resistor with a low temperature coefficient.

In this circuit, U1A serves as a high-impedance unity-gain buffer. Amplifier U1B converts the input voltage to a current through R1 and Q1. Amplifier U1C, IC1, and R4 form a 1 μA temperature-stable current source that sets the base-emitter voltage of Q2. Amplifier U1D then amplifies the difference between the base-emitter voltage of Q1 and Q2. The output voltage is given by the following equation:

$$V_O = -\left[1 + \frac{R6}{R5}\right]\frac{kT}{q}\left[\ln\frac{V_I}{(R1 \times 1 \times 10^{-6})}\right]$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in kelvins.



NOTES: U1A thru U1D = TL054A.
IC1 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 54. LOG AMPLIFIER

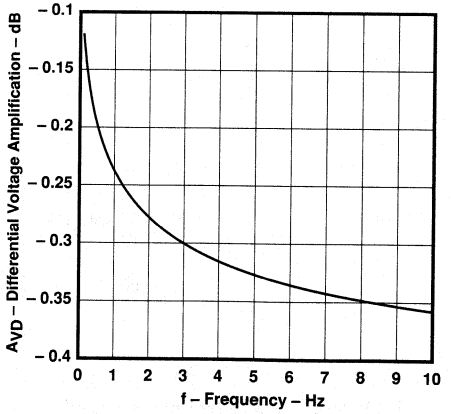


FIGURE 55. OUTPUT VOLTAGE vs INPUT VOLTAGE FOR LOG AMPLIFIER

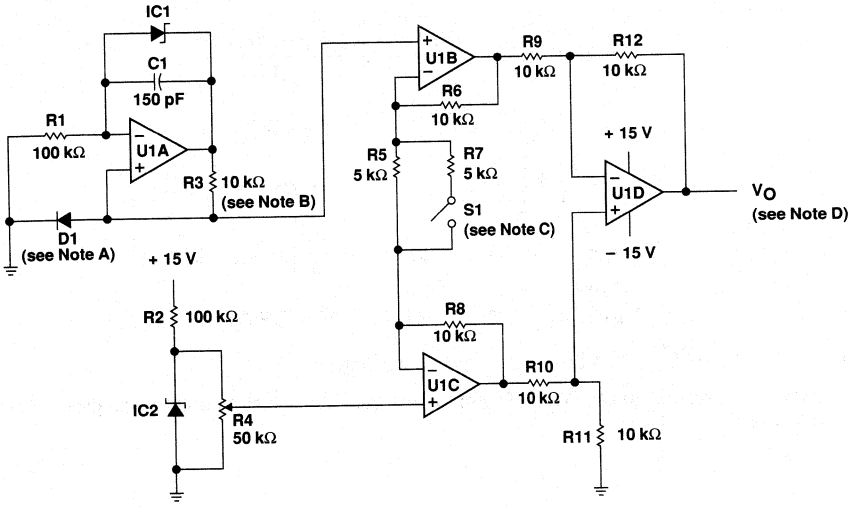
TYPICAL APPLICATION DATA

Analog thermometer

By combining a current source that does not vary over temperature with an instrumentation amplifier, a precise analog thermometer can be built (see Figure 56). Amplifier U1A and IC1 establish a constant current through the temperature sensing diode D1. For this section of the circuit to operate correctly, the TL054 must use split supplies and R3 must be a metal film resistor with a low temperature coefficient.

The temperature-sensitive voltage from the diode is compared to a temperature-stable voltage reference set by IC2. R4 should be adjusted to provide the correct output voltage when the diode is at a known temperature. Although this potentiometer resistance varies with temperature, the divider ratio of the potentiometer remains constant.

Amplifiers U1B, U1C, and U1D form the instrumentation amplifier that converts the difference between the diode and reference voltage to a voltage proportional to the temperature. With switch S1 closed, the amplifier gain equals 5, and the output voltage is proportional to temperature in degrees Celsius. With S1 open, the amplifier gain is 9, and the output is proportional to temperature in degrees Fahrenheit. Every time that S1 is changed, R4 must be recalibrated. By setting S1 correctly, the output voltage equals 10 mV per degree (C or F).



NOTES: A. Temperature sensing diode ≈ (− 2 mV/°C).
B. Metal film (low temperature coefficient).
C. Switch open for °F and closed for °C.
D. $V_O \propto$ Temperature; 10 mV/°C or 10 mV/°F.
E. U1A thru U1D = TL054. IC1, IC2 = LM385, LT1004, or LT1009 voltage reference.

FIGURE 56. ANALOG THERMOMETER

TYPICAL APPLICATION DATA

voltage-ratio-to-dB converter

The application in Figure 57 measures the amplitude ratio of two signals and then converts the ratio t decibels. The output voltage provides a resolution of 100 mV/dB. The two inputs can be either dc or sinusoida ac signals. When using ac signals, both signals should be the same frequency or output glitches will occur For measuring two input signals of different frequencies, extra filtering should be added after the rectifiers.

The circuit contains three low-offset TL054A devices. Two of these devices provide the rectification anc logarithmic conversion of the inputs. The third TL054A forms an instrumentation amplifier. The stage performing the logarithmic conversion also requires two well-matched NPN transistors.

The input signal first passes through a high impedance unity-gain buffer U1A (U2A). Then U1B (U2B) rectifies the input signal at a gain of 0.5, and U1C (U2C) provides a noninverting gain of 2 so that the system gain is still one. U1D (U2D), R6 (R13), and Q1 (Q2) perform the logarithmic conversion of the rectified input signal. The instrumentation amplifier formed by U3A, U3B, U3D scales the difference of the two logarithmic voltages by a gain of 33.6. As a result, the output voltage equals 100 mV/dB. The 1-kΩ potentiometer on the input of U3C calibrates the zero dB reference level. The following equations are used to derive the relationship between the input voltage ratio expressed in decibels and the output voltage.

$$X\,dB = 20\log\left[\frac{V_A}{V_B}\right] = 20\left[\frac{\ln(V_A) - \ln(V_B)}{\ln(10)}\right]$$

$$X\,dB = 8.686\left[\ln(V_A) - \ln(V_B)\right]$$

$$V_{BE(Q1)} = \frac{kT}{q}\ln\left[\frac{V_A}{R \times I_S}\right] \qquad V_{BE(Q2)} = \frac{kT}{q}\ln\left[\frac{V_B}{R \times I_S}\right]$$

$$\Delta V_{BE} = V_{BE(Q1)} - V_{BE(Q2)} = \frac{kT}{q}\left[\ln(V_A) - \ln(V_B)\right]$$

$$X\,dB = \frac{8.686}{kT/q}\left[V_{BE(Q1)} - V_{BE(Q2)}\right] = 336\left[V_{BE(Q1)} - V_{BE(Q2)}\right] \text{ at } 25°C.$$

where $k = 1.38 \times 10^{-23}$, $q = 1.602 \times 10^{-19}$, and T is in kelvins.

This would give a resolution of 1 V/dB. Therefore, the gain of the instrumentation amplifier is set at 33.6 to obtain 100 mV/dB.

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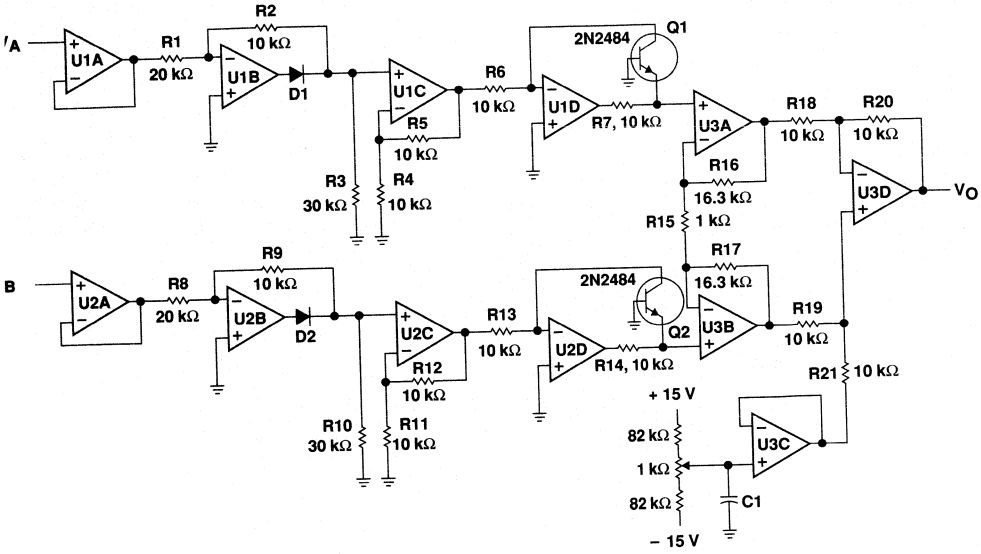
TYPICAL APPLICATION DATA



NOTES: U1A through U3D = TL054A, $V_{CC\pm}$ = ± 15 V.
D1 and D2 = 1N914.

FIGURE 57. VOLTAGE-RATIO-TO-dB CONVERTER

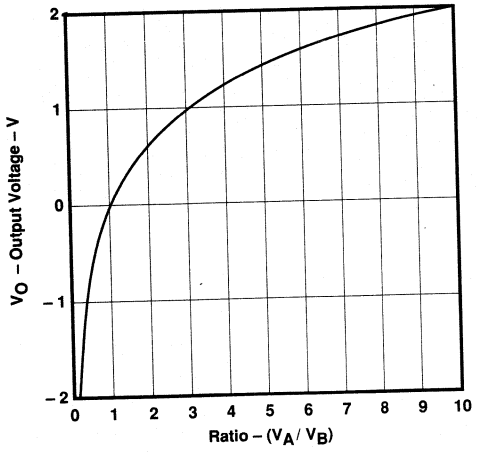


FIGURE 58. OUTPUT VOLTAGE vs THE RATIO OF THE INPUT VOLTAGES FOR VOLTAGE-TO-dB CONVERTER

20 DEVICES COVER MILITARY, INDUSTRIAL, AND COMMERCIAL TEMPERATURE RANGES

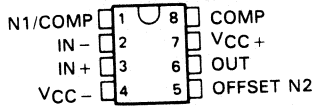
- Very Low Power Consumption
- Typical Supply Current . . . 200 μA (per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes V_{CC+}
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL060)
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/μs Typ

description

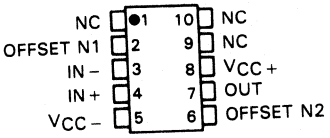
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

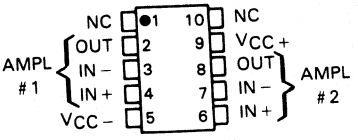
TL060, TL060A, TL060B
D, JG, OR P PACKAGE
(TOP VIEW)



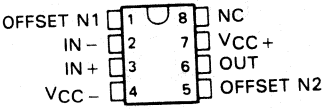
TL061 . . . U PACKAGE
(TOP VIEW)



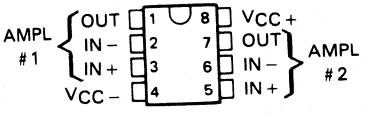
TL062 . . . U PACKAGE
(TOP VIEW)



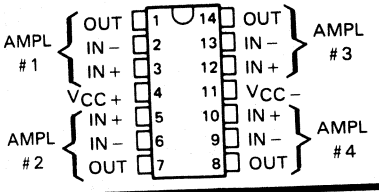
TL061, TL061A, TI061B
D, JG, OR P PACKAGE
(TOP VIEW)



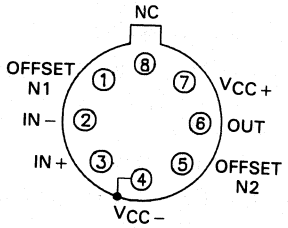
TL062, TL062A, TL062B
D, JG, OR P PACKAGE
(TOP VIEW)



TL064 . . . D, J, N, OR W PACKAGE
TL064A, TL064B . . . D, J, OR N PACKAGE
(TOP VIEW)

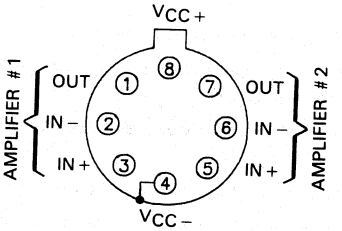


TL061 . . . L PACKAGE
(TOP VIEW)



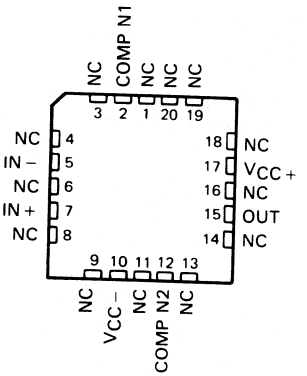
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL062 . . . L PACKAGE
(TOP VIEW)

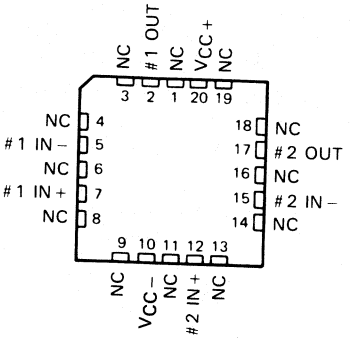


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

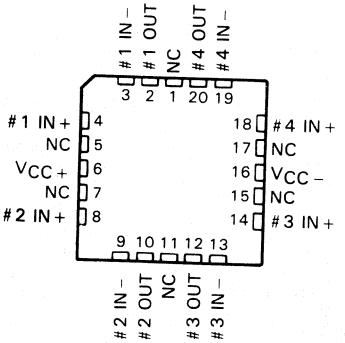
TL061 . . . FK PACKAGE
(TOP VIEW)



TL062 . . . FK PACKAGE
(TOP VIEW)



TL064 . . . FK PACKAGE
(TOP VIEW)



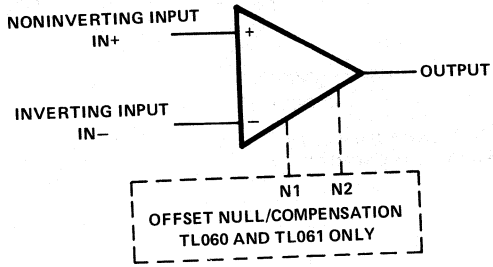
NC—No internal connection

AVAILABLE OPTIONS

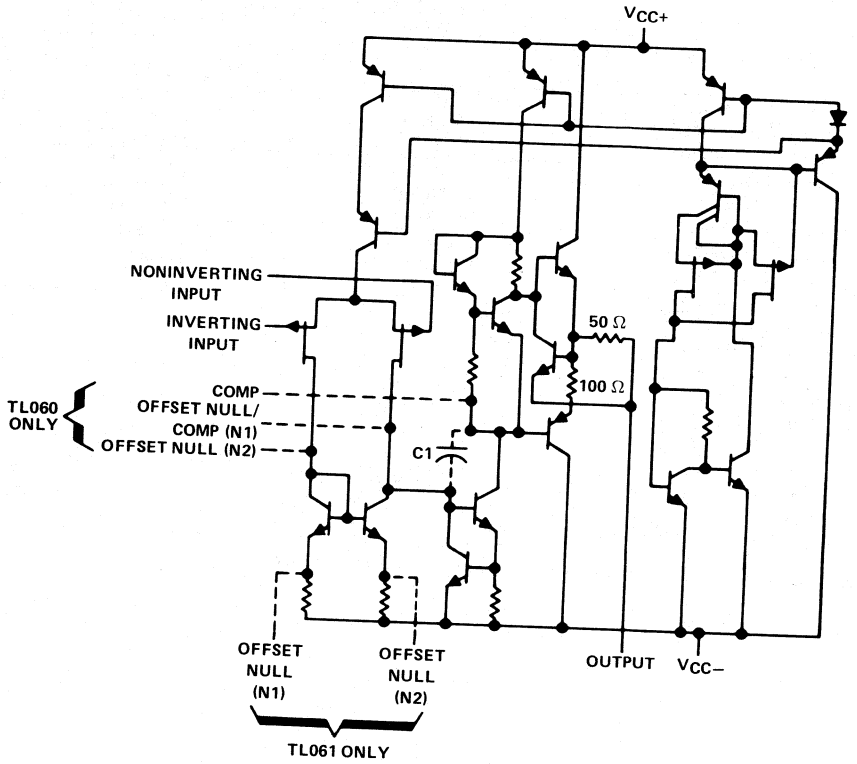
T_A	V_{IO} MAX at 25°C	PACKAGE								
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLUG-IN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	15 mV	TL060CD			TL060CJG			TL060CP		
	6 mV	TL060ACD			TL060ACJG			TL060ACP		
	3 mV	TL060BCD			TL060BCJG			TL060BCP		
	15 mV	TL061CD			TL061CJG			TL061CP		
	6 mV	TL061ACD			TL061ACJG			TL061ACP		
	3 mV	TL061BCD			TL061BCJG			TL061BCP		
	15 mV	TL062CD			TL062CJG			TL062CP		
	6 mV	TL062ACD			TL062ACJG			TL062ACP		
	3 mV	TL062BCD			TL062BCJG			TL062BCP		
	15 mV	TL064CD		TL064CJ			TL064CN			
	6 mV	TL064ACD		TL064ACJ			TL064ACN			
	3 mV	TL064BCD		TL064BCJ			TL064BCN			
−40°C to 85°C	6 mV	TL060ID			TL060IJG			TL060IP		
	6 mV	TL061ID			TL061IJG			TL061IP		
	6 mV	TL062ID			TL062IJG			TL062IP		
	6 mV	TL064ID		TL064IJ			TL064IN			
−55°C to 125°C	6 mV		TL061MFK		TL061MJG	TL061ML			TL061MU	
	6 mV		TL062MFK		TL062MJG	TL062ML			TL062MU	
	9 mV		TL064MFK	TL064MJ						TL064MW

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL061CDR).

symbol (each amplifier)



schematic (each amplifier)



C1 = 10 pF ON TL061, TL062, AND TL064 ONLY
COMPONENT VALUES SHOWN ARE NOMINAL

ɔsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL06_M	TL06_I	TL06_C, TL06_AC, TL06_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N or P package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300			°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL06_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL06_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
L	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	25°C	432 mW	351 mW	135 mW
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

electrical characteristics, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL061M TL062M			TL064M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω,	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		30	200		30	200	pA
			T_A = −55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = −55°C to 125°C	±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L ≥ 10 kΩ	T_A = 25°C	4	6		4	6		V/mV
			T_A = −55°C to 125°C	4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C								MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, V_O = 0, T_A = 25°C			6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			200	250		200	250	μA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ± 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL060I TL061I TL062I TL064I			TL060C TL061C TL062C TL064C			TL060AC TL061AC TL062AC TL064AC			TL060BC TL061BC TL062BC TL064BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range			10			10			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			5			3			3	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	200		30	400		30	200		30	200	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to +15		±11	−12 to +15		±11.5	−12 to +15		±11.5	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ,	T_A = 25°C	±10	±13.5		±10	±13.5		±10	±13.5		±10	±13.5		V
		R_L ≥ 10 kΩ,	T_A = full range	±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ± 10 V, R_L ≥ 10 kΩ	T_A = 25°C	4	6		3	6		4	6		4	6		V/mV
			T_A = full range	4			3			4			4			
B_1	Unity-gain bandwidth	R_L = 10 kΩ, T_A = 25°C			1			1			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	95		70	95		80	95		80	95		dB
P_D	Total power dissipation (each amplifier)	No load, T_A = 25°C	V_O = 0,		6	7.5		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current (each amplifier)	No load, T_A = 25°C	V_O = 0,		200	250		200	250		200	250		200	250	μA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL06_I and 0°C to 70°C for TL06_C, TL06_AC, and TL06_BC.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 17. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.2		μs
	Overshoot factor				10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		42		nV/√Hz

2 Operational Amplifiers

PARAMETER MEASUREMENT INFORMATION

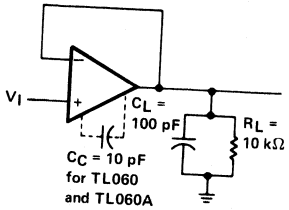


FIGURE 1. UNITY-GAIN AMPLIFIER

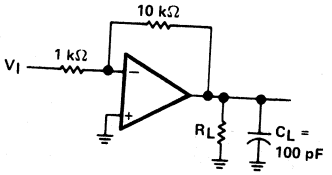


FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

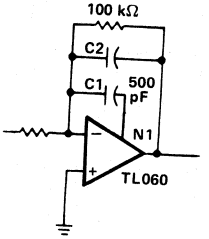
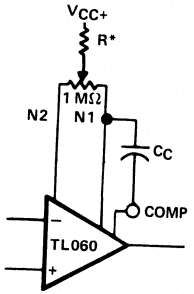


FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS



*For best results use R = 20 MΩ for $V_{CC\pm}$ = ±15 V to R = 5 MΩ for $V_{CC\pm}$ = ±3 V.

FIGURE 4

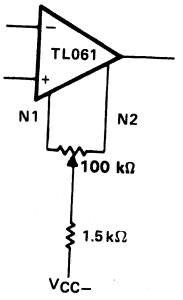


FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

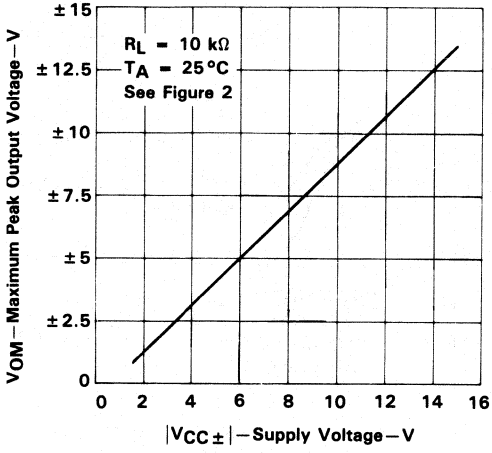


FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

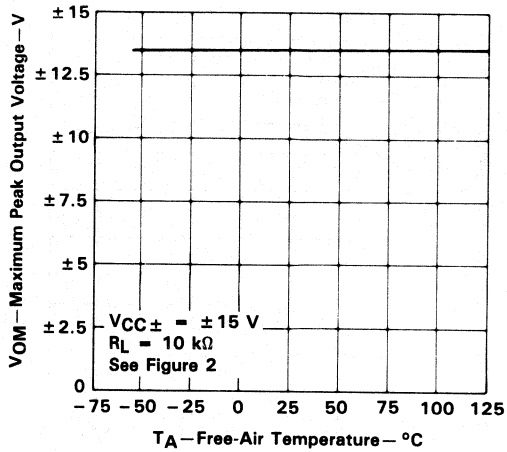


FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

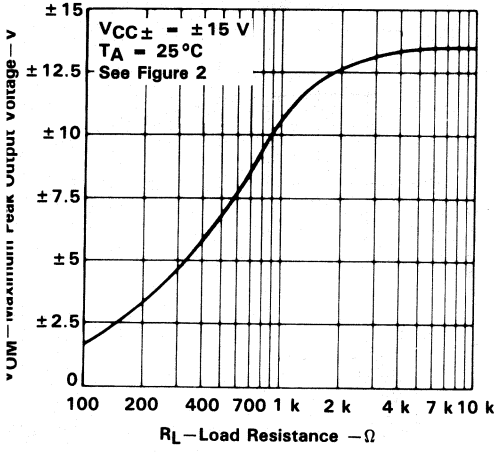


FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

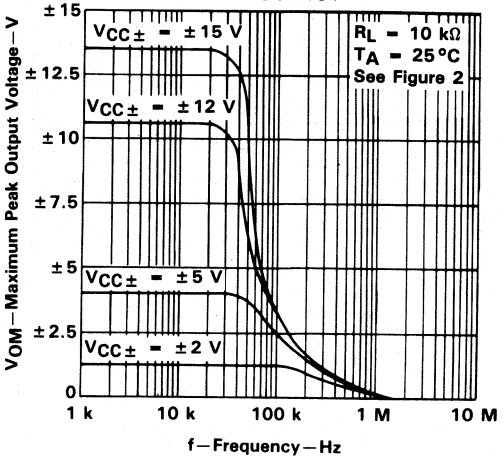


FIGURE 9

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

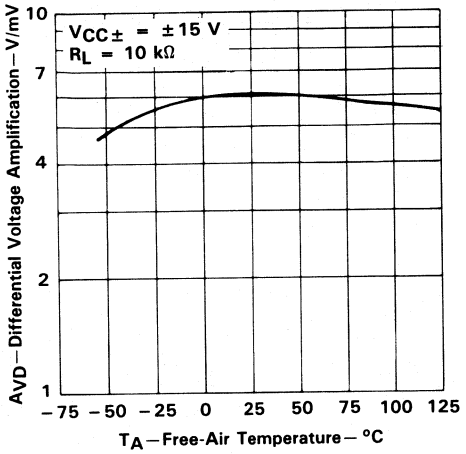


FIGURE 10

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

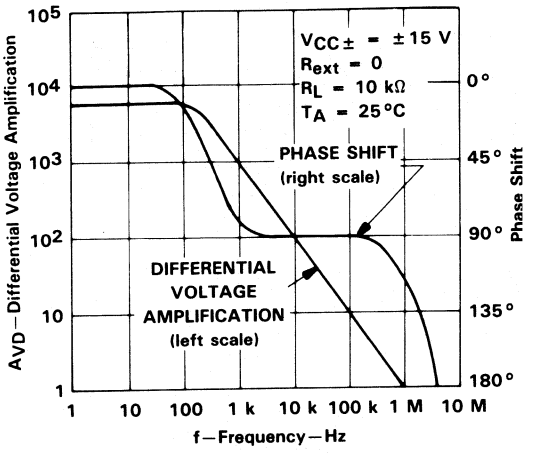


FIGURE 11

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

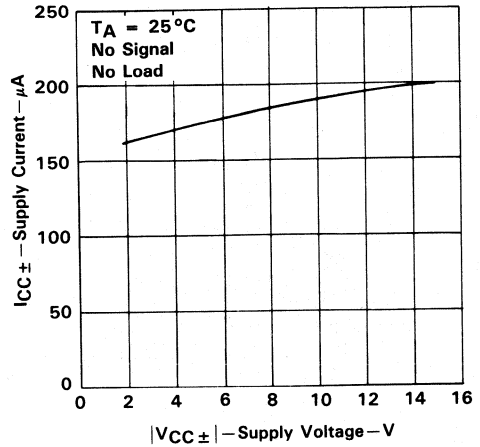


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

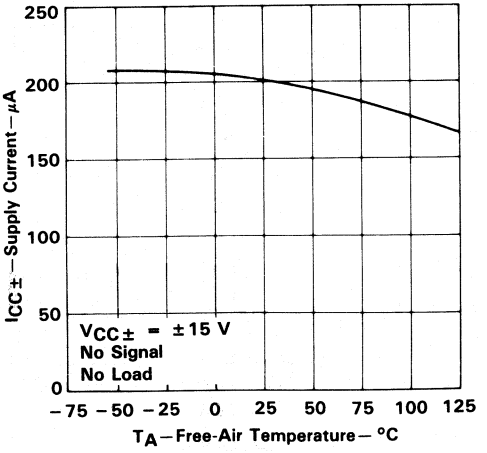


FIGURE 13

†A 10-pF compensation capacitor is used with TL060 and TL060A.

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TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

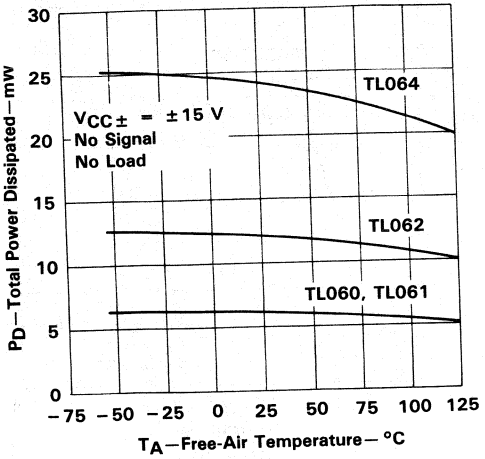

FIGURE 14

ALL EXCEPT TL06_C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

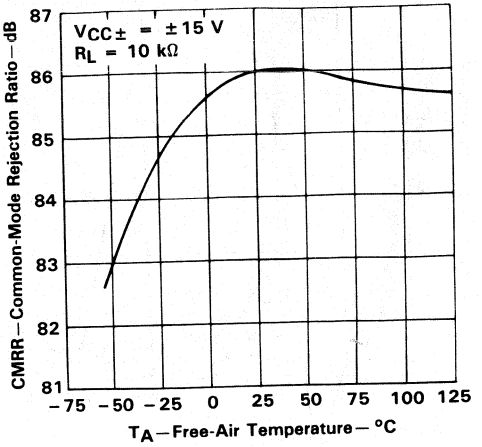

FIGURE 15

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

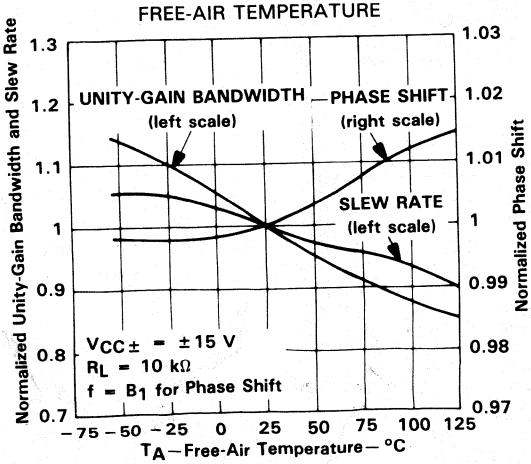

FIGURE 16

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

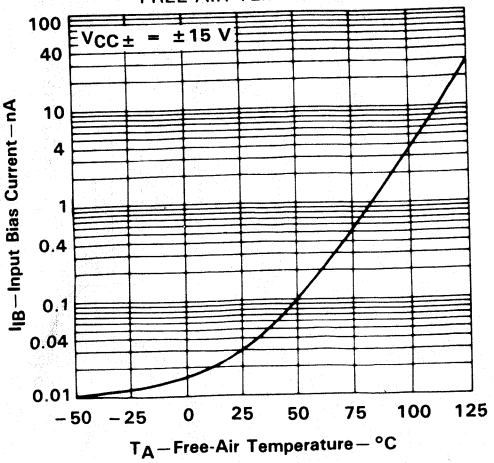

FIGURE 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

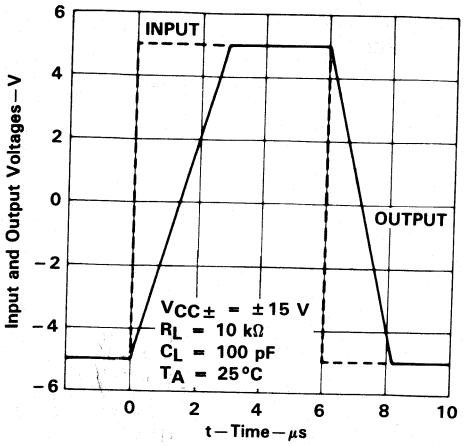

FIGURE 18

OUTPUT VOLTAGE
vs
ELAPSED TIME

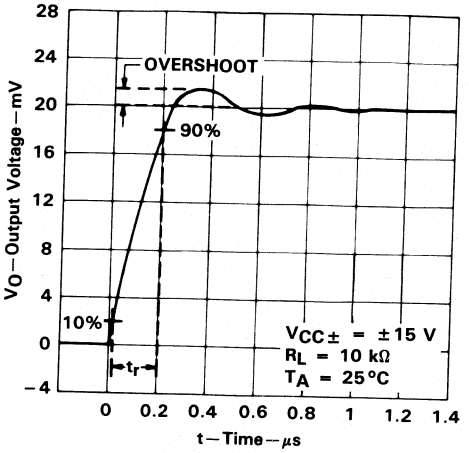

FIGURE 19

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

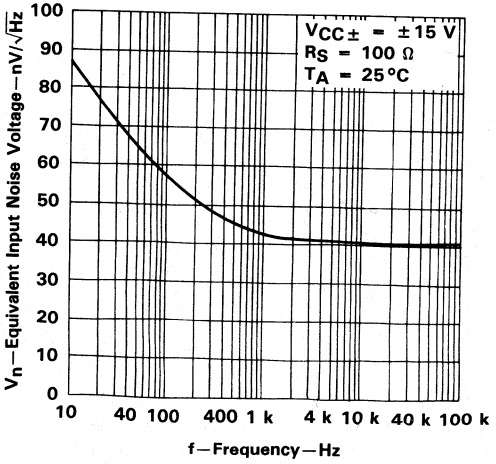

FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 10-pF compensation capacitor is used with TL060 and TL060A.

TYPICAL APPLICATION DATA

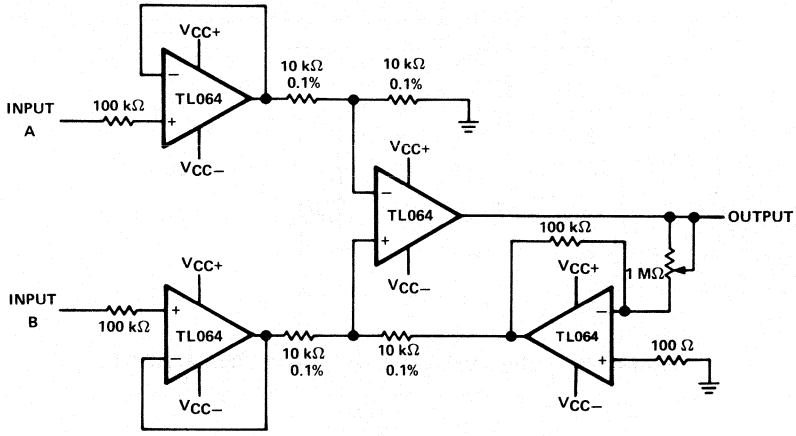

FIGURE 21. INSTRUMENTATION AMPLIFIER

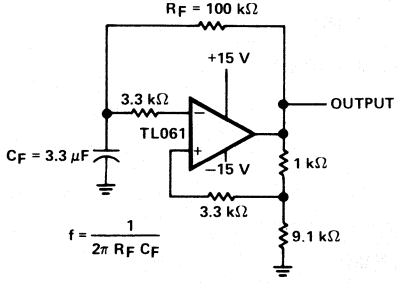

FIGURE 22. 0.5-Hz SQUARE-WAVE OSCILLATOR

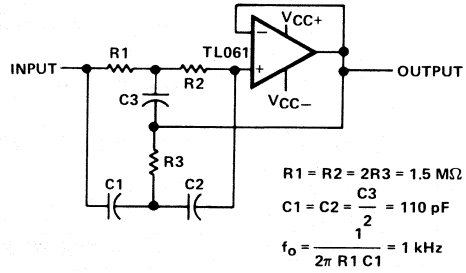

FIGURE 23. HIGH-Q NOTCH FILTER

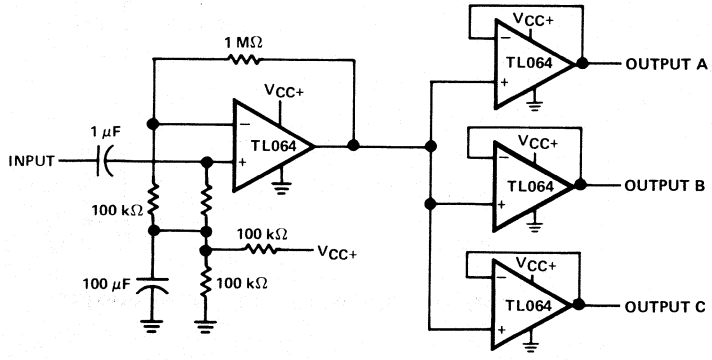

FIGURE 24. AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA

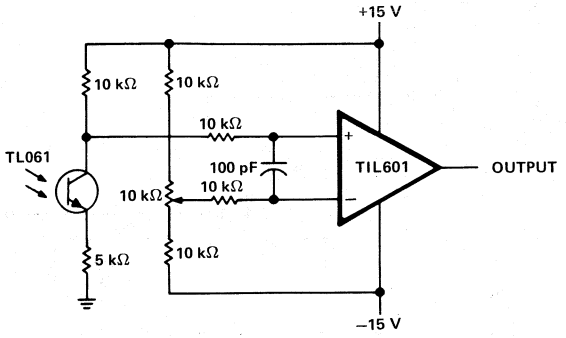

FIGURE 25. LOW-LEVEL LIGHT DETECTOR PREAMPLIFIER

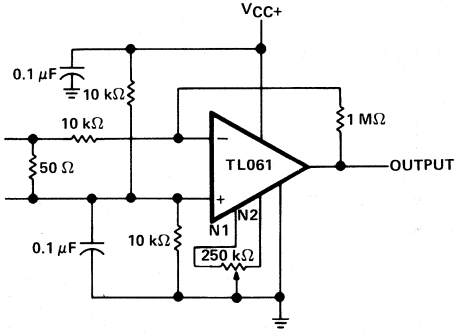

FIGURE 26. AC AMPLIFIER

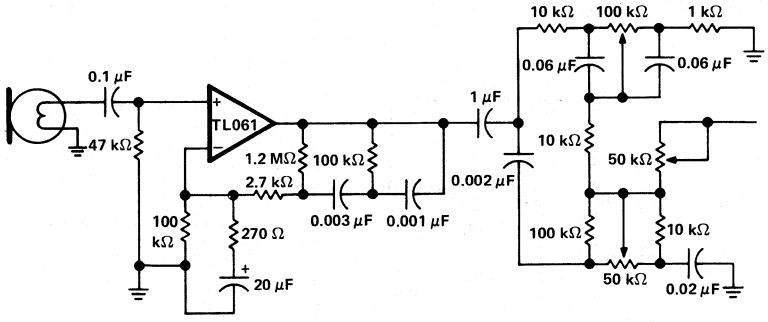

FIGURE 27. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

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TYPICAL APPLICATION DATA

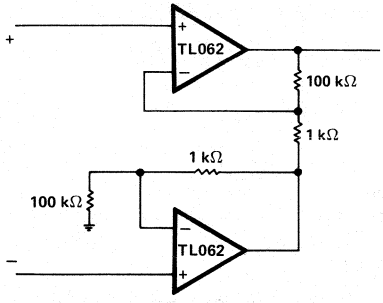


FIGURE 28. INSTRUMENTATION AMPLIFIER

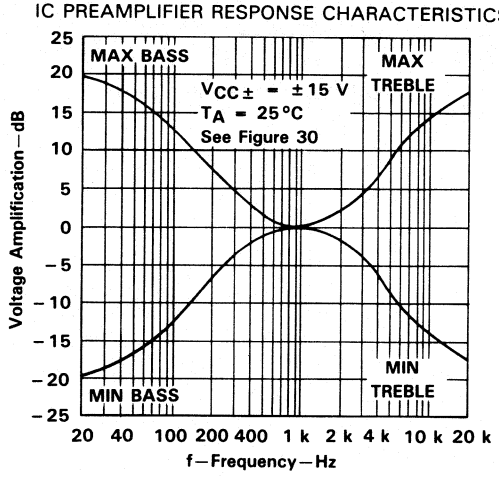


FIGURE 29

TYPICAL APPLICATION DATA

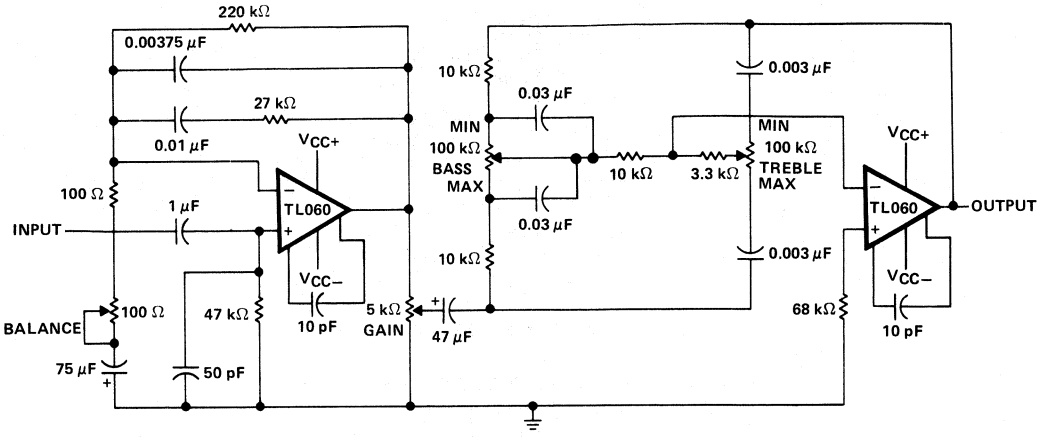


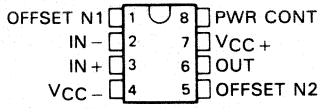
FIGURE 30. IC PREAMPLIFIER

D2494, FEBRUARY 1979—REVISED NOVEMBER 1988

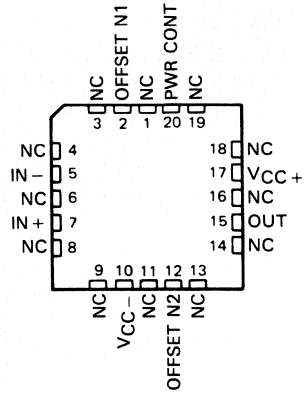
5 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- **Very Low, Adjustable ("Programmable") Power Consumption**
- **Adjustable Supply Current . . . 5 μA to 200 μA**
- **Very Low Input Bias and Offset Currents**
- **Wide Supply Range . . . ±1.2 V to ±18 V**
- **Wide Common-Mode and Differential Voltage Range**
- **Output Short-Circuit Protection**
- **High Input Impedance . . . JFET-Input Stage**
- **Unity-Gain Bandwidth . . . 1 MHz Typ (100 kHz at 25 μW)**
- **High Slew Rate . . . 3.5 V/μs Typ**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

TL066M . . . JG PACKAGE
TL066I, TL066C, TL066AC, TL066BC . . . D, JG, OR P PACKAGE
(TOP VIEW)



TL066M . . . FK PACKAGE
(TOP VIEW)



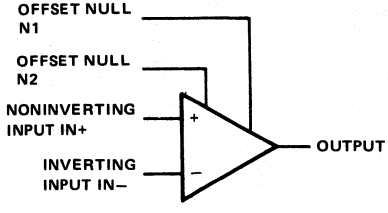
NC—No internal connection

TL066M IS NOT RECOMMENDED FOR NEW DESIGNS

description

The TL066, TL066A, and TL066B are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 μW of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable." The JFET-input stage combined with the adjustable-low-power feature results in superior bandwidth and slew-rate performance compared to low-power bipolar-input devices.

symbol



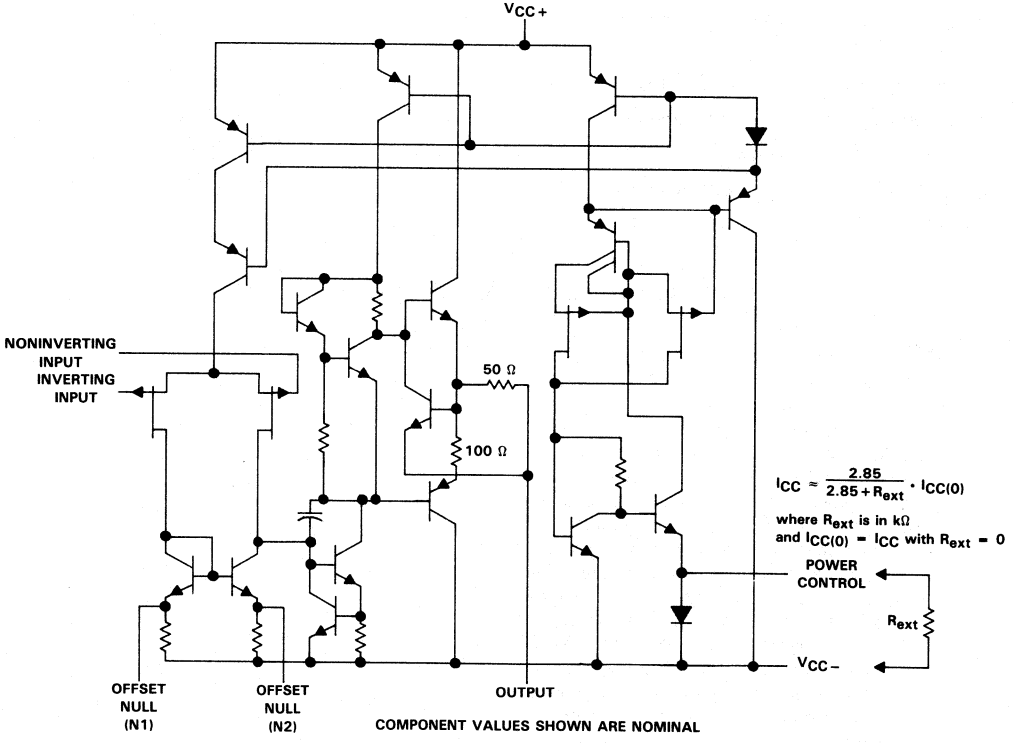
The TL066M is characterized for operation over the full military temperature range of −55°C to 125°C; the TL066I is characterized for operation from −40°C to 85°C; the TL066C, TL066AC, and TL066BC are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	15 mV	TL066CD		TL066CJG	TL066CP
	6 mV	TL066ACD		TL066ACJG	TL066ACP
	3 mV	TL066BCD		TL066BCJG	TL066BCP
−40°C to 85°C	6 mV	TL066ID		TL066IJG	TL066IP
−55°C to 125°C	6 mV		TL066MFK	TL066MJG	

The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TL066CDR).

schematic



COMPONENT VALUES SHOWN ARE NOMINAL

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ıbsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL066M	TL066I	TL066C, TL066AC, TL066BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Voltage between power-control terminal and V_{CC-}		±0.5	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
JG (TL066M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†		TL066M			TL066I			TL066C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, T_A = 25°C	R_S = 50 Ω,		3	6		3	6		3	15	mV
		V_O = 0, T_A = full range	R_S = 50 Ω,			9			9			20	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, T_A = full range	R_S = 50 Ω,		10			10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0,	T_A = 25°C		5	100		5	100		5	200	pA
		V_O = 0,	T_A = full range			20			10			5	nA
I_{IB}	Input bias current‡	V_O = 0,	T_A = 25°C		30	200		30	200		30	400	pA
		V_O = 0,	T_A = full range			50			20			10	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to +15		±11.5	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		V
		T_A = full range,	R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, T_A = 25°C	V_O = ±10 V,	4	6		4	6		3	6		V/mV
		R_L ≥ 10 kΩ, T_A = full range	V_O = ±10 V,	4						3			
B_1	Unity-gain bandwidth	T_A = 25°C,	R_L = 10 kΩ		1			1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
r_o	Output resistance	T_A = 25°C,	f = 1 kHz		220			220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		80	86		70	76		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ± 15 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	95		80	95		70	95		dB
P_D	Total power dissipation	V_O = 0, T_A = 25°C	No load,		6	7.5		6	7.5		6	7.5	mW
I_{CC}	Supply current	V_O = 0, T_A = 25°C	No load,		200	250		200	250		200	250	μA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is −55°C to 125°C for TL066M; −40°C to 85°C for TL066I; and 0°C to 70°C for TL066C. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

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electrical characteristics, V_{CC} = ±15 V

PARAMETER		TEST CONDITIONS†		TL066AC			TL066BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, T_A = 25°C	R_S = 50 Ω,		3	6		2	3	mV
		V_O = 0, T_A = full range	R_S = 50 Ω,			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, T_A = full range	R_S = 50 Ω,		10			10		μV/°C
I_{IO}	Input offset current‡	V_O = 0,	T_A = 25°C		5	100		5	100	pA
		V_O = 0,	T_A = full range			3			3	nA
I_{IB}	Input bias current‡	V_O = 0,	T_A = 25°C		30	200		30	200	pA
		V_O = 0,	T_A = full range			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11.5	−12 to ±15		±11.5	−12 to ±15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L ≥ 10 kΩ,	±10	±13.5		±10	±13.5		V
		T_A = full range,	R_L ≥ 10 kΩ	±10	±13.5		±10	±13.5		
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 10 kΩ, T_A = 25°C	V_O = ±10 V,	4	6		4	6		V/mV
		R_L ≥ 10 kΩ, T_A = full range	V_O = ±10 V,	4			4			
B_1	Unity-gain bandwidth	T_A = 25°C,	R_L = 10 kΩ		1			1		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
r_o	Output resistance	T_A = 25°C,	f = 1 kHz		220			220		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	95		80	95		dB
P_D	Total power dissipation	No load, T_A = 25°C	V_O = 0,		6	7.5		6	7.5	mW
I_{CC}	Supply current	No load, T_A = 25°C	V_O = 0,		200	250		200	250	μA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range of T_A is −55°C to 125°C for TL066M; −40°C to 85°C for TL066I; and 0°C to 70°C for TL066C, TL066AC, and TL066BC. The electrical parameters are measured with the power-control terminal (pin 8) connected to V_{CC-}.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature-sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as is possible.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C, R_{ext} = 0

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 10 kΩ, See Figure 1	1.5	3.5		V/μs
t_r	Rise time	V_I = 20 mV,	R_L = 10 kΩ		0.2		μs
	Overshoot factor	C_L = 100 pF,	See Figure 1		10%		
V_n	Equivalent input noise voltage	R_S = 100 Ω,	f = 1 kHz		42		nV/√Hz

PARAMETER MEASUREMENT INFORMATION

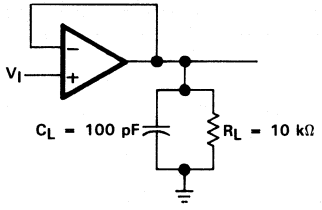

FIGURE 1. UNITY-GAIN AMPLIFIER

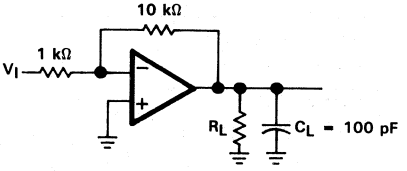

FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

INPUT OFFSET VOLTAGE NULL CIRCUIT

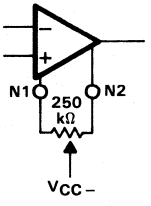

FIGURE 3

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

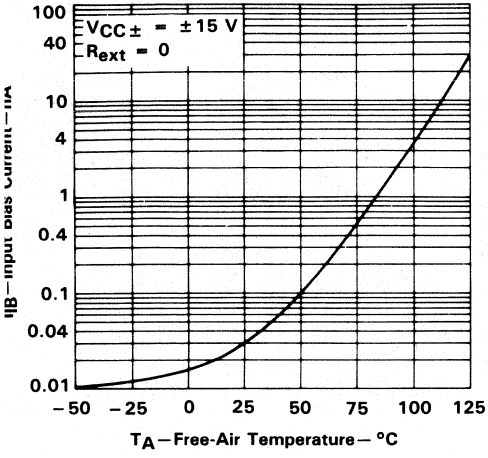

FIGURE 4

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

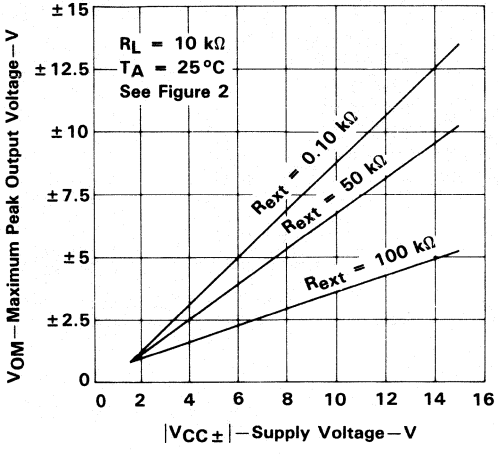

FIGURE 5

MAXIMUM PEAK OUTPUT VOLTAGE
vs
EXTERNAL CONTROL RESISTANCE

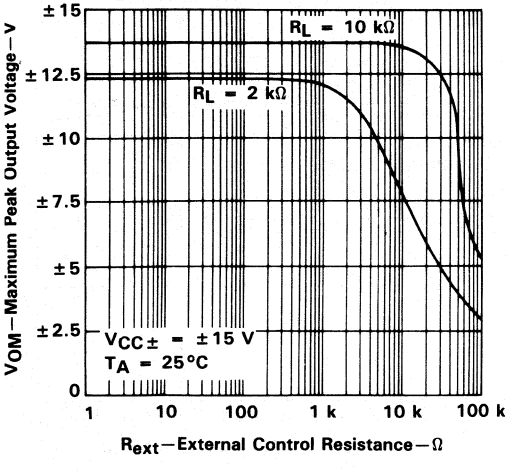

FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

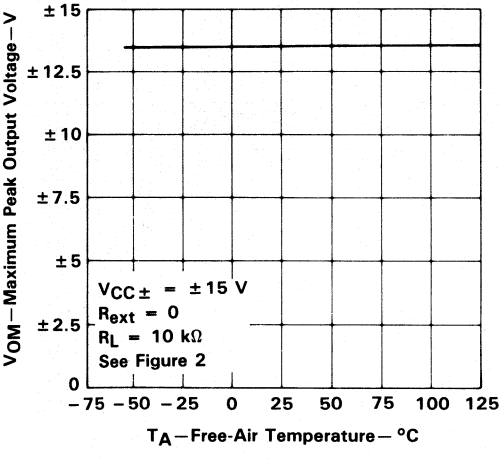

FIGURE 7

† Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

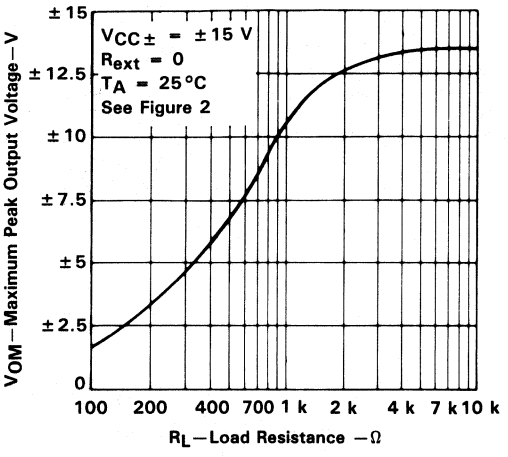

FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

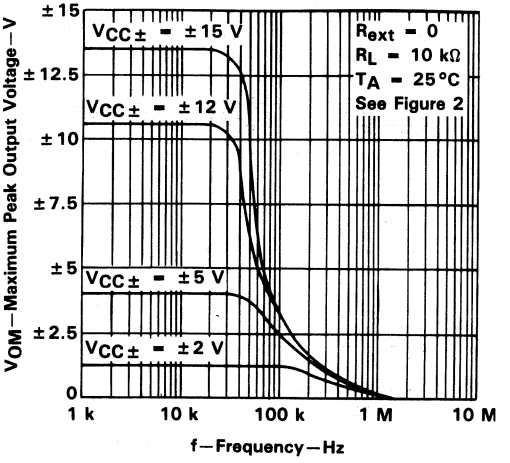

FIGURE 9

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
EXTERNAL CONTROL RESISTANCE

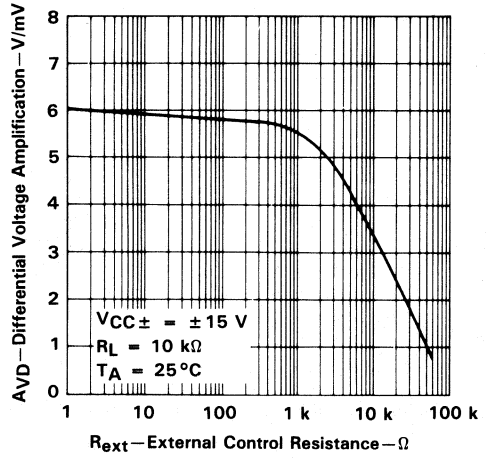

FIGURE 10

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

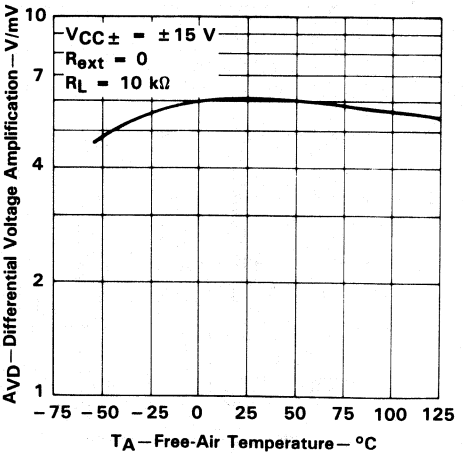

FIGURE 11

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

LARGE SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

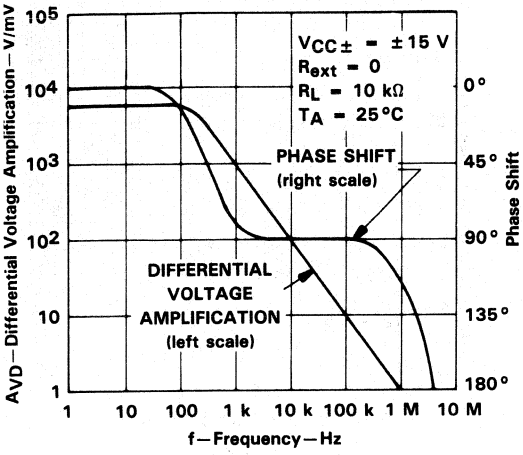

FIGURE 12

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

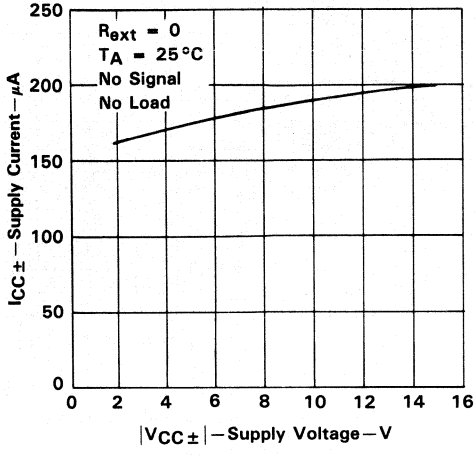

FIGURE 13

SUPPLY CURRENT
vs
EXTERNAL CONTROL RESISTANCE

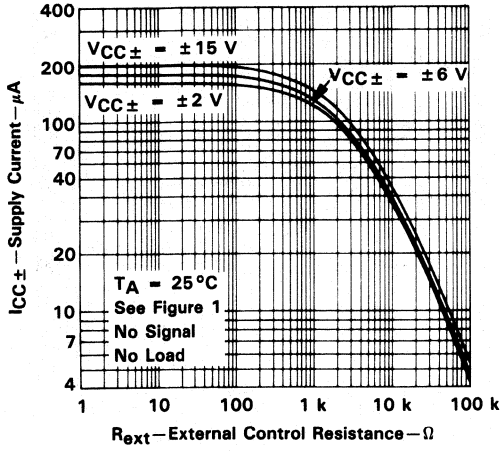

FIGURE 14

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

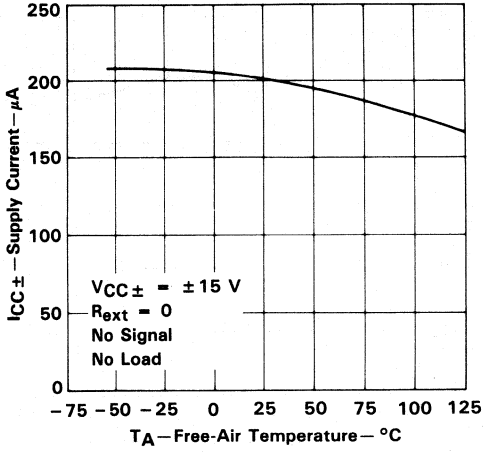

FIGURE 15

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

TOTAL POWER DISSIPATION
vs
EXTERNAL CONTROL RESISTANCE

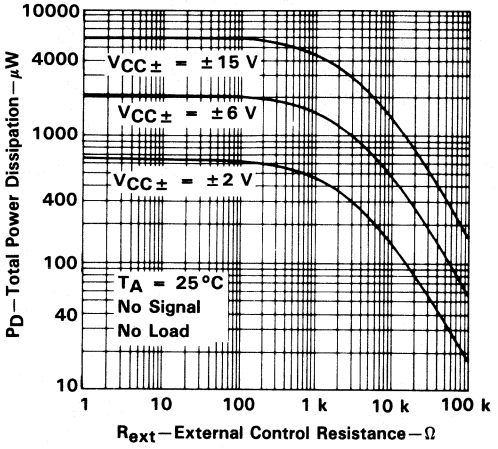

FIGURE 16

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
EXTERNAL CONTROL RESISTANCE

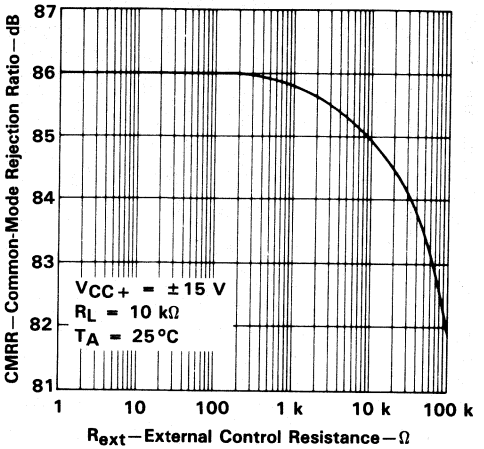

FIGURE 17

ALL EXCEPT TL066C
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

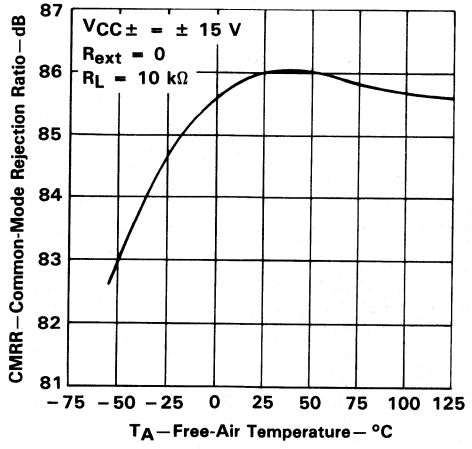

FIGURE 18

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

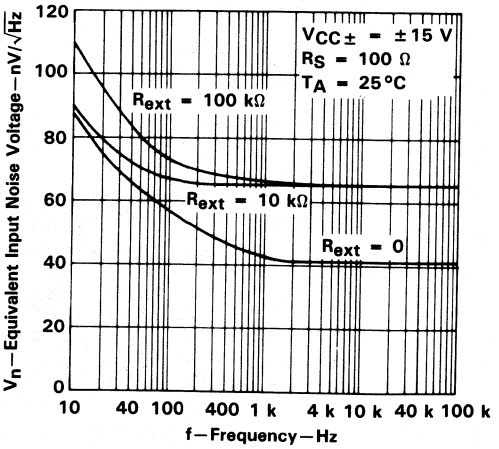

FIGURE 19

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

EQUIVALENT INPUT NOISE VOLTAGE
vs
SOURCE RESISTANCE

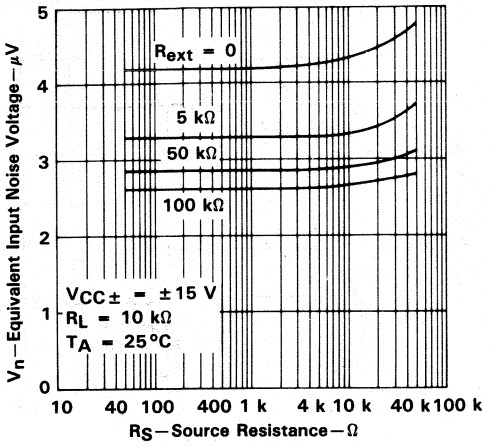

FIGURE 20

UNITY GAIN BANDWIDTH
vs
EXTERNAL CONTROL RESISTANCE

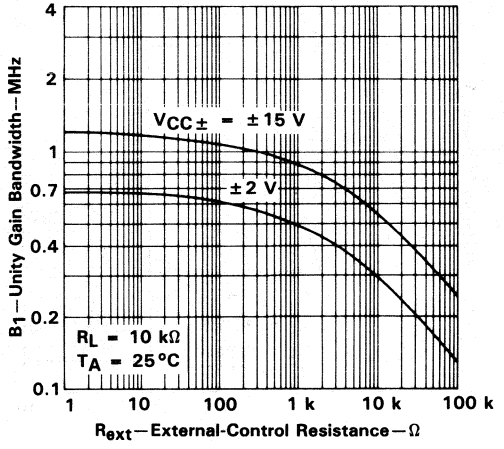

FIGURE 21

SLEW RATE
vs
EXTERNAL CONTROL RESISTANCE

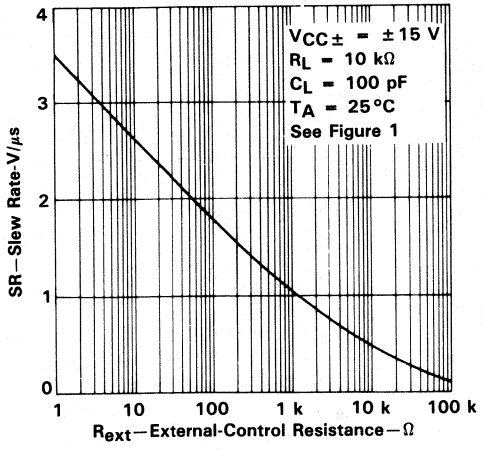

FIGURE 22

NORMALIZED UNITY GAIN BANDWIDTH
SLEW RATE, AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

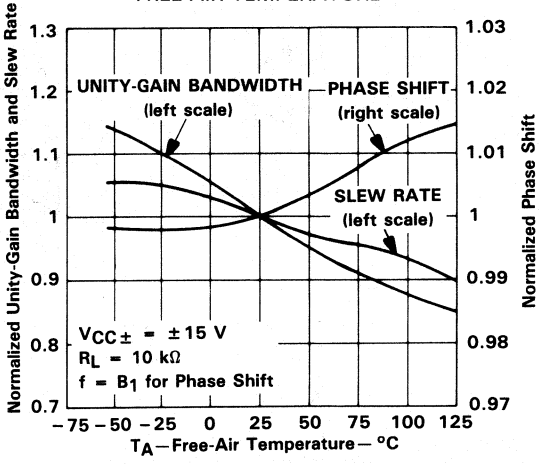

FIGURE 23

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE

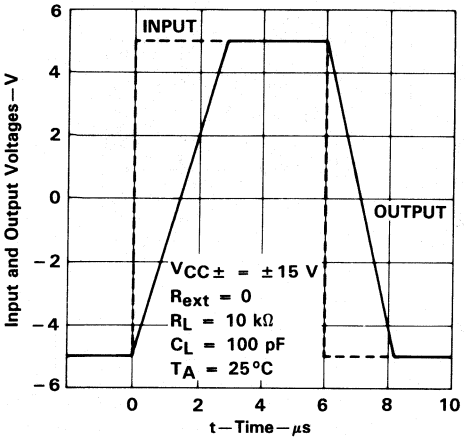

FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

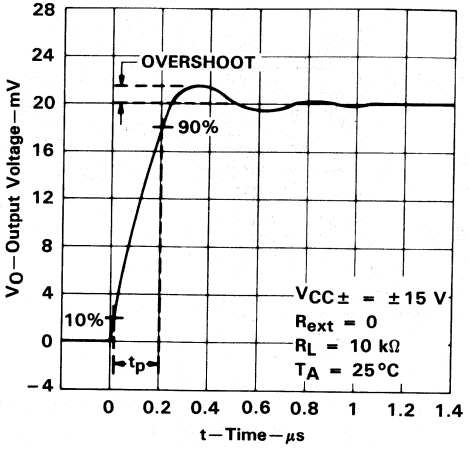

FIGURE 25

†Data at high and low temperatures are applicable only within the rated free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

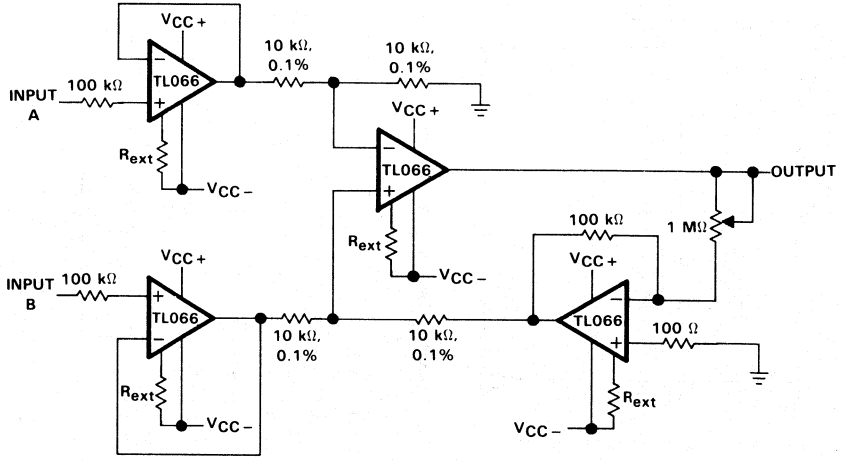

FIGURE 26. INSTRUMENTATION AMPLIFIER

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TYPICAL APPLICATION DATA

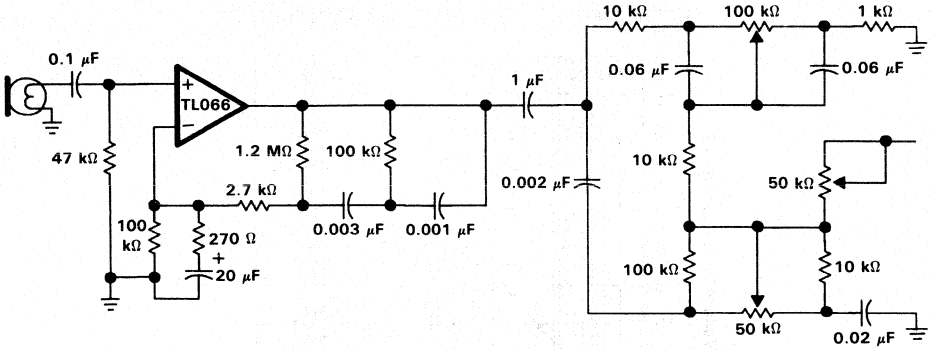

FIGURE 27. MICROPHONE PREAMPLIFIER WITH TONE CONTROL

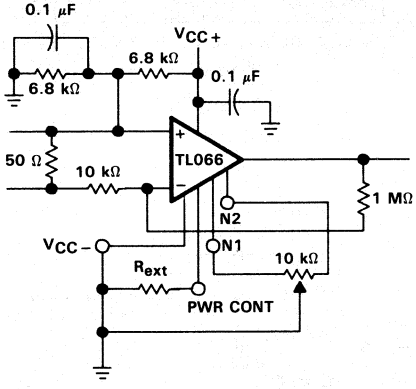

FIGURE 28. AC AMPLIFIER

TYPICAL APPLICATION DATA

IC PREAMPLIFIER RESPONSE CHARACTERISTICS

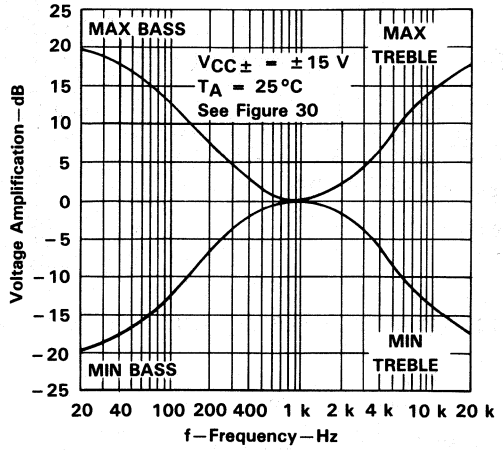

FIGURE 29

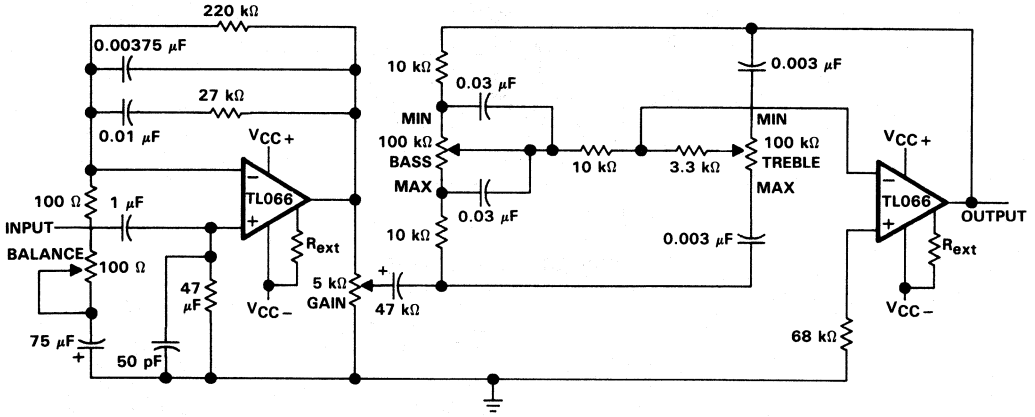

FIGURE 30. IC PREAMPLIFIER

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19 DEVICES COVER COMMERCIAL, INDUSTRIAL, AND MILITARY TEMPERATURE RANGES

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion . . . 0.003% Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**
- **Low Noise . . . V_n = 18 nV/$\sqrt{Hz}$ Typ**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation (Except TL070, TL070A)**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 13 V/μs Typ**

description

The JFET-input operational amplifiers in the TL07__ series are designed as low-noise versions of the TL08__ series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07__ series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

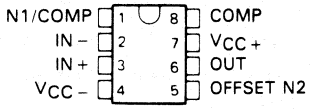
The M suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I suffix devices are characterized for operation from −40°C to 85°C, and the C suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

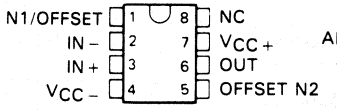
T_A	V_{IO} MAX AT 25°C	PACKAGE							
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (N)	PLASTIC DIP (P)	FLAT PACK (W)
0°C to 70°C	10 mV	TL070CD			TL070CJG			TL070CP	
	6 mV	TL070ACD			TL070ACJG			TL070ACP	
	10 mV	TL071CD			TL071CJG			TL071CP	
	6 mV	TL071ACD			TL071ACJG			TL071ACP	
	3 mV	TL071BCD			TL071BCJG			TL071BCP	
	10 mV	TL072CD			TL072CJG			TL072CP	
	6 mV	TL072ACD			TL072ACJG			TL072ACP	
	3 mV	TL072BCD			TL072BCJG			TL072BCP	
	10 mV	TL074CD		TL074CJ			TL074CN		
	6 mV	TL074ACD		TL074ACJ			TL074ACN		
	3 mV	TL074BCD		TL074BCJ			TL074BCN		
	10 mV						TL075CN		
−40°C to 85°C	6 mV	TL070ID			TL070IJG			TL070IP	
	6 mV	TL071ID			TL071IJG			TL071IP	
	6 mV	TL072ID			TL072IJG			TL072IP	
	6 mV	TL074ID		TL074IJ			TL074IN		
−55°C to 125°C	6 mV		TL071MFK		TL071MJG	TL071ML			
	6 mV		TL072MFK		TL072MJG	TL072ML			
	9 mV		TL074MFK	TL074MJ					TL074MW

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL071CDR).

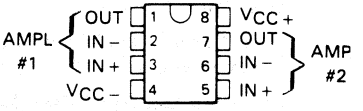
TL070, TL070A
D, JG, OR P PACKAGE
(TOP VIEW)



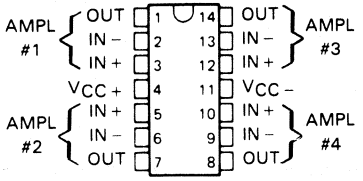
TL071, TL071A, TL071B
D, JG, OR P PACKAGE
(TOP VIEW)



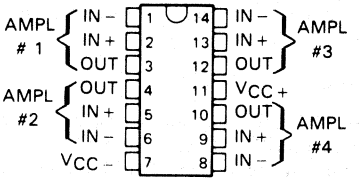
TL072, TL072A, TL072B
D, JG, OR P PACKAGE
(TOP VIEW)



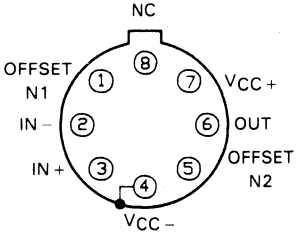
TL074, TL074A, TL074B
D, J, OR N PACKAGE
TL074 . . . W PACKAGE
(TOP VIEW)



TL075
N PACKAGE
(TOP VIEW)

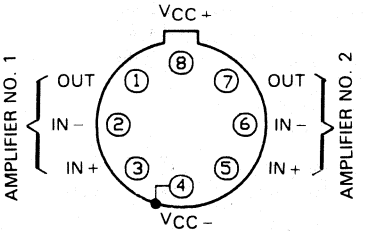


TL071 . . . L PACKAGE
(TOP VIEW)



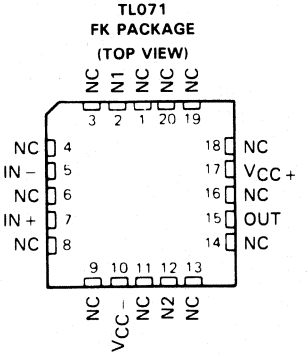
PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TL072 . . . L PACKAGE
(TOP VIEW)

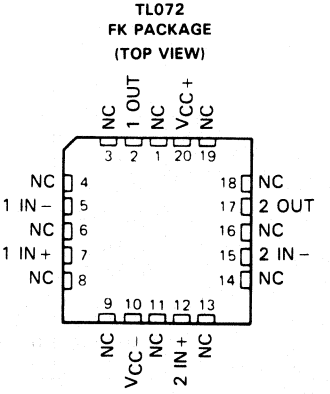


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

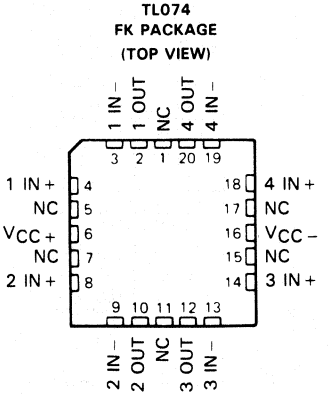
TL071
FK PACKAGE
(TOP VIEW)



TL072
FK PACKAGE
(TOP VIEW)



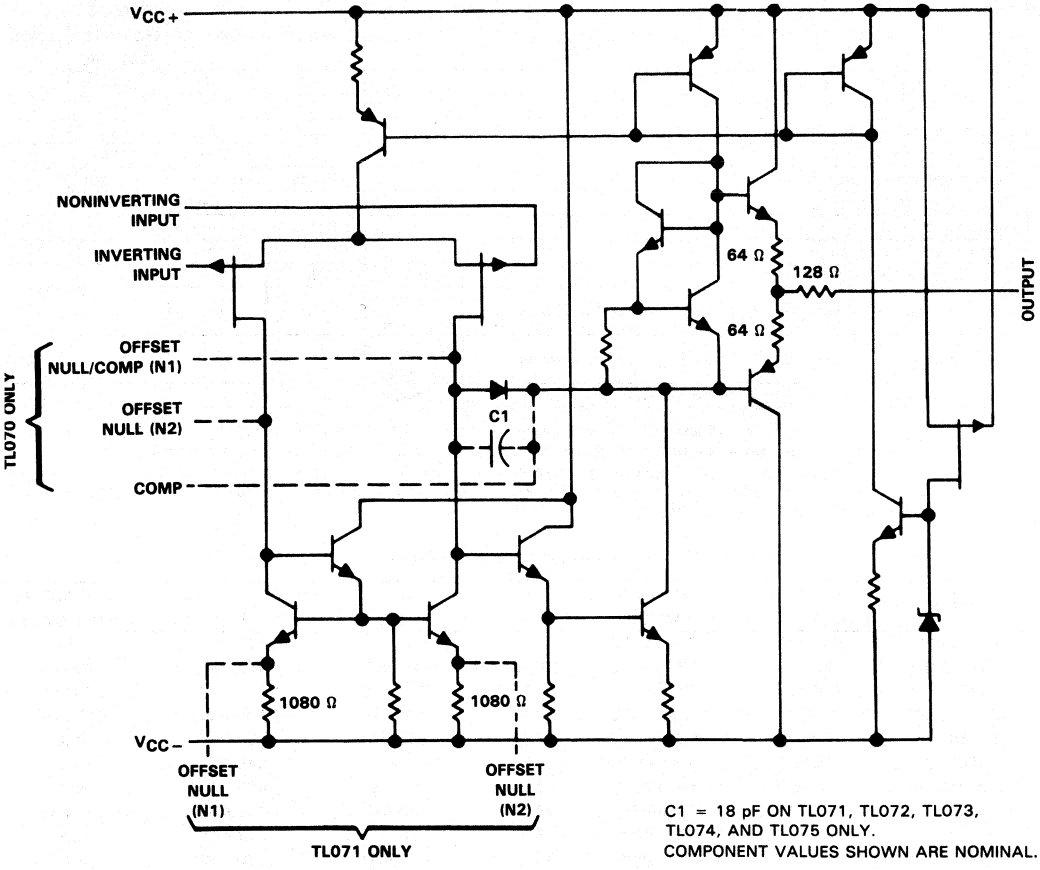
TL074
FK PACKAGE
(TOP VIEW)



NC – No internal connection.

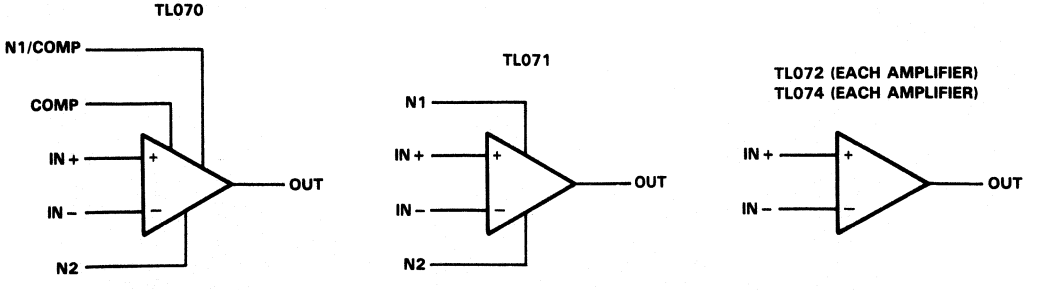
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

schematic (each amplifier)



C1 = 18 pF ON TL071, TL072, TL073, TL074, AND TL075 ONLY.
COMPONENT VALUES SHOWN ARE NOMINAL.

symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL07_M	TL07_I	TL07_C TL07_AC TL07_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or W package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300			°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8-pin)	680 mW	5.8 mW/°C	33°C	464 mW	377 mW	N/A
D (14-pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL07_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL07_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
L	680 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A
W	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	200 mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

lectrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL071M TL072M			TL074M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω,	T_A = 25°C		3	6		3	9	mV
			T_A = −55°C to 125°C			9			15	
αV_{IO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = −55°C to 125°C			18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100	pA
			T_A = −55°C to 125°C			20			20	nA
I_{IB}	Input bias current	V_O = 0	T_A = 25°C		65	200		65	200	pA
			T_A = −55°C to 125°C			50			50	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = −55°C to 125°C	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	35	200		35	200		V/mV
			T_A = −55°C to 125°C	15			15			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL070I TL071I TL072I TL074I			TL070C TL071C TL072C TL074C			TL070AC TL071AC TL072AC TL074AC			TL070BC TL071BC TL072BC TL074BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	10		3	6		2	3	mV
			T_A = full range			8			13			7.5			5	
αV_{IO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω, T_A = full range			18			18			18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	100		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		65	200		65	200		65	200		65	200	pA
			T_A = full range			20			7			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		±11	−12 to +15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	T_A = 25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	T_A = full range	±12			±12			±12			±12			
		R_L ≥ 2 kΩ		±10			±10			±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	T_A = 25°C	50	200		25	200		50	200		50	200		V/mV
			T_A = full range	25			15			25			25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	100		70	100		80	100		80	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, V_O = 0, R_S = 50 Ω, T_A = 25°C		80	100		70	100		80	100		80	100		dB
I_{CC}	Supply current (each amplifier)	No load, V_O = 0, T_A = 25°C			1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, T_A = 25°C			120			120			120			120		dB

†All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL07__I and 0°C to 70°C for TL07__C, TL07__AC, and TL07__BC.

‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 6. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

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Operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		TL07_M			ALL OTHERS			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	8	13		8	13		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		μs
	overshoot factor				20			20		%
V_n	Equivalent input noise voltage	R_S = 100 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		μV
I_n	Equivalent input noise current	R_S = 100 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, $R_L \geq$ 2 kΩ,	$R_S \leq$ 1 kΩ, f = 1 kHz		0.003			0.003		%

PARAMETER MEASUREMENT INFORMATION

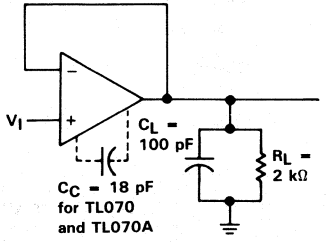

FIGURE 1. UNITY-GAIN AMPLIFIER

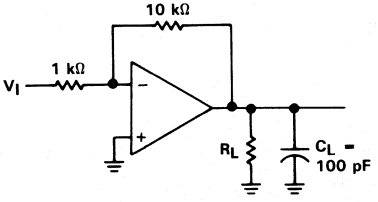

FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

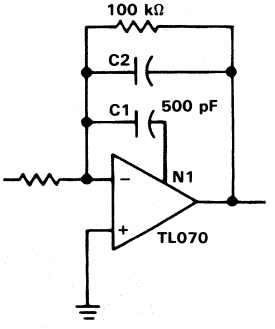

FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

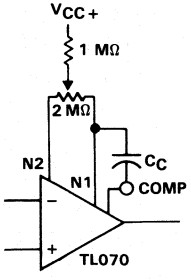

FIGURE 4

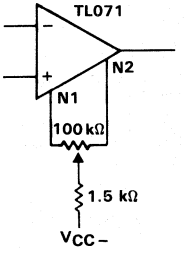

FIGURE 5

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

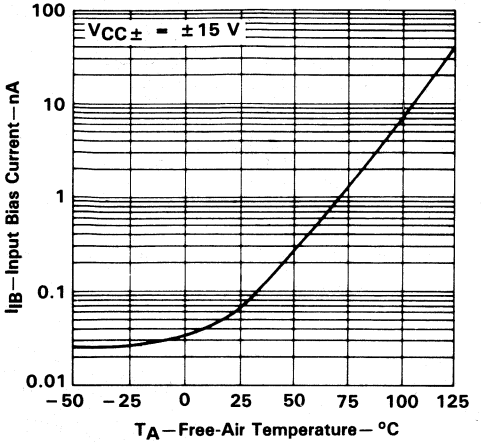

FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

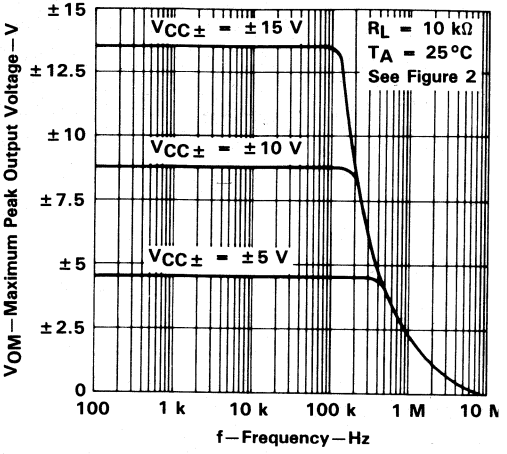

FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

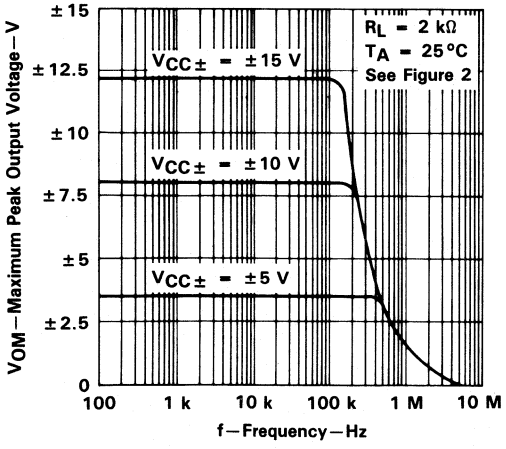

FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

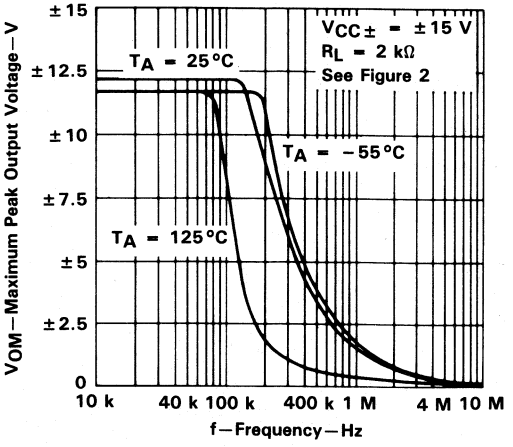

FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

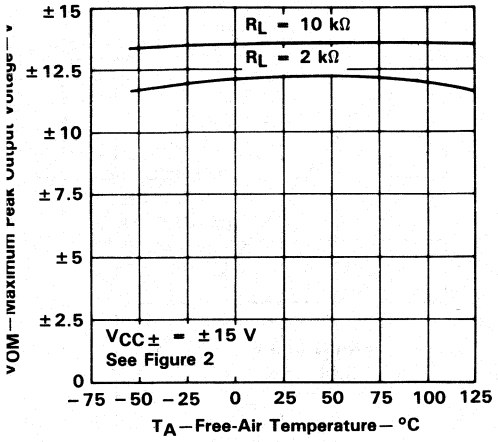

FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

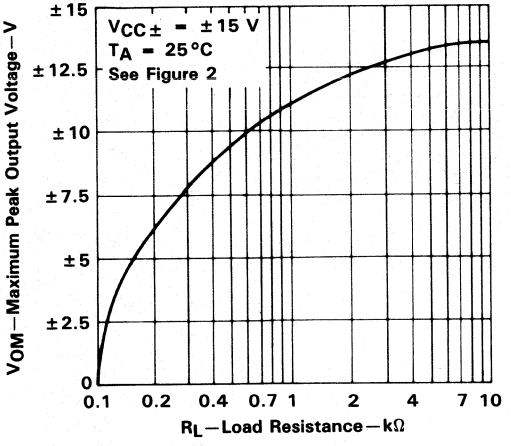

FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

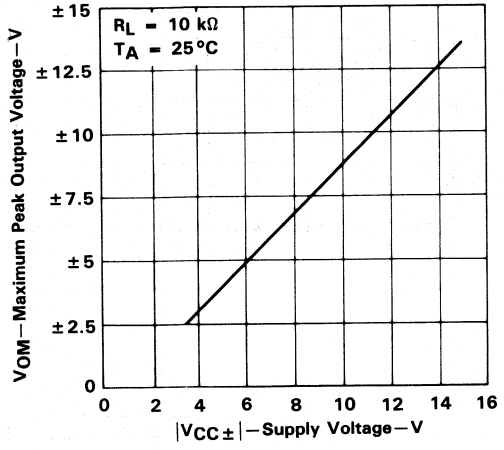

FIGURE 12

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

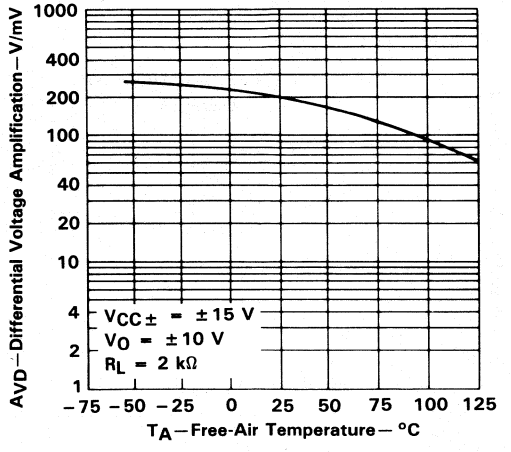

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

TYPICAL CHARACTERISTICS†

TL070
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

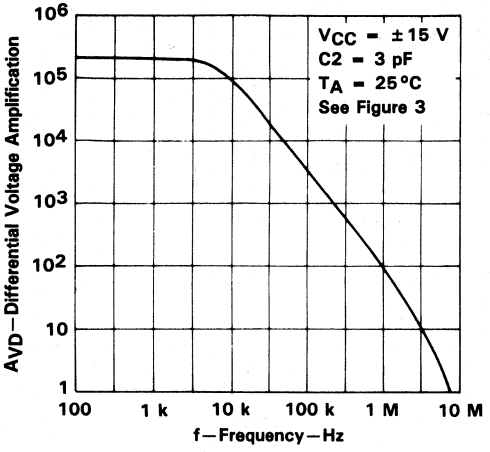

FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

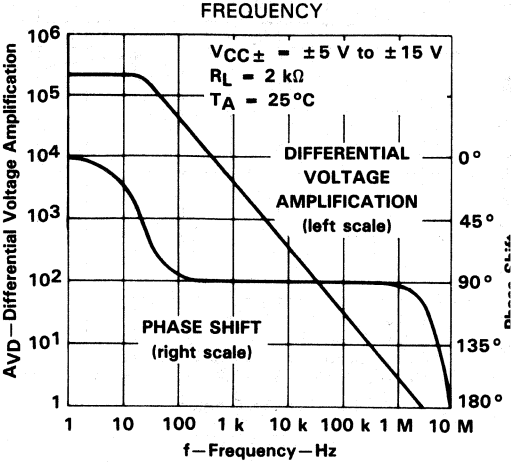

FIGURE 15

NORMALIZED UNITY-GAIN BANDWIDTH
and PHASE SHIFT
vs
FREE-AIR TEMPERATURE

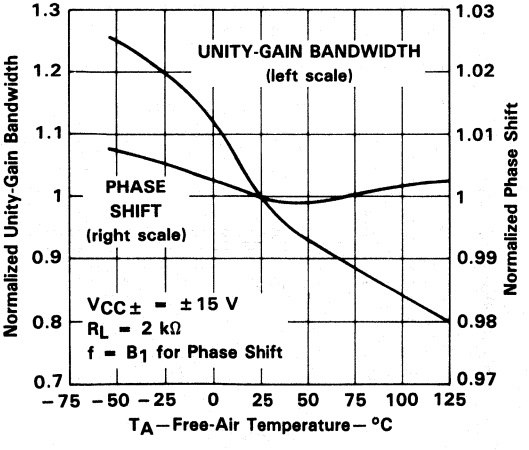

FIGURE 16

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

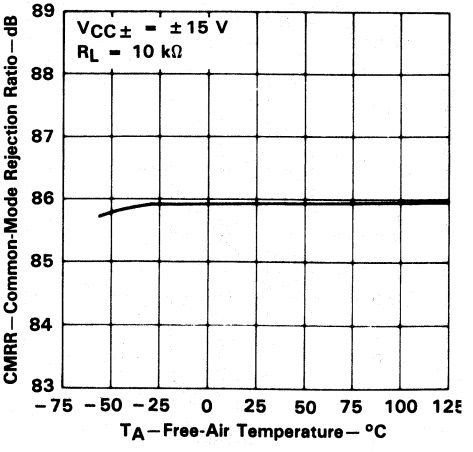

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

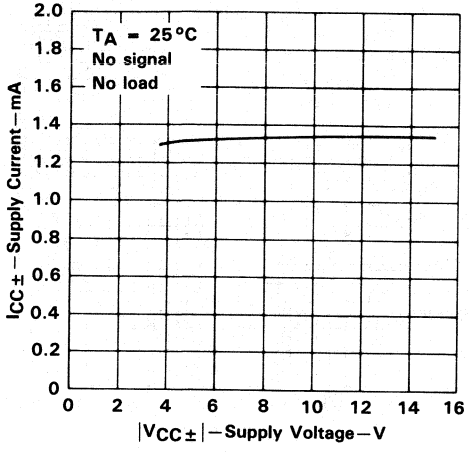

FIGURE 18

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

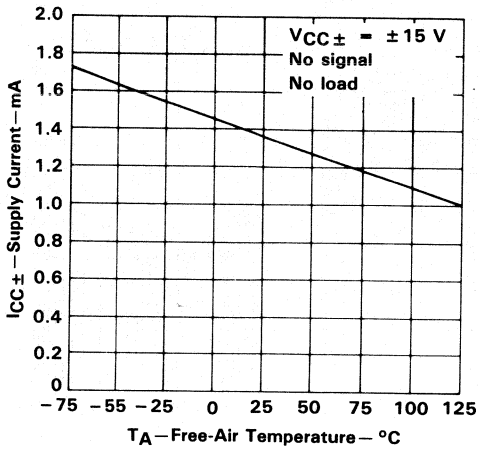

FIGURE 19

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

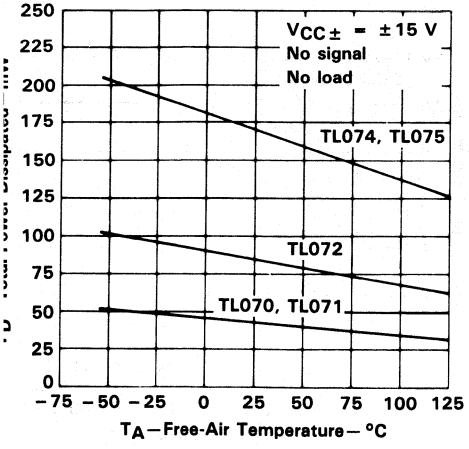

FIGURE 20

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

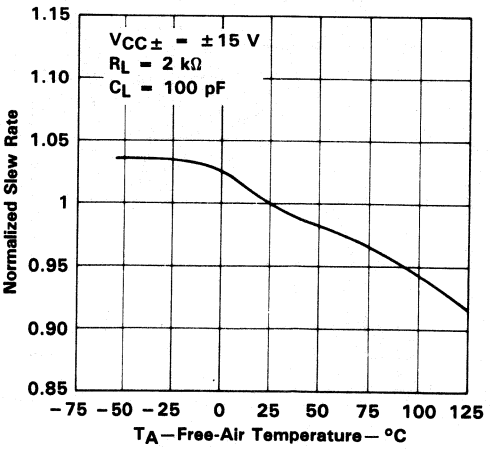

FIGURE 21

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. An 18-pF compensation capacitor is used with TL070 and TL070A.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

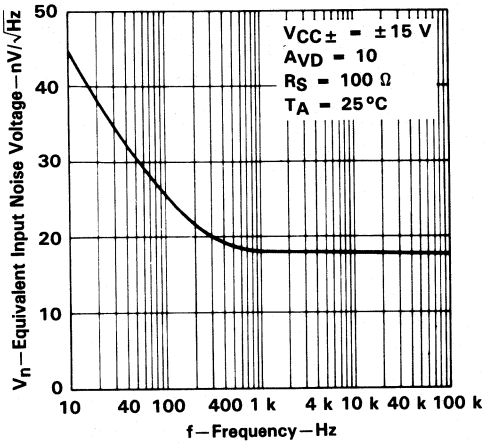

FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

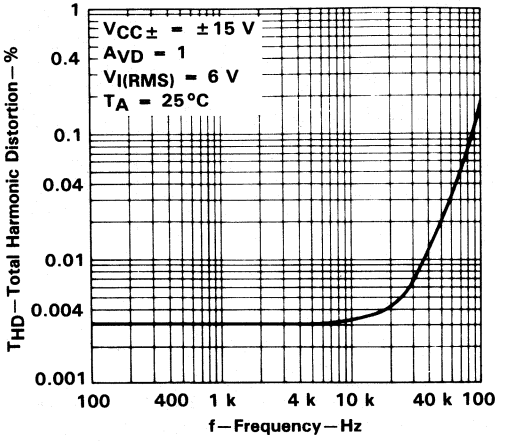

FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

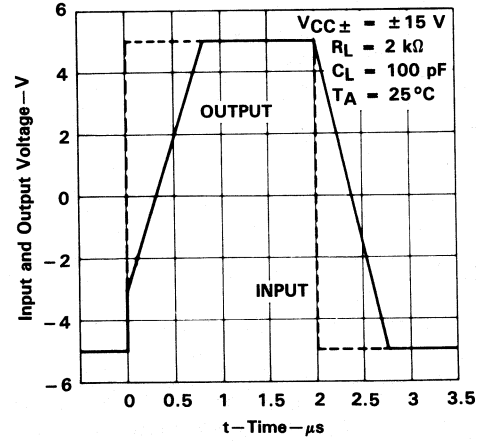

FIGURE 24

OUTPUT VOLTAGE
vs
ELAPSED TIME

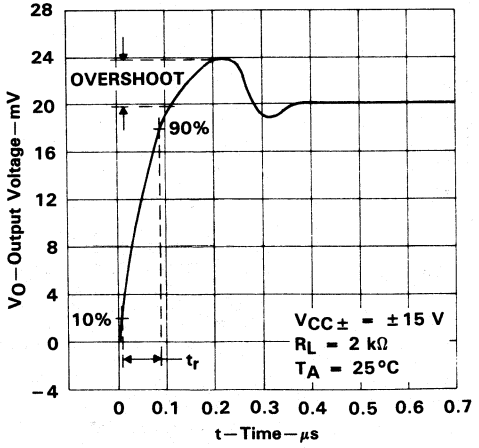

FIGURE 25

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TYPICAL APPLICATION DATA

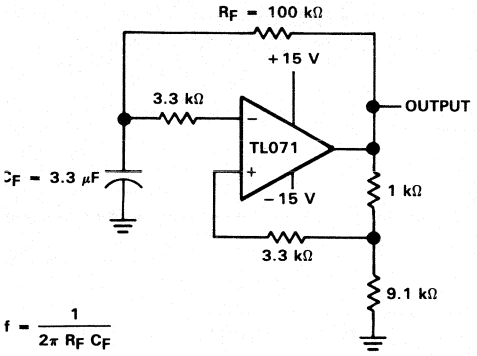


FIGURE 26. 0.5-Hz SQUARE-WAVE OSCILLATOR

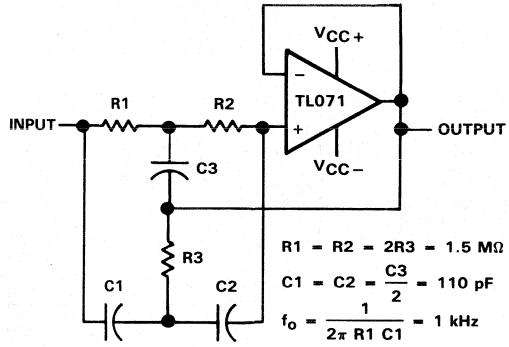
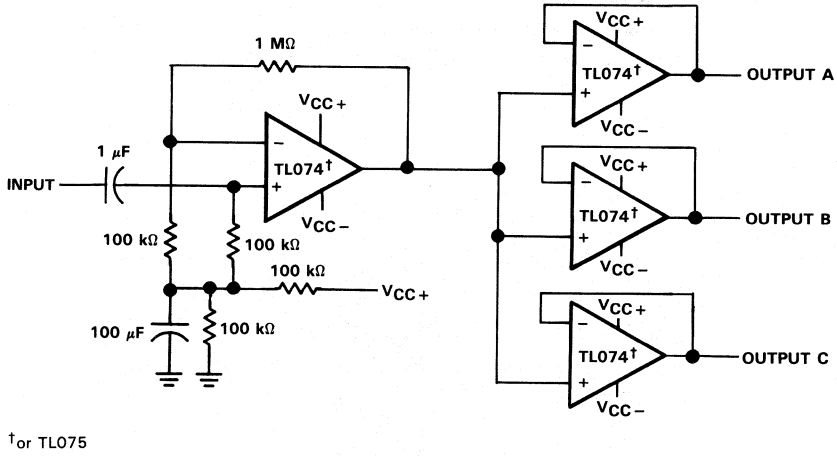


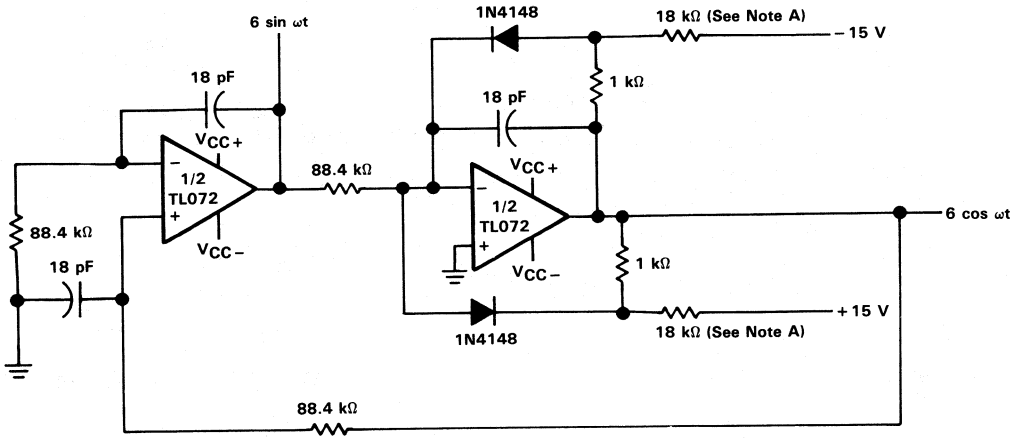
FIGURE 27. HIGH-Q NOTCH FILTER



†or TL075

FIGURE 28. AUDIO DISTRIBUTION AMPLIFIER

TYPICAL APPLICATION DATA



Note A: These resistor values may be adjusted for a symmetrical output.

FIGURE 29. 100-kHz QUADRATURE OSCILLATOR

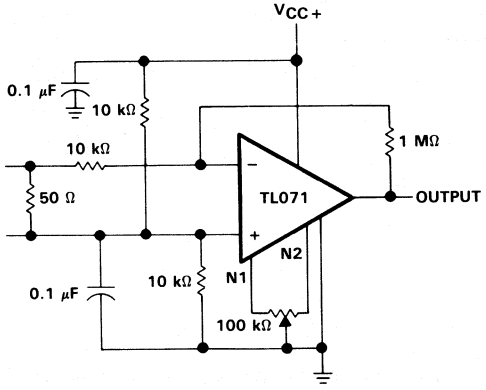


FIGURE 30. AC AMPLIFIER

TYPICAL APPLICATION DATA

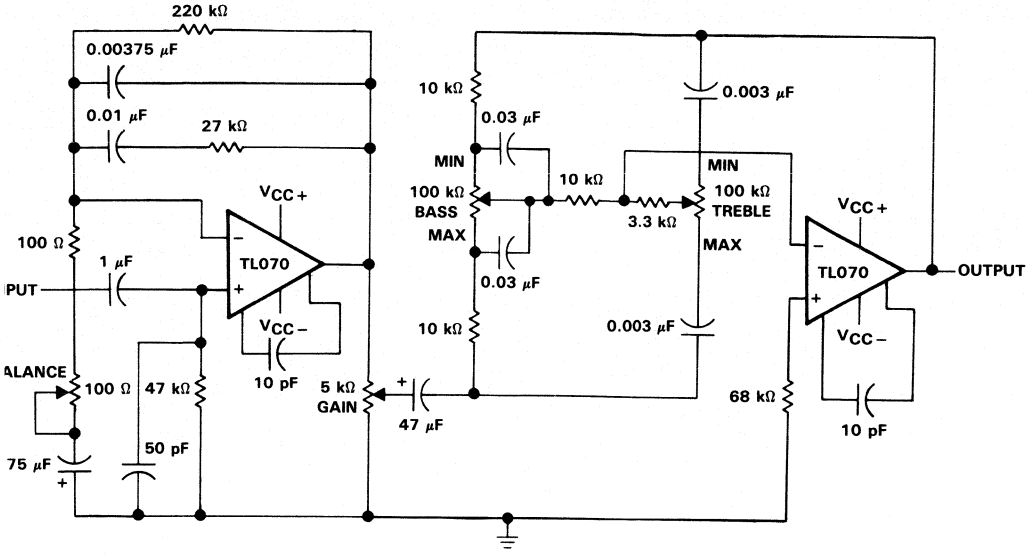


FIGURE 31. IC PREAMPLIFIER

IC PREAMPLIFIER
RESPONSE CHARACTERISTICS

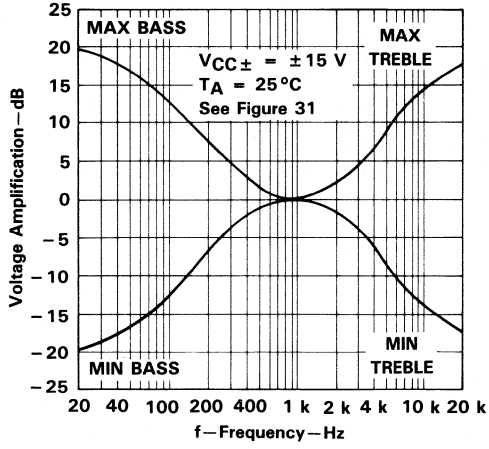


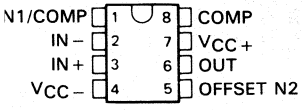
FIGURE 32

2 Operational Amplifiers

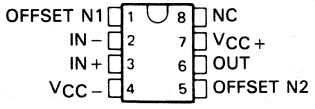
24 DEVICES COVER MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

- Low-Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation (Except TL080, TL080A)
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/μs Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

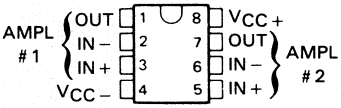
TL080, TL080A
D, JG, OR P PACKAGE
(TOP VIEW)



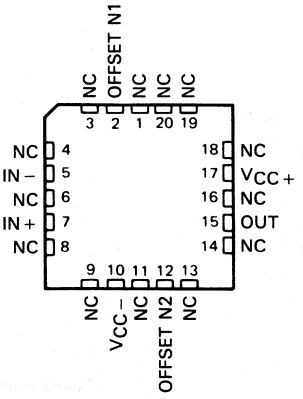
TL081, TL081A, TL081B
D, JG, OR P PACKAGE
(TOP VIEW)



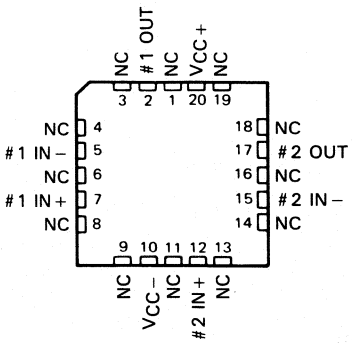
TL082, TL082A, TL082B
D, JG, OR P PACKAGE
(TOP VIEW)



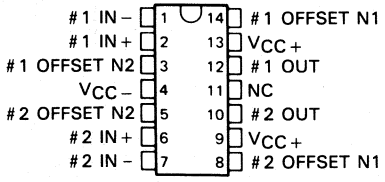
TL081M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



TL082M . . . FK CHIP CHARRIER PACKAGE
(TOP VIEW)

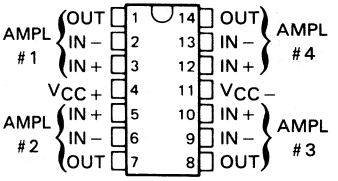


TL083, TL083A
D, J, OR N PACKAGE
(TOP VIEW)



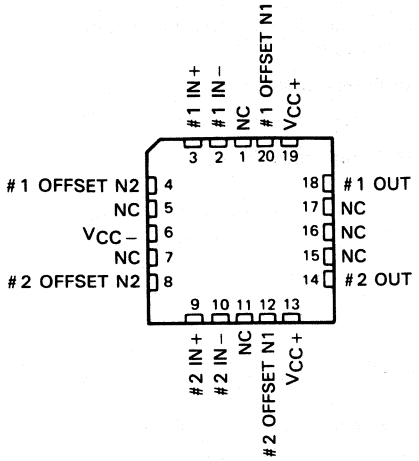
Pins 9 and 13 are internally interconnected

TL084, TL084A, TL084B
D, J, OR N PACKAGE
(TOP VIEW)

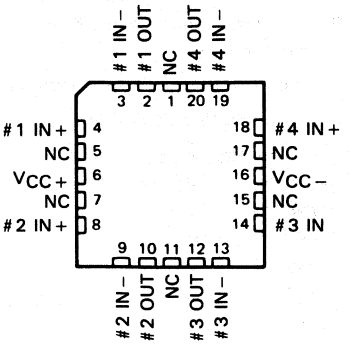


NC—No internal connection

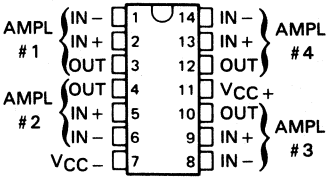
TL083M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



TL084M . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



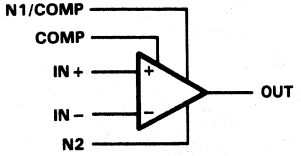
TL085
N PACKAGE
(TOP VIEW)



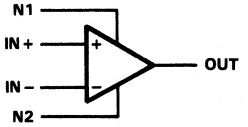
NC—No internal connection

symbols

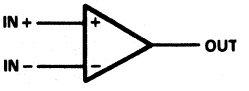
TL080



TL081
TL083 (each amplifier)



TL082 (each amplifier)
TL084 (each amplifier)
TL085 (each amplifier)



lescription

The TL08_ JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08_ family.

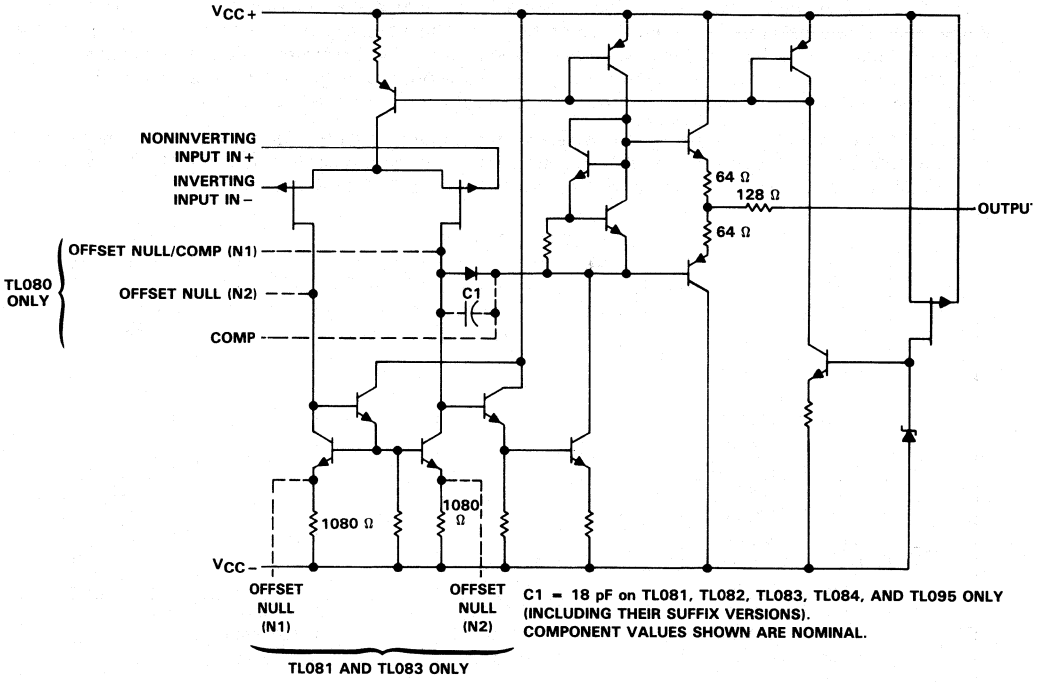
Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −40°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C TO 70°C	15 mV	TL080CD			TL080CJG		TL080CP
	6 mV	TL080ACD			TL080ACJG		TL080ACP
	15 mV	TL081CD			TL081CJG		TL081CP
	6 mV	TL081ACD			TL081ACJG		TL081ACP
	3 mV	TL081BCD			TL081BCJG		TL081BCP
	15 mV	TL082CD			TL082CJG		TL082CP
	6 mV	TL082ACD			TL082ACJG		TL082ACP
	3 mV	TL082BCD			TL082BCJG		TL082BCP
	15 mV	TL083CD		TL083CJ		TL083CN	
	6 mV	TL083ACD		TL083ACJ		TL083ACN	
	15 mV	TL084CD		TL084CJ		TL084CN	
	6 mV	TL084ACD		TL084ACJ		TL084ACN	
	3 mV	TL084BCD		TL084BCJ		TL084BCN	
	15 mV					TL085CN	
−40°C TO 85°C	6 mV	TL080ID			TL080IJG		TL080IP
	6 mV	TL081ID			TL081IJG		TL081IP
	6 mV	TL082ID			TL082IJG		TL082IP
	6 mV	TL083ID		TL083IJ		TL083IN	
	6 mV	TL084ID		TL084IJ		TL084IN	
−55°C TO 125°C	6 mV				TL080MJG		
	6 mV		TL081MFK		TL081MJG		
	6 mV		TL082MFK		TL082MJG		
	6 mV		TL083MFK	TL083MJ			
	9 mV		TL084MFK	TL084MJ			

The D package is available taped and reeled. Add "R" suffix to device type (e.g., TL080CDR).

schematic (each amplifier)



C1 = 18 pF on TL081, TL082, TL083, TL084, AND TL095 ONLY (INCLUDING THEIR SUFFIX VERSIONS).
COMPONENT VALUES SHOWN ARE NOMINAL.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL08_M	TL08_I	TL08_C TL08_AC TL08_BC	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, N, or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8 Pin)	680 mW	5.8 mW/°C	32°C	464 mW	377 mW	N/A
D (14 Pin)	680 mW	7.6 mW/°C	60°C	608 mW	494 mW	N/A
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (TL08_M)	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	275 mW
J (all others)	680 mW	8.2 mW/°C	67°C	656 mW	533 mW	N/A
JG (TL08_M)	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW
JG (all others)	680 mW	6.6 mW/°C	47°C	528 mW	429 mW	N/A
N	680 mW	9.2 mW/°C	76°C	680 mW	598 mW	N/A
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW	N/A

electrical characteristics, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080M, TL081M TL082M, TL083M			TL084M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	$T_A = 25°C$		3	6		3	9	mV
			$T_A = -55°C$ to $125°C$			9			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $T_A = -55°C$ to $125°C$	$R_S = 50\ \Omega$,		18			18		μV/°C
I_{IO}	Input offset current‡	$V_O = 0$	$T_A = 25°C$		5	100		5	100	pA
			$T_A = 125°C$			20			20	nA
I_{IB}	Input bias current‡	$V_O = 0$	$T_A = 25°C$		30	200		30	200	pA
			$T_A = 125°C$			50			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	$T_A = 25°C$,	$R_L = 10\ k\Omega$	±12	±13.5		±12	±13.5		V
		$T_A = -55°C$ to $125°C$	$R_L \ge 10\ k\Omega$	±12			±12			
			$R_L \ge 2\ k\Omega$	±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V, $T_A = 25°C$	$R_L \ge 2\ k\Omega$,	25	200		25	200		V/mV
		$V_O = \pm 10$ V, $T_A = -55°C$ to $125°C$	$R_L \ge 2\ k\Omega$,	15			15			
B_1	Unity-gain bandwidth	$T_A = 25°C$			3			3		MHz
r_i	Input resistance	$T_A = 25°C$			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15$ V to ± 9 V, $R_S = 50\ \Omega$,	$V_O = 0$, $T_A = 25°C$	80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, $T_A = 25°C$	$V_O = 0$,		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	$A_{VD} = 100$,	$T_A = 25°C$		120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

electrical characteristics, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL080I TL081I TL082I TL083I TL084I			TL080C TL081C TL082C TL083C TL084C TL085C			TL080AC TL081AC TL082AC TL083AC TL084AC			TL081BC TL082BC TL084BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	T_A = 25°C		3	6		3	15		3	6		2	3	mV
			T_A = full range			9			20			7.5			5	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, T_A = full range	R_S = 50 Ω,		18			18			18			18		μV/°C
I_{IO}	Input offset current‡	V_O = 0	T_A = 25°C		5	100		5	200		5	100		5	100	pA
			T_A = full range			10			2			2			2	nA
I_{IB}	Input bias current‡	V_O = 0	T_A = 25°C		30	200		30	400		30	200		30	200	pA
			T_A = full range			20			10			7			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
		T_A = full range	R_L = ≥ 10 kΩ	±12			±12			±12			±12			
			R_L ≥ 2 kΩ	±10	±12		±10	±12		±10	±12		±10	±12		
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, T_A = 25°C	R_L ≥ 2 kΩ,	50	200		25	200		50	200		50	200		V/mV
		V_O = ±10 V, T_A = full range	R_L ≥ 2 kΩ,	25			15			25			25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		70	86		80	86		80	86		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±15 V to ±9 V, R_S = 50 Ω,	V_O = 0, T_A = 25°C	80	86		70	86		80	86		80	86		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0,		1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100,	T_A = 25°C		120			120			120			120		dB

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −40°C to 85°C for TL08_I and 0°C to 70°C for TL08_C, TL08_AC, and TL08_BC.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive as shown in Figure 18. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

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Operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	8	13		V/μs
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.05		μs
	Overshoot factor				20%		
V_n	Equivalent input noise voltage	R_S = 100 Ω	f = 1 kHz		18		$nV/\sqrt{Hz}$
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 100 Ω,	f = 1 kHz		0.01		$pA/\sqrt{Hz}$
THD	Total harmonic distortion	$V_{O(rms)}$ = 10 V, $R_L \geq$ 2 kΩ,	$R_S \leq$ 1 kΩ, f = 1 kHz		0.003%		

PARAMETER MEASUREMENT INFORMATION

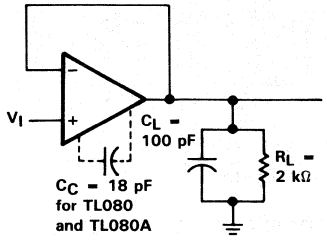

FIGURE 1. UNITY-GAIN AMPLIFIER

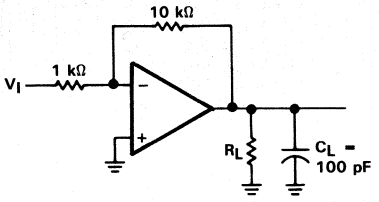

FIGURE 2. GAIN-OF-10 INVERTING AMPLIFIER

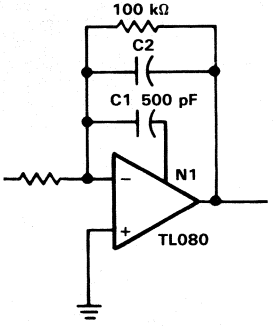

FIGURE 3. FEED-FORWARD COMPENSATION

INPUT OFFSET VOLTAGE NULL CIRCUITS

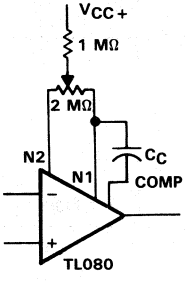

FIGURE 4

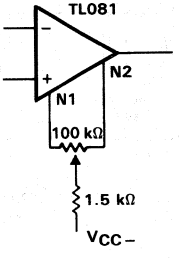

FIGURE 5

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

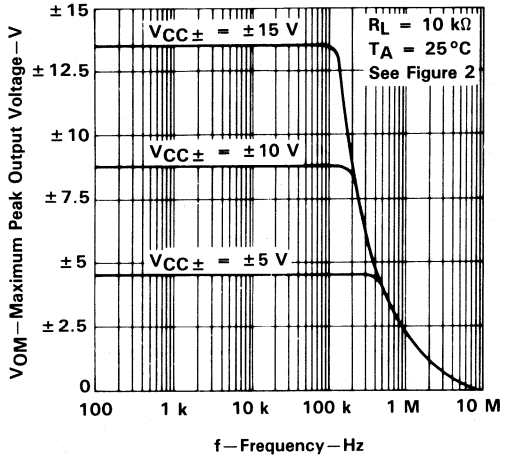

FIGURE 6

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

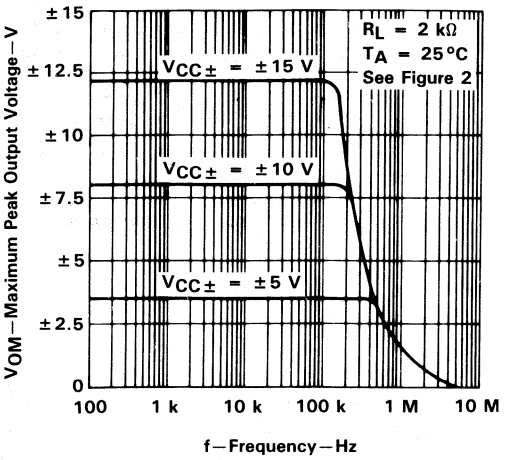

FIGURE 7

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

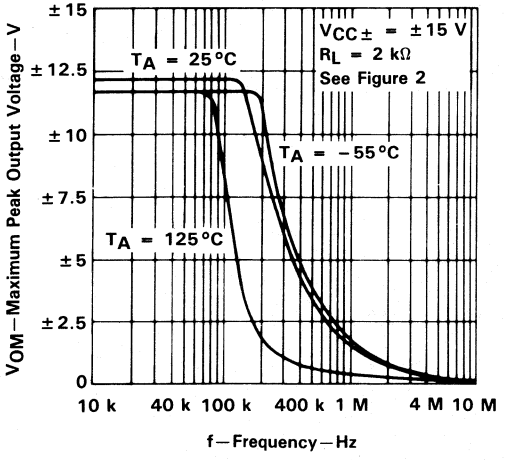

FIGURE 8

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

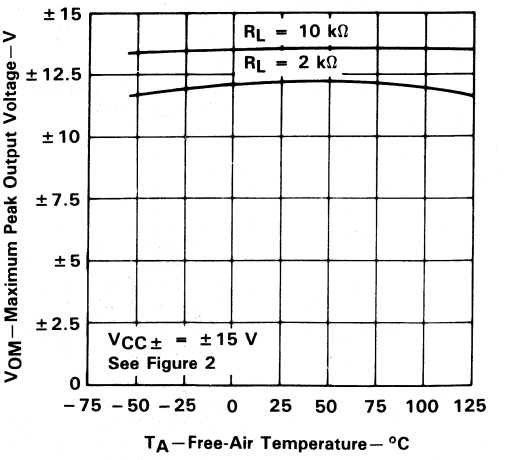

FIGURE 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

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TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

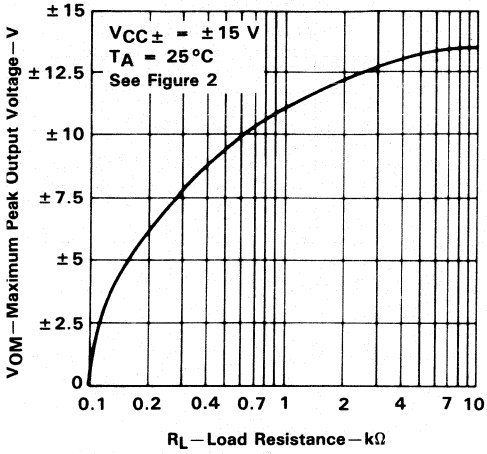

FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

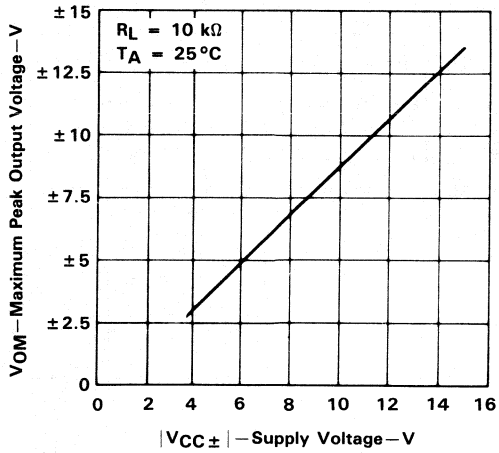

FIGURE 11

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

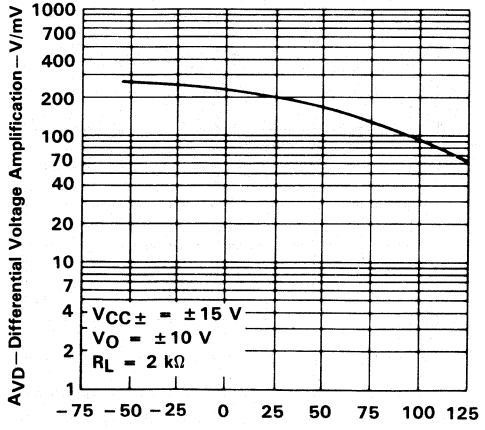

FIGURE 12

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

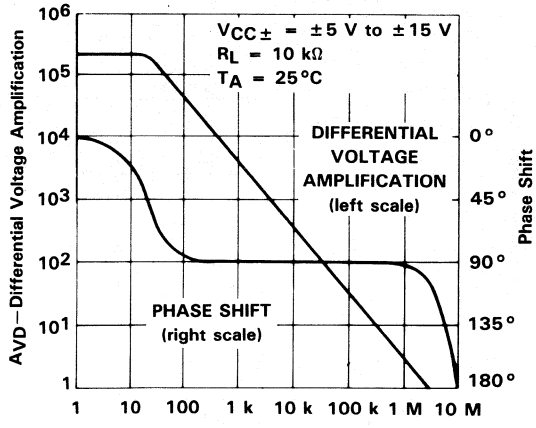

FIGURE 13

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL CHARACTERISTICS†

TL080, TL080A
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION

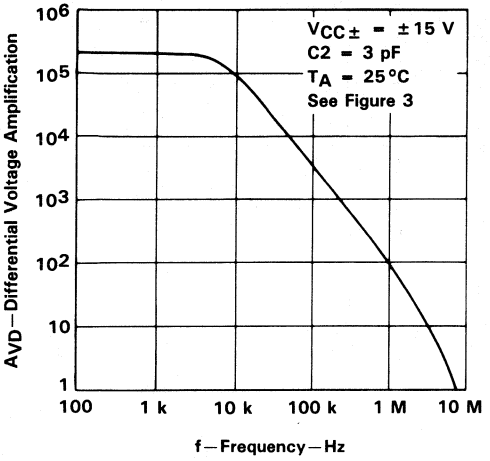

FIGURE 14

TOTAL POWER DISSIPATED
vs
FREE-AIR TEMPERATURE

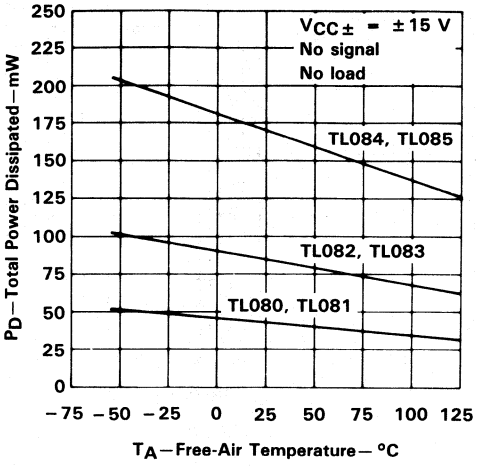

FIGURE 15

SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE

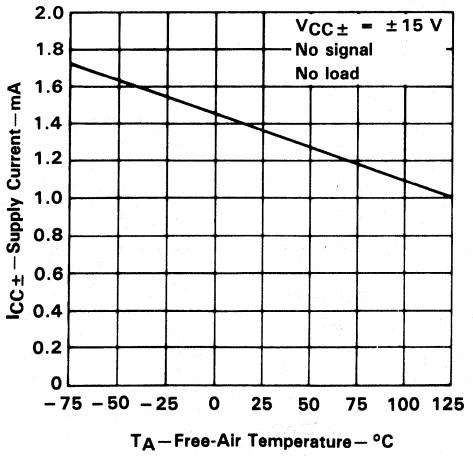

FIGURE 16

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

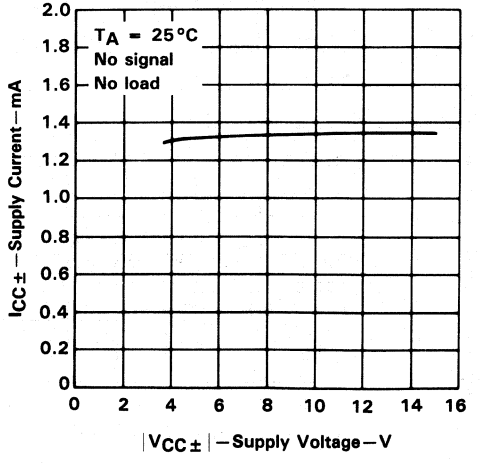

FIGURE 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

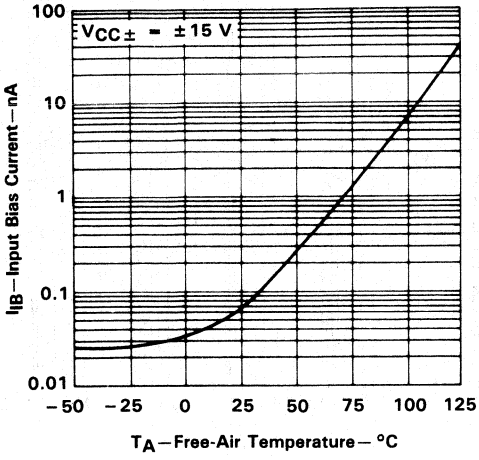


FIGURE 18

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

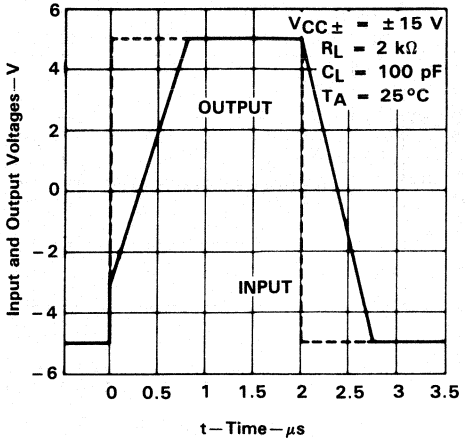


FIGURE 19

OUTPUT VOLTAGE
vs
ELAPSED TIME

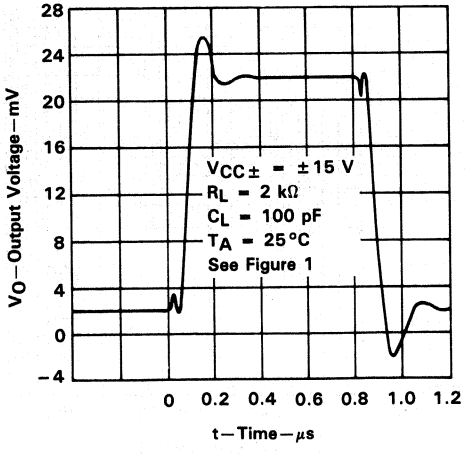


FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

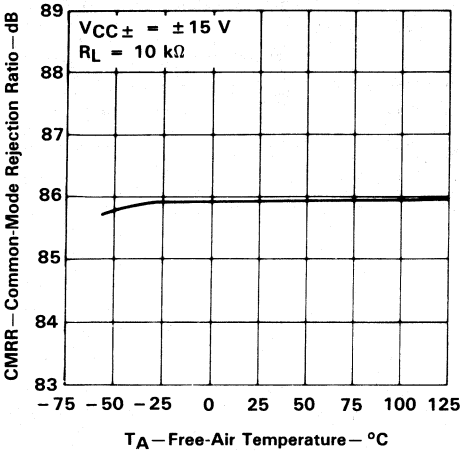


FIGURE 21

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

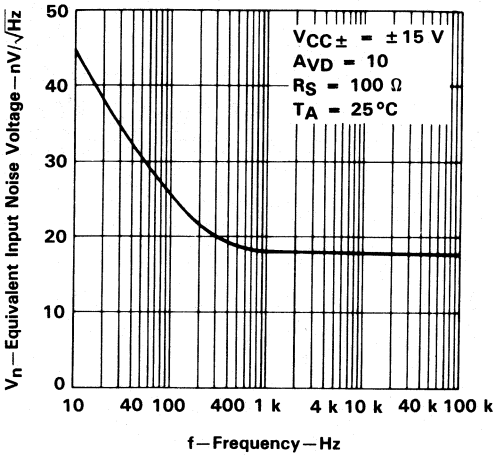


FIGURE 22

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

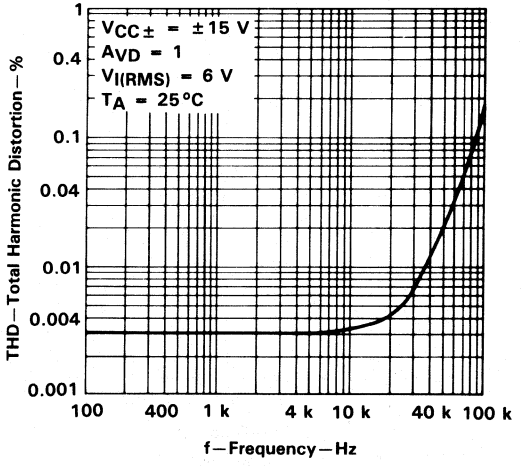


FIGURE 23

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. A 12-pF compensation capacitor is used with TL080 and TL080A.

TYPICAL APPLICATION DATA

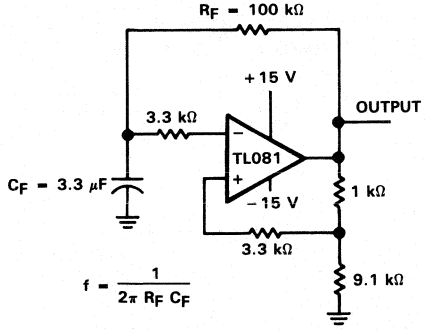


FIGURE 24. 0.5-Hz SQUARE-WAVE OSCILLATOR

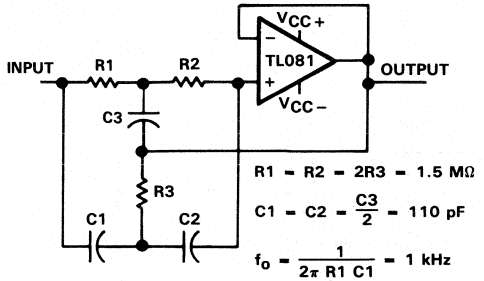
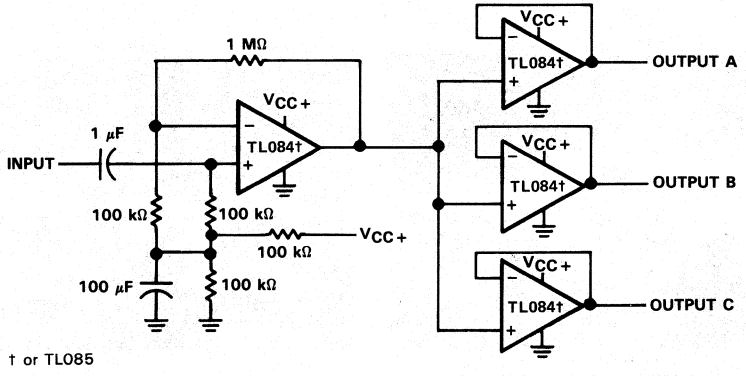
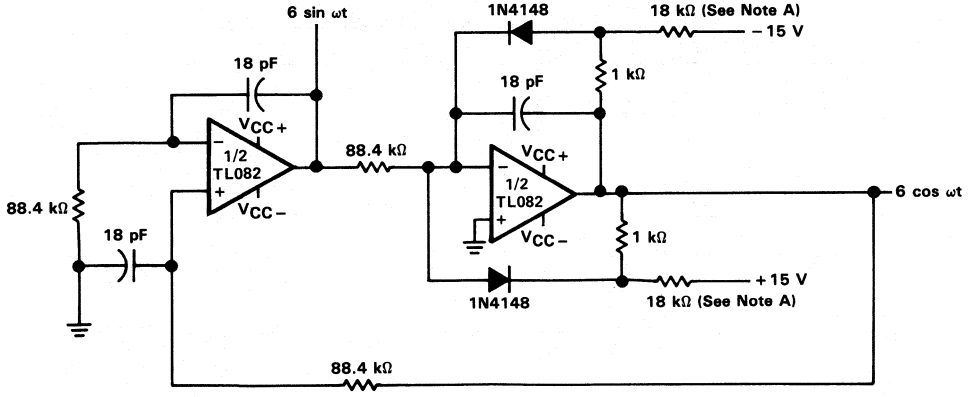


FIGURE 25. HIGH-Q NOTCH FILTER



† or TL085

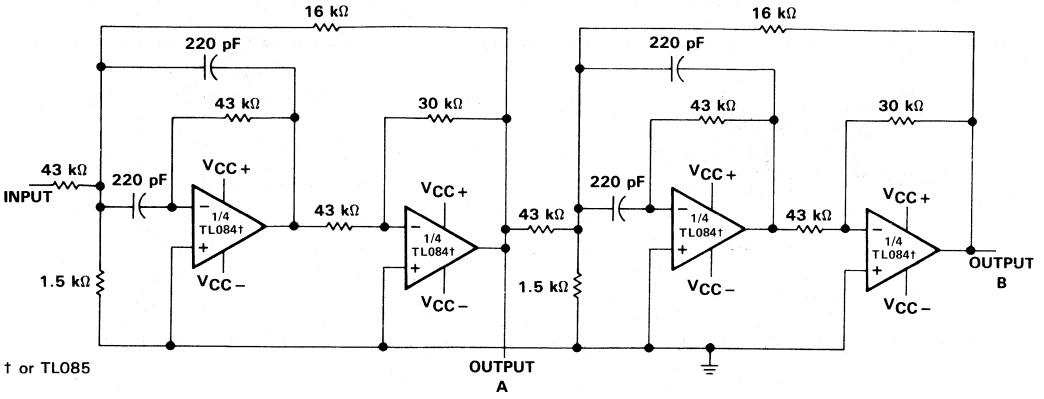
FIGURE 26. AUDIO DISTRIBUTION AMPLIFIER

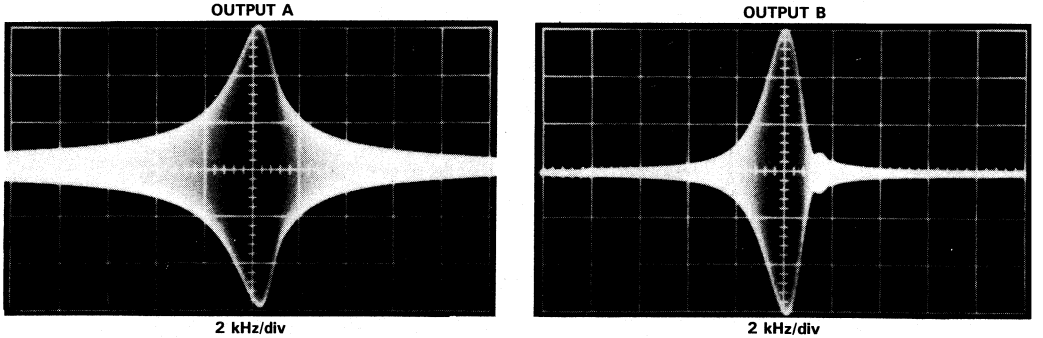


NOTE A: These resistor values may be adjusted for a symmetrical output.

FIGURE 27. 100-kHZ QUADRATURE OSCILLATOR

TYPICAL APPLICATION DATA





SECOND-ORDER BANDPASS FILTER
f_o = 100 kHz, Q = 30, GAIN = 4

CASCADED BANDPASS FILTER
f_o = 100 kHz, Q = 69, GAIN = 16

FIGURE 28. POSITIVE-FEEDBACK BANDPASS FILTER

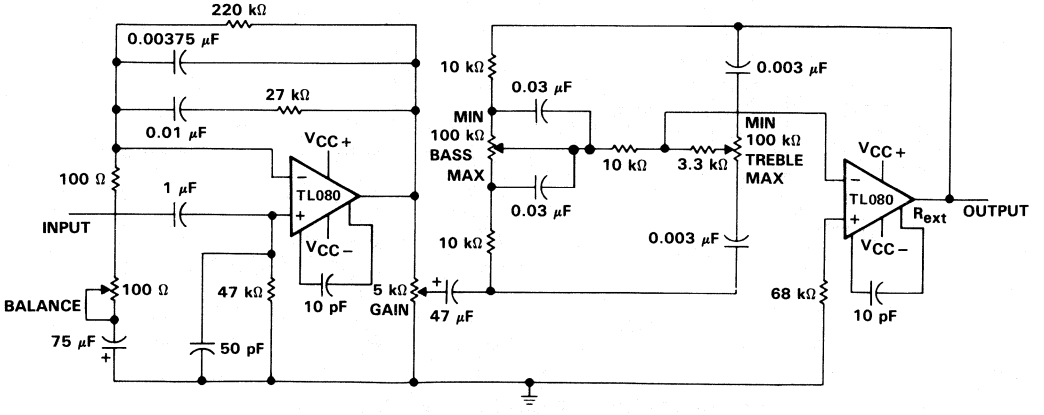


FIGURE 29. IC PREAMPLIFIER

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D2484, MARCH 1979—REVISED MARCH 1989

- **Low Input Offset Voltage . . . 0.5 mV Max**
- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **High Input Impedance . . . JFET-Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate . . . 18 V/μs Typ**
- **Low Total Harmonic Distortion . . . 0.003% Typ**

description

These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset currents, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

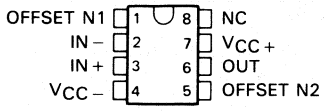
The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

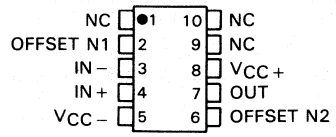
T_A	TYPE	V_{IO} MAX AT 25°C	PACKAGE				
			SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)	FLAT (U)
0°C to 70°C	Single	0.5 mV	TL087CD	TL087CJG	TL087CL	TL087CP	
		1 mV	TL088CD	TL088CJG	TL088CL	TL088CP	
	Dual	0.5 mV	TL287CD	TL287CJG	TL287CL	TL287CP	
		1 mV	TL288CD	TL288CJG	TL288CL	TL288CP	
−40°C to 85°C	Single	0.5 mV	TL087ID	TL087IJG	TL087IL	TL087IP	
		1 mV	TL088ID	TL088IJG	TL088IL	TL088IP	
	Dual	0.5 mV	TL287ID	TL287IJG	TL287IL	TL287IP	
		1 mV	TL288ID	TL288IJG	TL288IL	TL288IP	
−55°C to 125°C	Single	1 mV		TL088MJG	TL088ML		TL088MU
	Dual	1 mV		TL288MJG	TL288ML		TL288MU

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL087CDR).

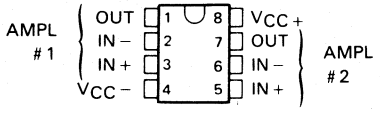
TL087, TL088
D, JG, OR P PACKAGE
(TOP VIEW)



TL088M
U PACKAGE
(TOP VIEW)

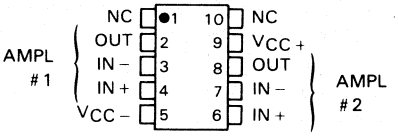


TL287, TL288
D, JG, OR P PACKAGE
(TOP VIEW)

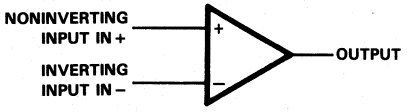


NC—No internal connection

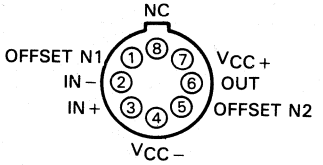
TL288M
U PACKAGE
(TOP VIEW)



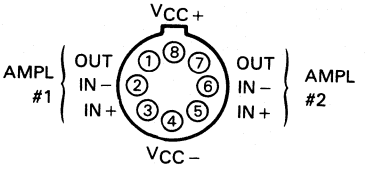
symbol (each amplifier)



TL087, TL088
L PACKAGE
(TOP VIEW)



TL287, TL288
L PACKAGE
(TOP VIEW)



Pin 4 (L Package) is in electrical contact with the case
NC—No internal connection

TEXAS INSTRUMENTS
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bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		−18	−18	−18	V
Differential input voltage (see Note 2)		±30	±30	±30	V
Input voltage (see Notes 1 and 3)		±15	±15	±15	V
Input current, I_I (each input)		±1	±1	±1	mA
Output current, I_O (each output)		±80	±80	±80	mA
Total V_{CC+} terminal current		160	160	160	mA
Total V_{CC-} terminal current		−160	−160	−160	mA
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG, L, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
U	675 mW	5.4 mW/°C	432 mW	351 mW	135 mW

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		±5		±15	±5		±15	±5		±15	V
Common-mode input voltage, V_{IC}	$V_{CC\pm}$ = ±5 V	−1		4	−1		4	−1		4	V
	$V_{CC\pm}$ = ±15 V	−11		11	−11		11	−11		11	V
Input voltage, V_I	$V_{CC\pm}$ = ±5 V	−1		4	−1		4	−1		4	V
	$V_{CC\pm}$ = ±15 V	−11		11	−11		11	−11		11	V
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics, $V_{CC\pm}$ = ±15 V

PARAMETER		TEST CONDITIONS†		TL088M TL288M			TL087I TL088I TL287I TL288I			TL087C TL088C TL287C TL288C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	R_S = 50 Ω, V_O = 0, T_A = 25°C	TL087, TL287					0.1	0.5		0.1	0.5	mV
			TL088, TL288		0.1	3		0.1	1		0.1	1	
		R_S = 50 Ω, V_O = 0, T_A = full range	TL087, TL287						2			1.5	
			TL088, TL288			6			3			2.5	
αV_{IO}	Temperature coefficient of input offset voltage	R_S = 50 Ω, T_A = 25°C to MAX			10			8			8		μV/°C
I_{IO}	Input offset current	T_A = 25°C			5			5	100		5	100	pA
		T_A = full range				25			3			2	nA
I_{IB}	Input bias current‡	T_A = 25°C			30			30	200		30	200	pA
		T_A = full range				100			20			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		V_{CC-} +4 to V_{CC+} −4			V_{CC-} +4 to V_{CC+} −4			V_{CC-} +4 to V_{CC+} −4			V
V_{OPP}	Maximum-peak-to-peak output voltage swing	T_A = 25°C,	R_L = 10 kΩ	24	27		24	27		24	27		V
		T_A = full range	R_L ≥ 10 kΩ	24			24			24			
			R_L ≥ 2 kΩ	20			20			20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, T_A = 25°C	V_O = ±10 V,	50	105		50	105		50	105		V/mV
		R_L ≥ 2 kΩ, T_A = full range	V_O = ±10 V,	25			25			25			
B_1	Unity-gain bandwidth	T_A = 25°C			3			3			3		MHz
r_i	Input resistance	T_A = 25°C			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	R_S = 50 Ω, V_{IC} = V_{ICR} min,	V_O = 0 V, T_A = 25°C	80	93		80	93		80	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	R_S = 50 Ω, $V_{CC\pm}$ = ±9 V to ±15 V, T_A = 25°C	V_O = 0 V,	80	99		80	99		80	99		dB
I_{CC}	Supply current (per amplifier)	No load, T_A = 25°C	V_O = 0,		2.6	2.8		2.6	2.8		2.6	2.8	mA

†All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for T_A is −55°C to 125°C for TL__88M; −40°C to 85°C for TL__8__I; and 0°C to 70°C for TL__8__C.

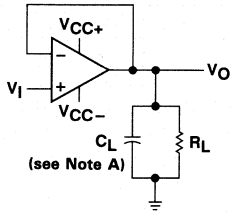
‡Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

operating characteristics V_{CC} = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TL088M, TL288M			TL087I, TL087C TL088I, TL088C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1		18		8	18		V/μs
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1		55			55		ns
	Overshoot factor			25%			25%		
V_n	Equivalent input noise voltage	R_S = 100 Ω, f = 1 kHz		19			19		nV/√Hz

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

FIGURE 1. SLEW RATE, RISE/FALL TIME, AND OVERSHOOT TEST CIRCUIT

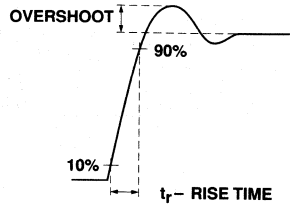


FIGURE 2. RISE TIME AND OVERSHOOT WAVEFORM

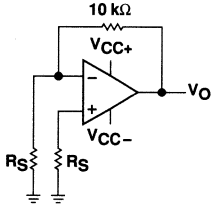
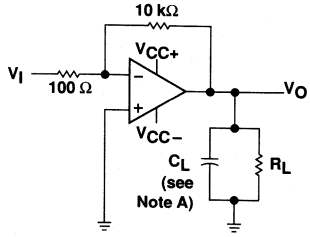


FIGURE 3. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 4. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

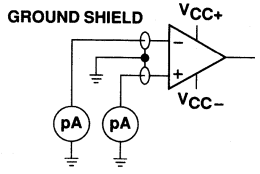


FIGURE 5. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

input bias and offset current

At the picoamp bias current level typical of these JFET operational amplifiers, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied, but with no device in the socket. The device is then inserted in the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
αV_{IO}	Temperature coefficient of input offset voltage	Distribution	6, 7
I_{IO}	Input offset current	vs Temperature	8
I_{IB}	Input bias current	vs V_{IC}	9
		vs Temperature	8
V_I	Common-mode input voltage range limits	vs V_{CC}	10
		vs Temperature	11
V_{ID}	Differential input voltage	vs Output voltage	12
V_{OM}	Maximum peak output voltage swing	vs V_{CC}	13
		vs Output current	17
		vs Frequency	14, 15, 16
		vs Temperature	18
A_{VD}	Differential voltage amplification	vs R_L	19
		vs Frequency	20
		vs Temperature	21
z_o	Output impedance	vs Frequency	24
CMRR	Common-mode rejection ratio	vs Frequency	22
		vs Temperature	23
k_{SVR}	Supply-voltage rejection ratio	vs Temperature	25
I_{OS}	Short-circuit output current	vs V_{CC}	26
		vs Time	27
		vs Temperature	28
I_{CC}	Supply current	vs V_{CC}	29
		vs Temperature	30
SR	Slew Rate	vs R_L	31
		vs Temperature	32
	Overshoot factor	vs C_L	33
V_n	Equivalent input noise voltage	vs Frequency	34
THD	Total harmonic distortion	vs Frequency	35
B_1	Unity-gain bandwidth	vs V_{CC}	36
		vs Temperature	37
ϕ_m	Phase margin	vs V_{CC}	38
		vs C_L	39
		vs Temperature	40
	Phase shift	vs Frequency	20
	Pulse response	Small-signal	41
		Large-signal	42

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TL088
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

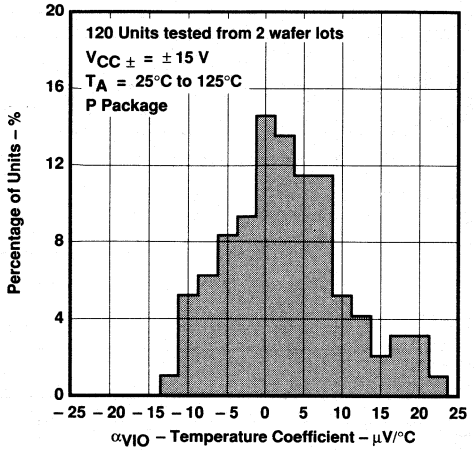


FIGURE 6

DISTRIBUTION OF TL288
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

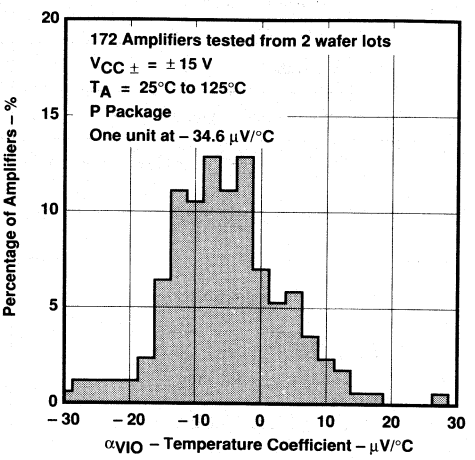


FIGURE 7

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

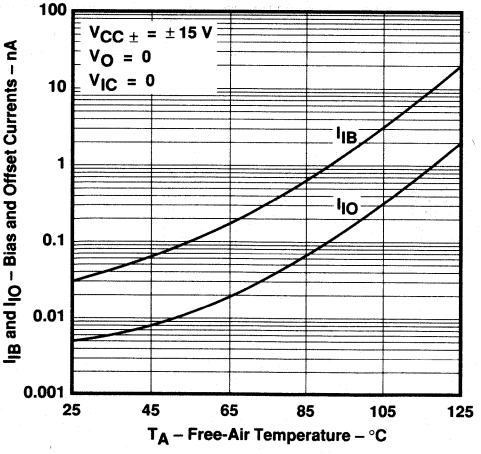


FIGURE 8

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

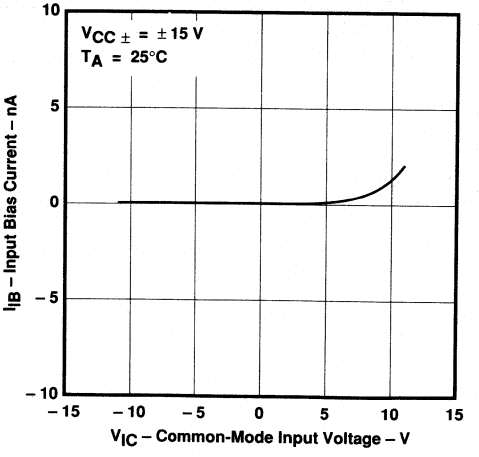


FIGURE 9

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
SUPPLY VOLTAGE

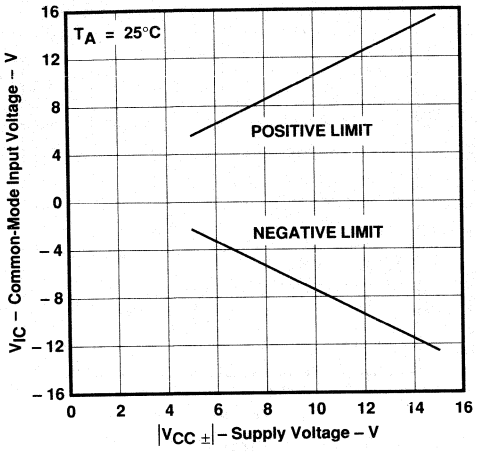


FIGURE 10

COMMON-MODE
INPUT VOLTAGE RANGE LIMITS
vs
FREE-AIR TEMPERATURE

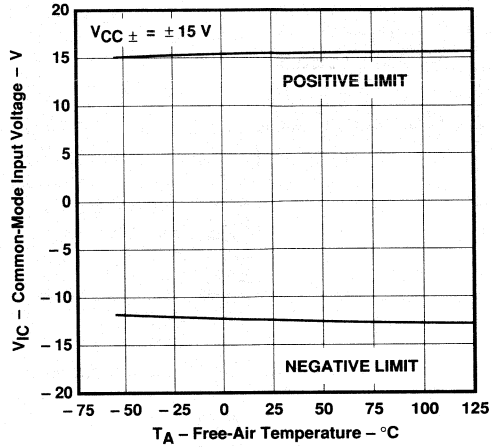


FIGURE 11

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

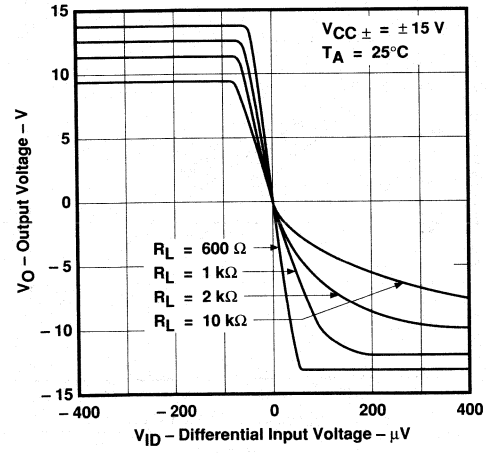


FIGURE 12

MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

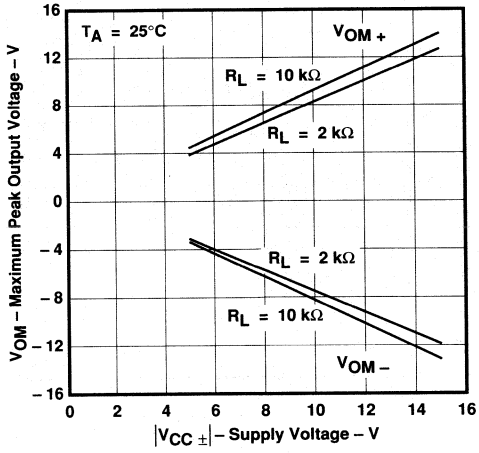


FIGURE 13

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

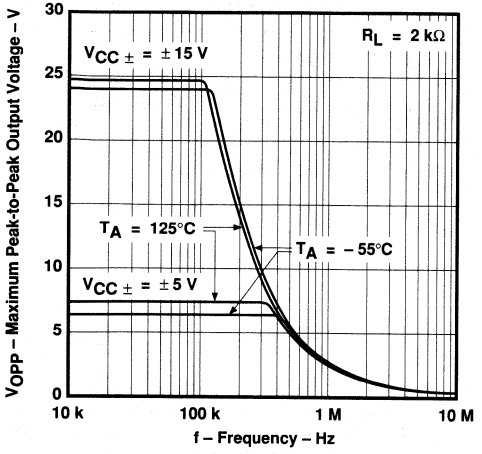


FIGURE 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

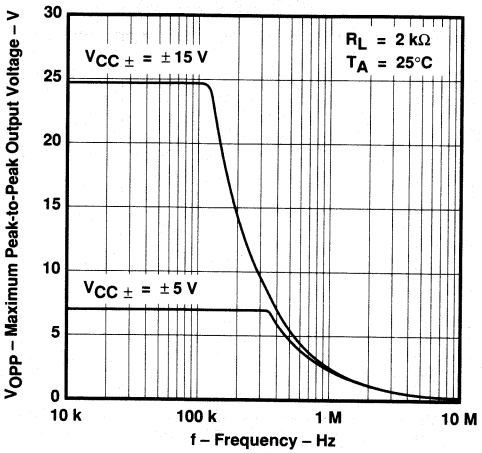


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

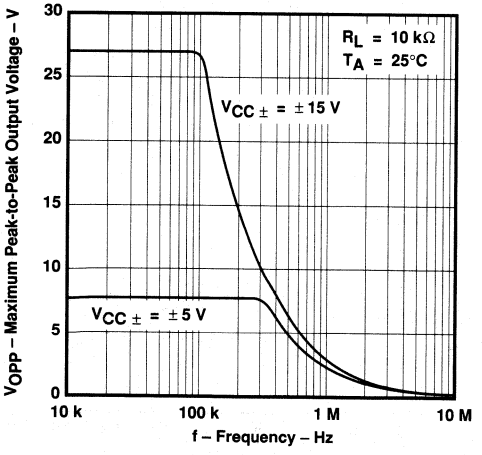


FIGURE 16

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

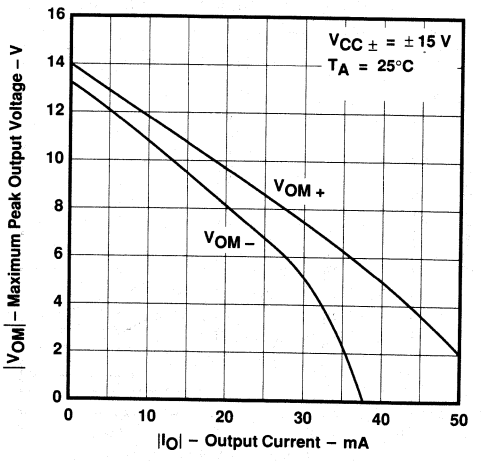


FIGURE 17

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

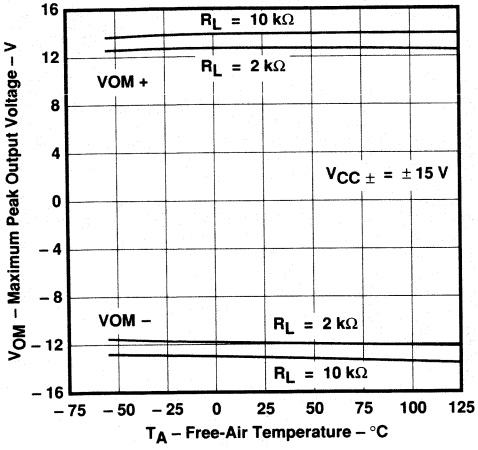


FIGURE 18

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

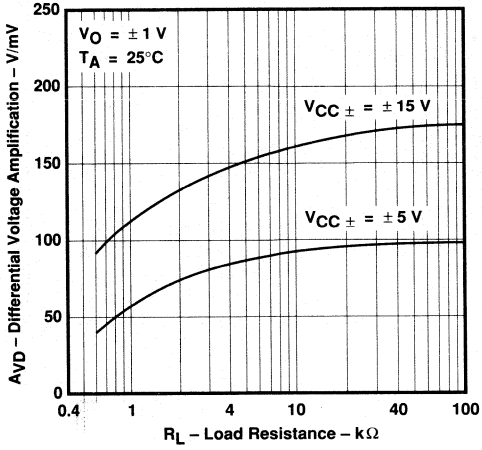


FIGURE 19

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

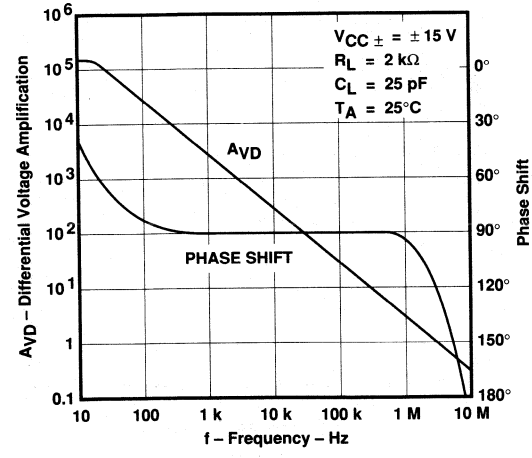


FIGURE 20

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

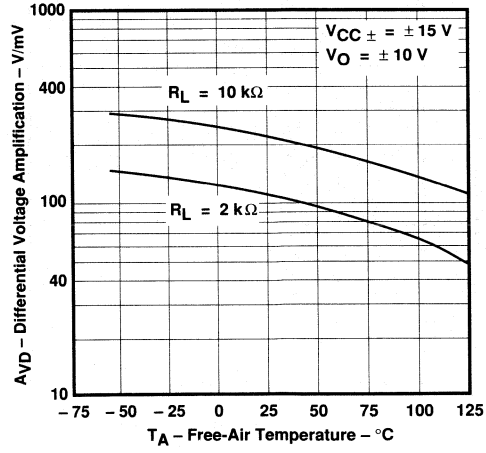


FIGURE 21

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

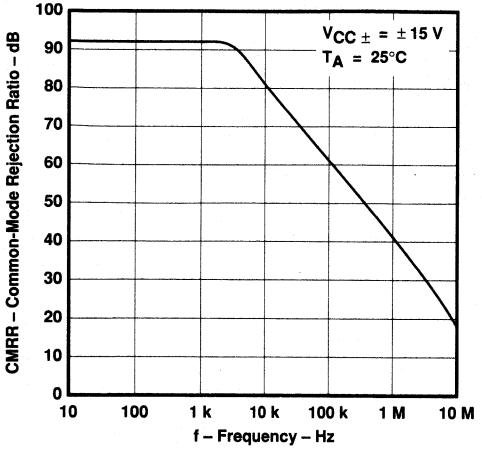


FIGURE 22

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

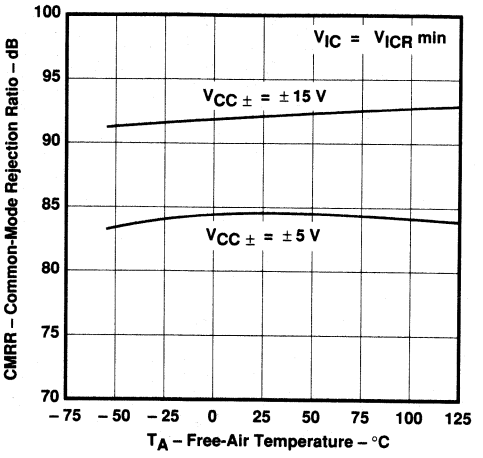


FIGURE 23

OUTPUT IMPEDANCE
vs
FREQUENCY

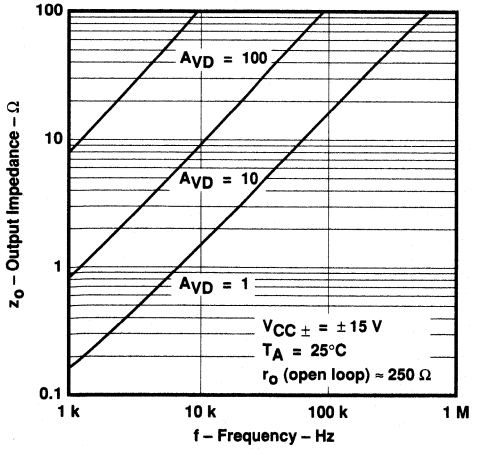


FIGURE 24

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

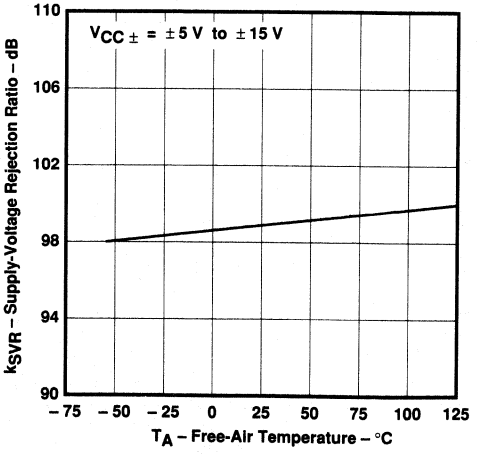


FIGURE 25

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

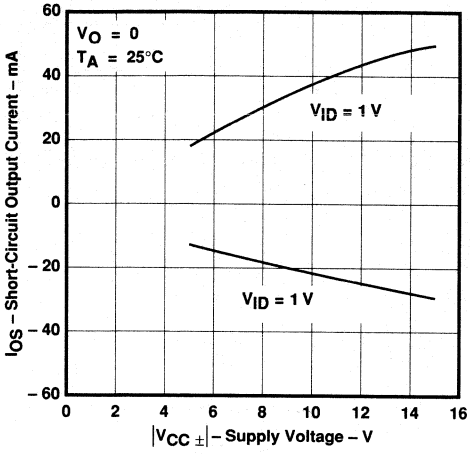


FIGURE 26

SHORT-CIRCUIT OUTPUT CURRENT
vs
TIME

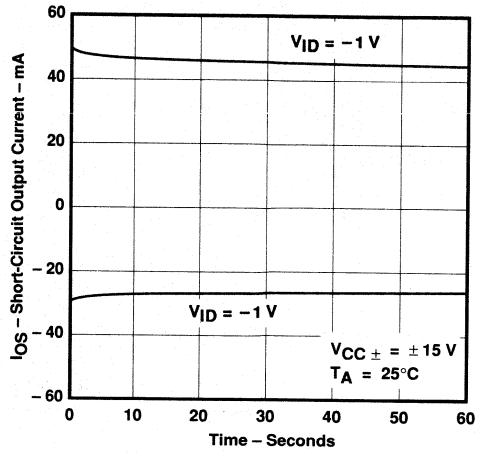


FIGURE 27

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

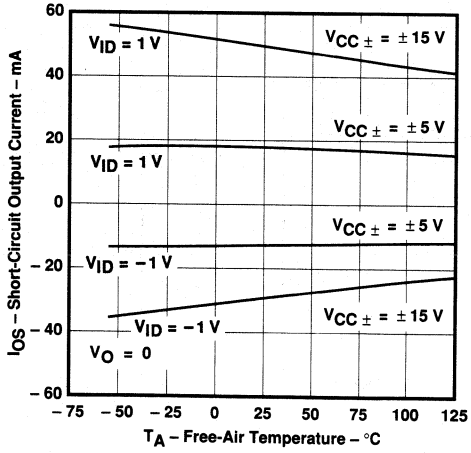


FIGURE 28

Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

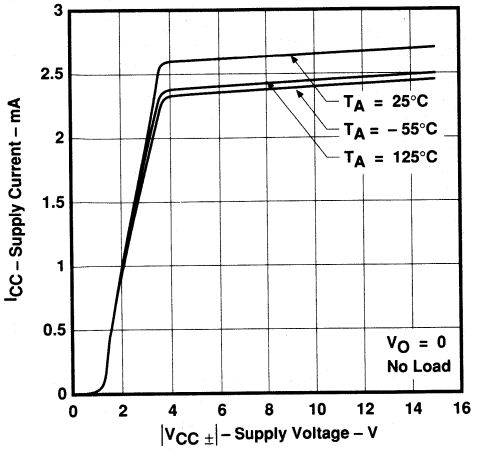


FIGURE 29

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

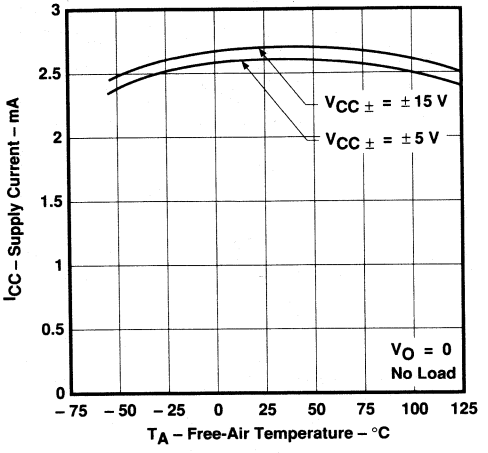


FIGURE 30

SLEW RATE
vs
LOAD RESISTANCE

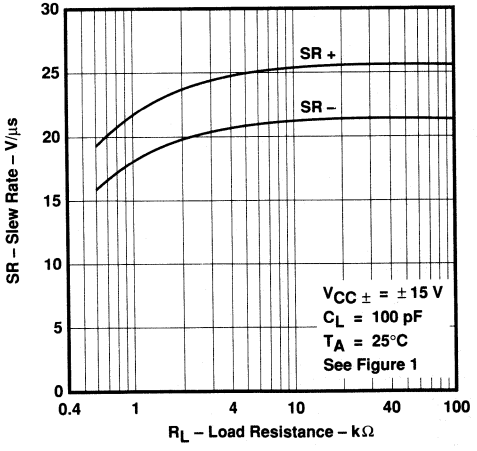


FIGURE 31

SLEW RATE
vs
FREE-AIR TEMPERATURE

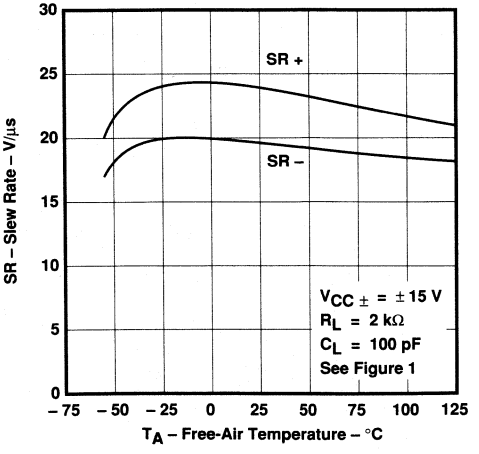


FIGURE 32

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

OVERSHOOT FACTOR
vs
LOAD CAPACITANCE

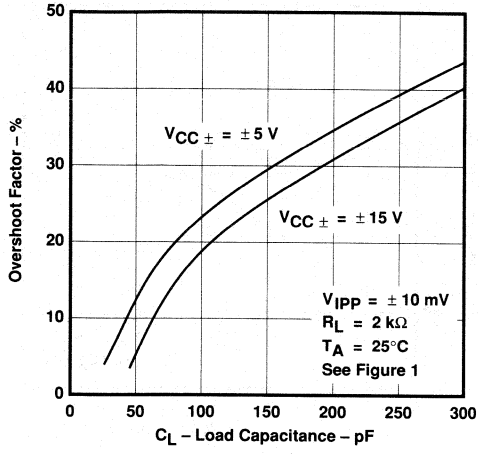


FIGURE 33

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

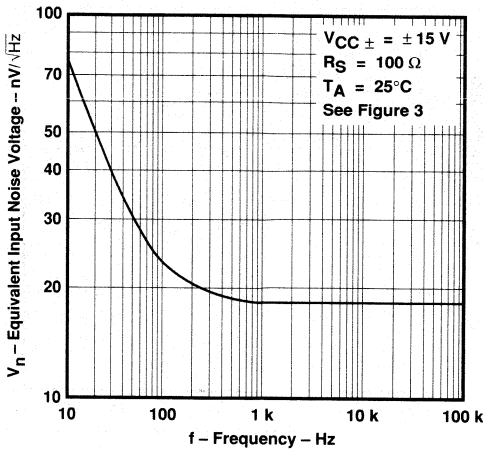


FIGURE 34

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

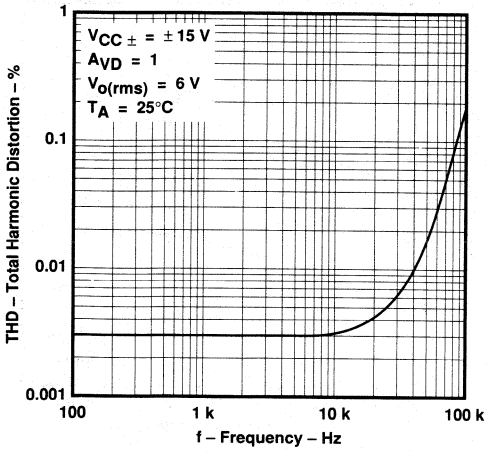


FIGURE 35

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

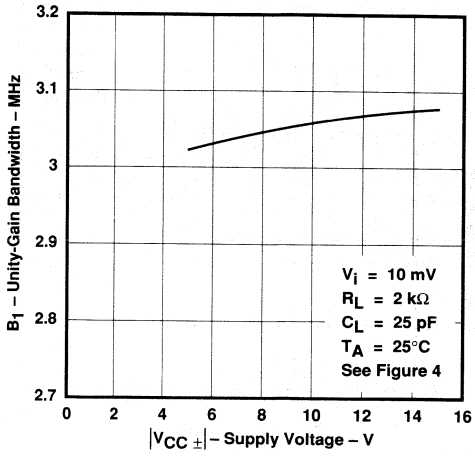


FIGURE 36

Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

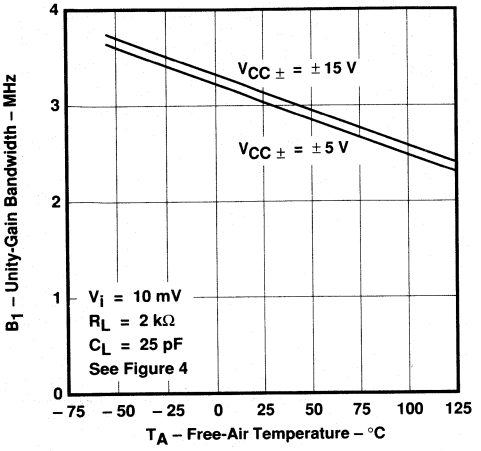


FIGURE 37

PHASE MARGIN
vs
SUPPLY VOLTAGE

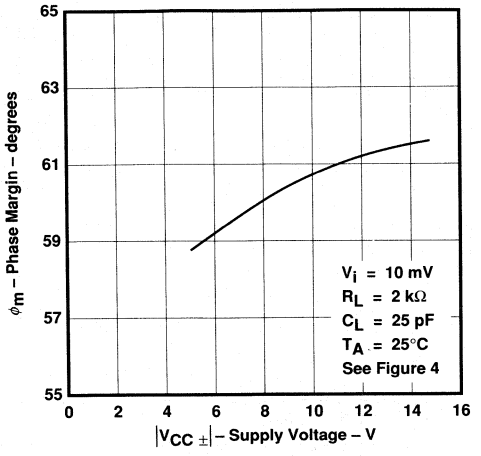


FIGURE 38

PHASE MARGIN
vs
LOAD CAPACITANCE

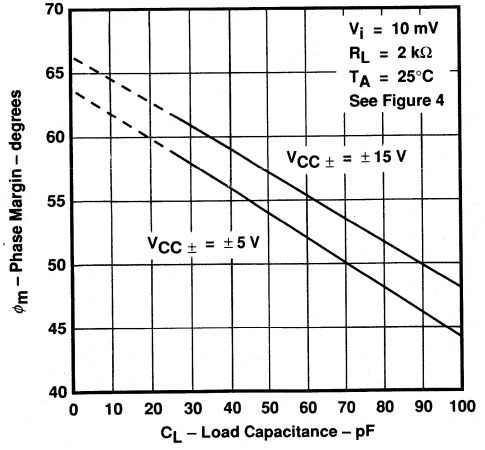


FIGURE 39

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

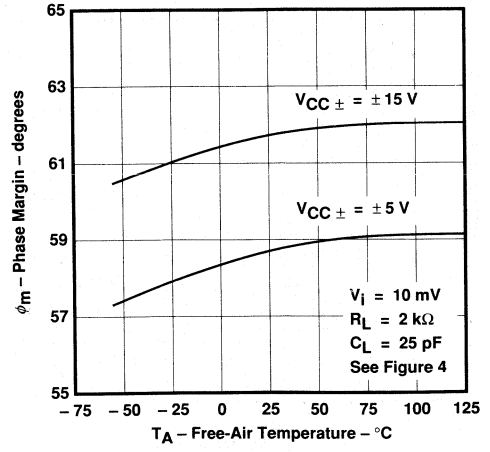


FIGURE 40

†Data at high and low temperatures are applicable within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

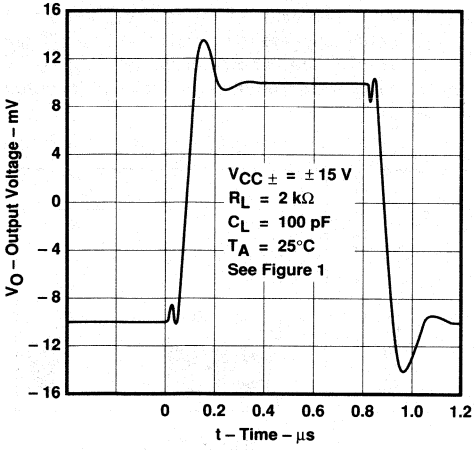


FIGURE 41

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

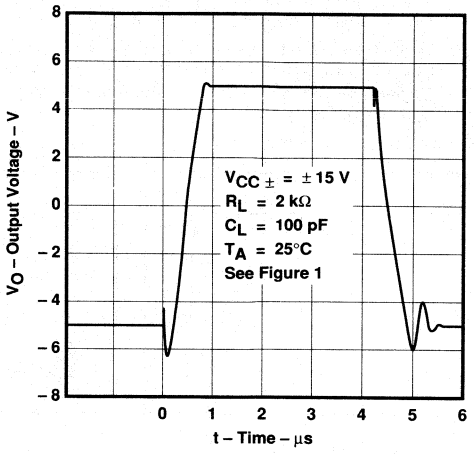
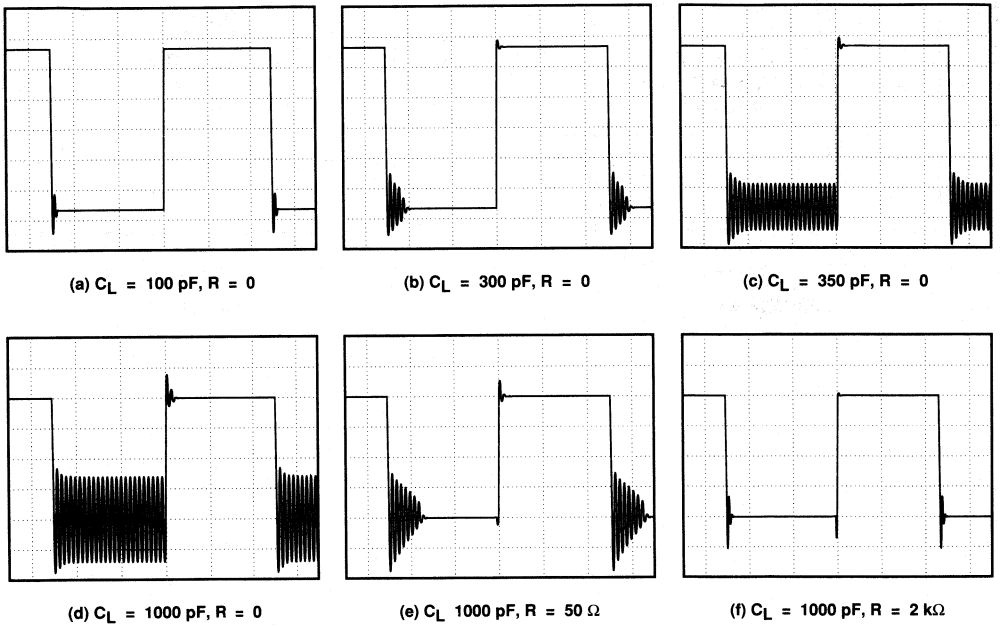


FIGURE 42

TYPICAL APPLICATION DATA

output characteristics

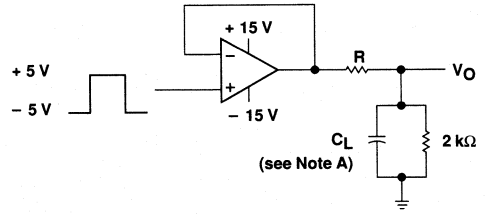
All operating characteristics are specified with 100-pF load capacitance. These amplifiers will drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem. Capacitive loads of 1000 pF and larger may be driven if enough resistance is added in series with the output (see Figure 43).



(a) C_L = 100 pF, R = 0 (b) C_L = 300 pF, R = 0 (c) C_L = 350 pF, R = 0

(d) C_L = 1000 pF, R = 0 (e) C_L 1000 pF, R = 50 Ω (f) C_L = 1000 pF, R = 2 kΩ

FIGURE 43. EFFECT OF CAPACITIVE LOADS



NOTE A: C_L includes fixture capacitance.

FIGURE 44. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS

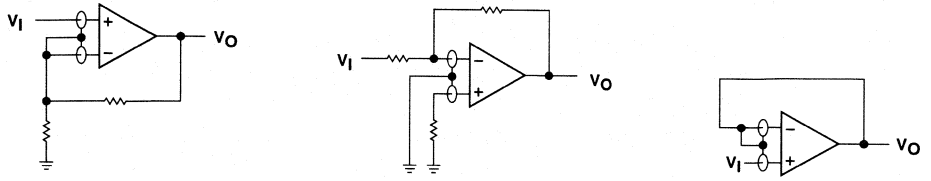
TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

input characteristics

These amplifiers are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Because of the extremely high input impedance and resulting low bias current requirements, these amplifiers are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause degradation in system performance. It is good practice to include guard rings around inputs (see Figure 45). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 45. USE OF GUARD RINGS

noise performance

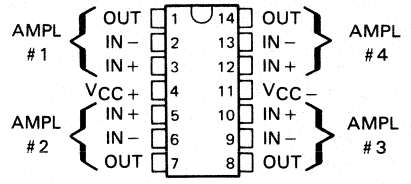
The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of these amplifiers result in a very low current noise. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ.

2 Operational Amplifiers

D2604, NOVEMBER 1981 – MAY 1988

- Continuous-Short Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Unity-Gain Bandwidth 3 MHz Typical
- Gain and Phase Match Between Amplifiers

N PACKAGE
(TOP VIEW)



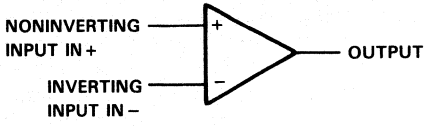
Description

The TL136C is a quad high-performance operational amplifier with each amplifier electrically similar to the uA741 except that offset null capability is not provided.

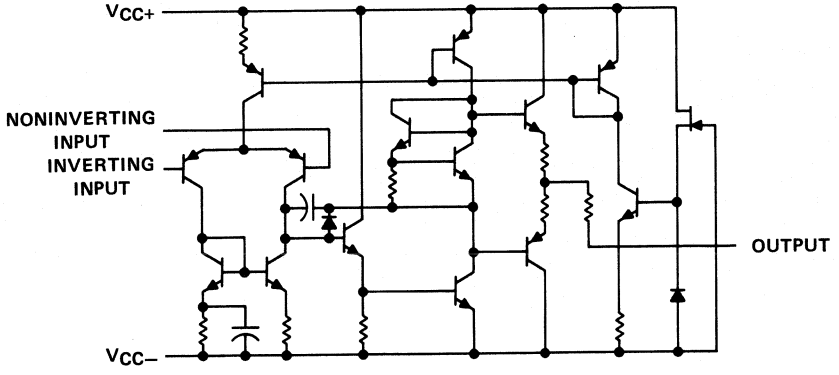
The high common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

The TL136C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) 18
Supply voltage V_{CC-} (see Note 1) . . . . . −18
Differential input voltage (see Note 2) . . . . . ±30
Input voltage (any input, see Notes 1 and 3) . . . . . ±15
Duration of output short-circuit to ground, one amplifier at a time (see Note 4) . . . . . unlimite
Continuous total dissipation . . . . . See Dissipation Rating Tabl
Operating free-air temperature range . . . . . 0°C to 70°
Storage temperature range . . . . . −65°C to 150°
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
N	800 mW	9.2 mW/°C	736 mW

lectrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0,	R_S = 50 Ω	25°C		0.5	6	mV
				0°C to 70°C			7.5	
I_{IO}	Input offset current	V_O = 0		25°C		5	200	nA
				0°C to 70°C			300	
I_{IB}	Input bias current	V_O = 0		25°C		40	500	nA
				0°C to 70°C			800	
V_{ICR}	Common-mode input voltage range			25°C	±12	±14		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L = 10 kΩ		25°C	24	28		V
		R_L = 2 kΩ		25°C	20	26		
		R_L ≥ 2 kΩ		0°C to 70°C	20			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ,	V_O = ±10 V	25°C	20	300		V/mV
				0°C to 70°C	15			
B_1	Unity-gain bandwidth			25°C		3		MHz
r_i	Input resistance			25°C	0.3	5		MΩ
CMRR	Common-mode rejection ratio	V_C = V_{ICR} min, R_S = 50 Ω		25°C	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm}$ = ±9 V to ± 15 V, R_S = 50 Ω		25°C		30	150	μV/V
V_n	Equivalent input noise voltage (closed-loop)	A_{VD} = 100, f = 1 kHz,	R_S = 100 Ω, BW = 1 Hz	25°C		7.5		nV/√Hz
I_{CC}	Supply current (All four amplifiers)	No load,	V_O = 0 V	25°C		5	11.3	mA
				0°C		6	13.7	
				70°C		4.5	11.3	
P_D	Total power dissipation (All four amplifiers)	No load,	V_O = 0 V	25°C		150	340	mW
				0°C		180	400	
				70°C		135	300	
$V_{o1}V_{o2}$	Crosstalk attenuation	Open loop A_{VD}	R_S = 1 kΩ, f = 10 kHz	25°C		105		dB
				25°C		105		

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, C_L = 100 pF	R_L = 2 kΩ,		0.13		μs
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF	R_L = 2 kΩ,		2.0		V/μs

D2343, APRIL 1977—REVISED OCTOBER 1988

- **Wide Range of Supply Voltages Single Supply . . 3 V to 30 V or Dual Supplies**
- **Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ**
- **Common-Mode Input Voltage Range Includes Ground Allowing Direct Sensing near Ground**
- **Low Input Bias and Offset Parameters Input Offset Voltage . . . 2 mV Typ Input Offset Current . . . 3 nA Typ (TL321I) Input Bias Current . . . 45 nA Typ**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±32 V**
- **Open-Loop Differential Voltage Amplification . . . 100 V/mV Typ**
- **Internal Frequency Compensation**

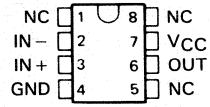
description

The TL321 is a high-gain, frequency-compensated operational amplifier that was designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies is also possible as long as the difference between the two supplies is 3 V to 30 V and pin 7 is at least 1.5 V more positive than the input common-mode voltage. The low supply current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, d-c amplification blocks, and all the conventional operational amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the TL321 can be operated directly off of the standard 5-V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15-V supplies.

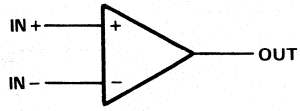
The TL321I is characterized for operation from −25°C to 85°C. The TL321C is characterized for operation from 0°C to 70°C.

TL321I, TL321C . . . D, JG OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

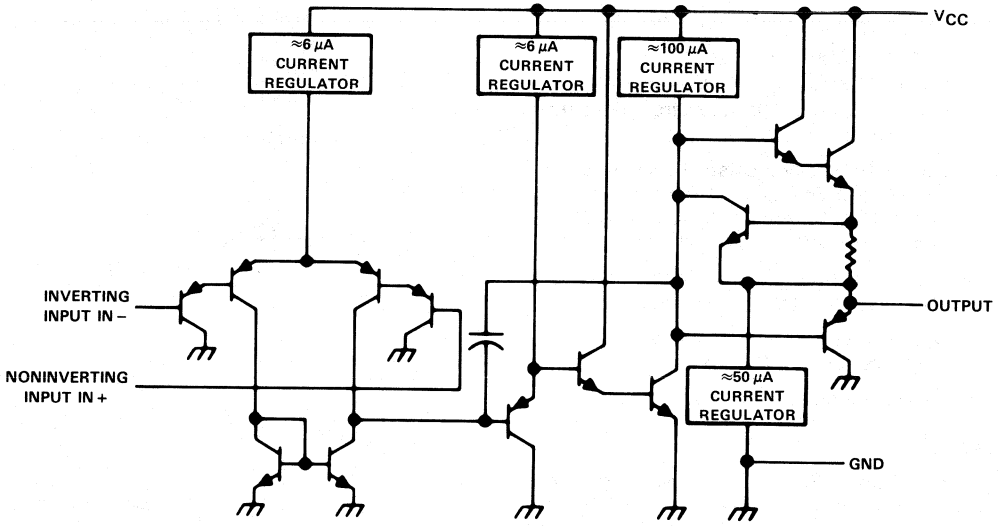


AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	7 mV	TL321CD	TL321CJG	TL321CP
−25°C to 85°C	5 mV	TL321ID	TL321IJG	TL321IP

The D packages are available taped and reeled. Add the suffix R to the device type. (e.g., TL321CDR)

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 32 V
Differential input voltage (see Note 2) . . . . . ±32 V
Input voltage range (either input) . . . . . −0.3 V to 32 V
Duration of output short-circuit to ground at (or below) 25°C free-air temperature
(V_{CC} ≤ 15 V) (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL321I . . . . . −25°C to 85°C
TL321C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW
JG	680 mW	6.6 mW/°C	47°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW

lectrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TL321I			TL321C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		$V_{IC} = V_{ICR}$ min, V_{CC} = 5 V to 30 V, V_O = 1.4 V, R_S = 50 kΩ	25°C		2	5		2	7	mV
				Full range			7			9	
I_{IO}	Input offset current		V_O = 1.4 V	25°C		3	30		5	50	nA
				Full range			100			150	
I_{IB}	Input bias current		V_O = 1.4 V	25°C		−45	−150		−45	−250	nA
				Full range			−300			−500	
V_{ICR}	Common-mode input voltage range		V_{CC} = 5 V to 30 V	25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			
V_{OH}	High-level output voltage		V_{CC} = 30 V, R_L = 2 kΩ	Full range	26			26			V
			V_{CC} = 30 V, R_L ≥ 10 kΩ	Full range	27	28		27	28		
			R_L ≥ 2 kΩ	25°C	3.5			3.5			
V_{OL}	Low-level output voltage		R_L ≤ 10 kΩ	Full range		5	20		5	20	mV
A_{VD}	Large-signal differential voltage amplification		V_{CC} = 15 V, V_O = 1 V to 11 V, R_L ≥ 2 kΩ	25°C	50	100		25	100		V/mV
				Full range	25			15			
CMRR	Common-mode rejection ratio		$V_{IC} = V_{ICR}$ min, R_S = 50 Ω	25°C	70	85		65	85		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{CC} = 5 V to 30 V, R_S = 50 Ω	25°C	65	100		65	100		dB
I_O	Output current	Source	V_{CC} = 15 V, V_{ID} = 1 V, V_O = 0	25°C	−25	−40		−20	−40		mA
				Full range	−10	−20		−10	−20		
		Sink	V_{CC} = 15 V, V_{ID} = −1 V, V_O = 15 V	25°C	10	20		10	20		
				Full range	5	8		5	8		
			V_{ID} = −1 V, V_O = 200 mV	25°C	12	50		12	50		µA
I_{CC}	Supply current		No load, V_O = 15 V, V_{CC} = 30 V	Full range			2			2	mA
			No load, V_O = 2.5 V, V_{CC} = 5 V	Full range		0.4	1			1	

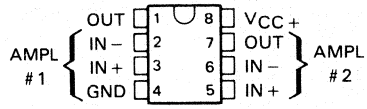
† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range is −25°C to 85°C for TL321I, and 0°C to 70°C for TL321C.

2 Operational Amplifiers

D2567, OCTOBER 1979—REVISED OCTOBER 1988

- **Wide Range of Supply Voltages Single Supply . . . 3 V to 36 V or Dual Supplies**
- **Class AB Output Stage**
- **True Differential Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**

D, JG, OR P PACKAGE
(TOP VIEW)

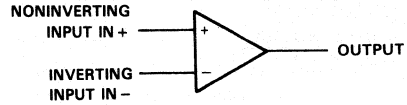


description

The TL322I and the TL322C are dual operational amplifiers similar in performance to the uA741 but with several distinct advantages. They are designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies is also possible provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to V_{CC-} 1.5 V. Quiescent supply currents per amplifier are typically less than one-half those of the uA741.

The TL322I is characterized for operation from −40°C to 85°C. The TL322C is characterized for operation from 0°C to 70°C.

symbol (each amplifier)

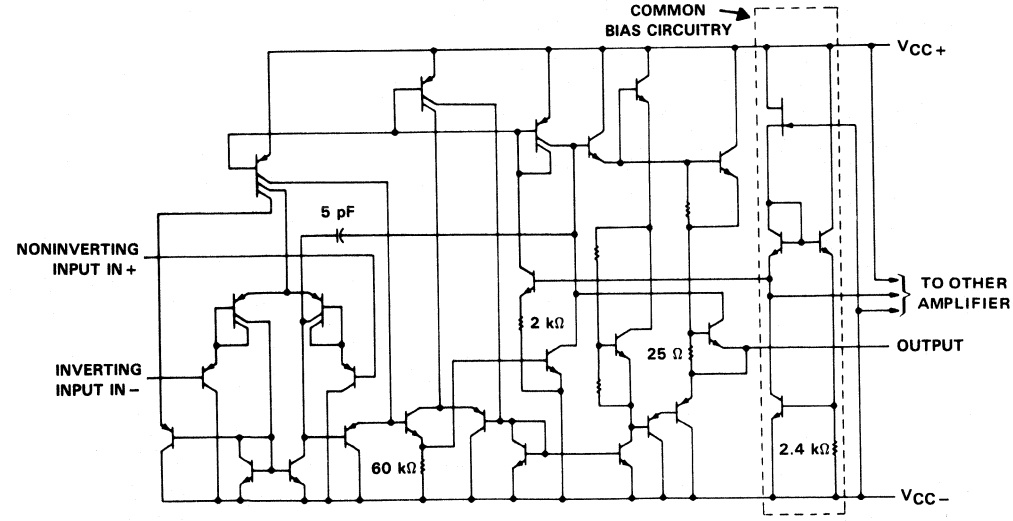


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	10 mV	TL322CD	TL322CJG	TL322CP
−40°C to 85°C	8 mV	TL322ID	TL322IJG	TL322IP

D packages are available taped and reeled. Add "R" suffix to device type, (e.g. TL322CDR)

schematic (each amplifier)



All component values shown are nominal

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL322I	TL322C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Supply voltage V_{CC+} with respect to V_{CC-}		36	36	V
Differential input voltage (see Note 2)		±36	±36	V
Input voltage (see Notes 1 and 3)		±18	±18	V
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package	260	260	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Neither input must ever be more positive then V_{CC+} or more negative than V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	680 mW	5.8 mW/°C	33°C	464 mW	377 mW
JG	680 mW	6.6 mW/°C	47°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	65°C	640 mW	520 mW

lectrical characteristics at specified free-air temperature; $V_{CC\pm}$ = 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL322I			TL322C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		2	8		2	10	mV
			Full range			10			12	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	25°C		10			10		μV/°C
I_{IO}	Input offset current	V_O = 0	25°C		30	75		30	50	nA
			Full range			250			200	
α_{IIO}	Temperature coefficient of input offset current	V_O = 0	25°C		50			50		pA/°C
I_{IB}	Input bias current	V_O = 0	25°C		−0.2	−0.5		−0.2	−0.5	μA
			Full range			−1			−0.8	
V_{ICR}	Common-mode input voltage range‡		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output voltage swing	R_L = 10 kΩ	25°C	±12	±12.5		±12	±13.5		V
		R_L = 2 kΩ	25°C	±10	±12		±10	±13		
			Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L = 2 kΩ	25°C	20	200		20	200		V/mV
			Full range	15			15			
B_{OM}	Maximum-output-swing bandwidth	V_{OPP} = 20 V, A_{VD} = 1, THD ≤ 5%, R_L = 2 kΩ	25°C		9			9		kHz
B_1	Unity-gain bandwidth	V_O = 50 mV, R_L = 10 kΩ	25°C		1			1		MHz
ϕ_m	Phase margin	R_L = 2 kΩ, C_L = 200 pF	25°C		60°			60°		
r_i	Input resistance	f = 20 Hz	25°C	0.3	1		0.3	1		MΩ
r_o	Output resistance	f = 20 Hz	25°C		75			75		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	70	90		70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±2.5 V to ±15 V, R_S = 50 Ω	25°C		30	150		30	150	μV/V
I_{OS}	Short-circuit output current§	V_O = 0	25°C	±10	±30	±45	±10	±30	±45	mA
I_{CC}	Total supply current	V_O = 0, No load	25°C		1.4	4		1.4	4	mA

†All characteristics are noted under open-loop conditions unless otherwise noted. Full range for T_A is −40°C to 85°C for TL322I, and 0°C to 70°C for TL322C.
‡The V_{ICR} limits are directly linked volt-for-volt to supply voltage; the positive limit is 2 V less than V_{CC+}.
§Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	TL322I			TL322C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 2.5 V, R_S = 50 Ω			8		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V			75		30	50	nA
I_{IB}	Input bias current				−0.5		−0.2	−0.5	pA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		3.3	3.5		V
		R_L = 10 kΩ, V_{CC+} = 5 V to 30 V	V_{CC+} −1.7			V_{CC+} −1.7			
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		20	200		V/mV
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	V_{CC} = ±2.5 V to ±15 V			150			150	μV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		1.2	4		1.2	4	mA
V_{o1}/V_{o2}	Crosstalk attenuation	A_{VD} = 100, f = 1 kHz to 20 kHz		120			120		dB

†All characteristics are specified under open-loop conditions.
‡Output will swing essentially to ground.

switching characteristics: V_{CC+} = ±15 V, A_{VD} = 1, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V, C_L = 100 pF, See Figure 1		0.6		V/μs
t_r	Rise time	ΔV_O = 50 mV, C_L = 100 pF, R_L = 10 kΩ, See Figure 1		0.35		μs
t_f	Fall time			0.35		μs
	Overshoot factor			20%		
	Crossover distortion	V_{IPP} = 30 mV, V_{OPP} = 2 V, f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION

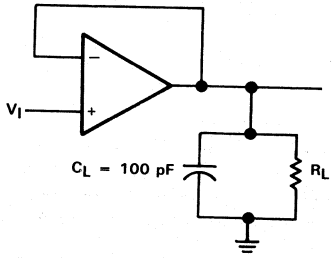


FIGURE 1. UNITY-GAIN AMPLIFIER

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

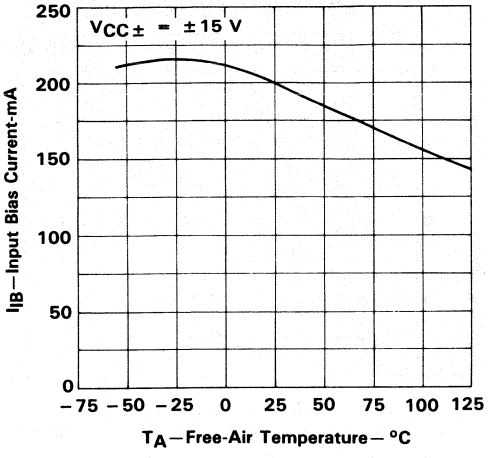


FIGURE 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

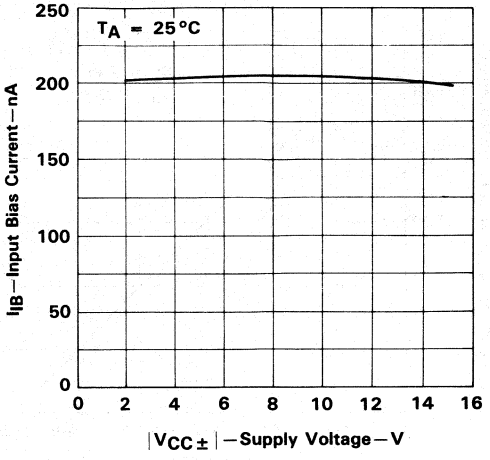


FIGURE 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

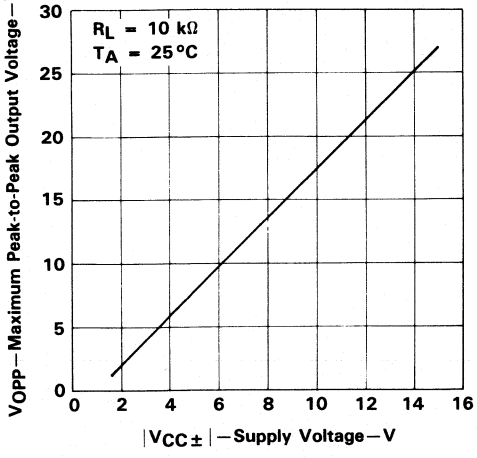


FIGURE 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

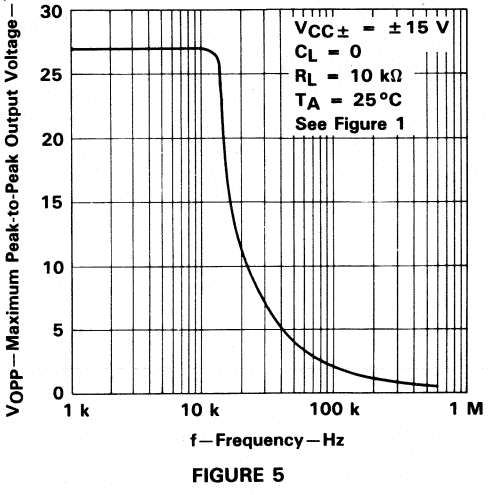


FIGURE 5

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY

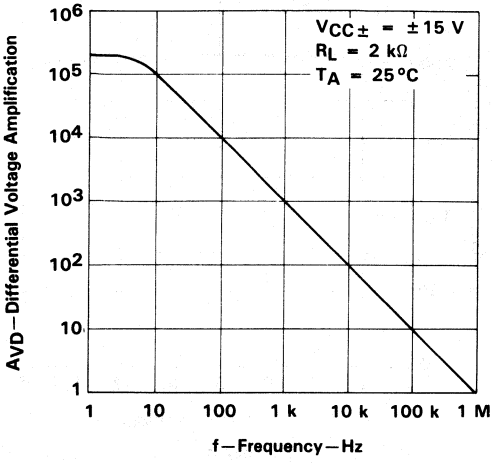


FIGURE 6

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

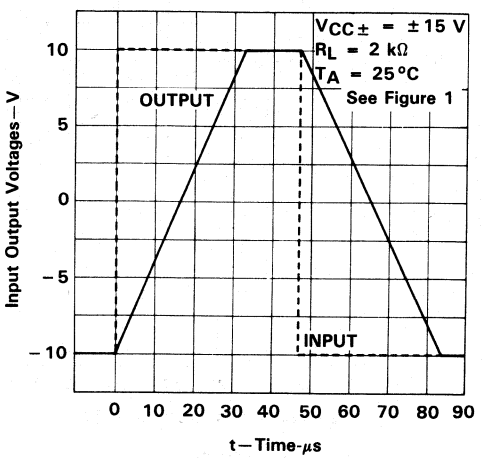


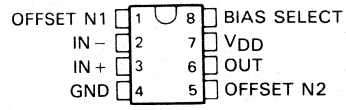
FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

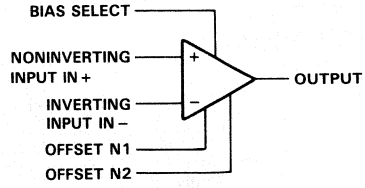
D2751, JULY 1983—REVISED SEPTEMBER 1988

- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **Low Noise . . . 30 nV √Hz Typ at 1 kHz (High Bias)**

D, JG, OR P PACKAGE
(TOP VIEW)



symbol



ɜscription

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS op amps, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS. This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features operation down to a 1.4-V supply and is stable at unity gain.

The TLC251C series is characterized for operation from 0°C to 70°C.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)
0°C to 70°C	10 mV	TLC251CD	TLC251CP	TLC251CJG
	5 mV	TLC251ACD	TLC251ACP	TLC251ACJG
	2 mV	TLC251BCD	TLC251BCP	TLC251BCJG

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC251CDR).

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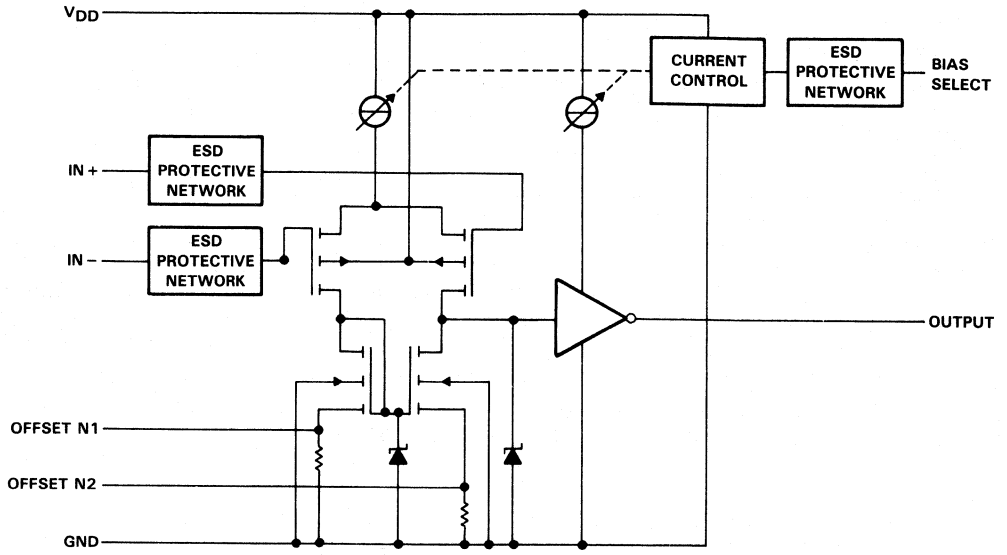
description (continued)

inaccessible equipment applications are possible using the low-voltage and low-power capabilities of th TLC251C series. In addition, by driving the bias-select input with a logic signal from a microprocesso these operational amplifiers can have software-controlled performance and power consumption. Th TLC251C series is well suited to solve the difficult problems associated with single battery and solar cel powered applications.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C
Bias Select pin voltage		See Application Information			

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 1.4 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	Low		0.7		μV/°C
					Medium		2		
					High		5		
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	−0.2 to 9			V
V_{OM}	Peak output voltage range‡		V_{ID} = 100 mV	25°C	Any	8	8.6		V
				0°C to 70°C		7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	Low	30	500		V/mV
					Medium	20	280		
					High	10	40		
				0°C to 70°C	Low	25			
					Medium	15			
					High	7.5			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	Any	65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	Low	70	88		dB
					Medium	70	88		
					High	65	82		
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C	Any		−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV				15		
$I_{IH(SEL)}$	High-level input current to bias select		$V_{I(SEL)}$ = 0 V	25°C	High		10.5		μA
$I_{IL(SEL)}$	Low-level input current to bias select		$V_{I(SEL)}$ = 10 V	25°C	Low		1.3		μA
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C	Low		10	23	μA
					Medium		150	300	
					High		1000	2000	
				0°C to 70°C	Low			33	
					Medium			400	
					High			2200	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V

PARAMETER			TEST CONDITIONS†		BIAS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC251C	V_O = 0.2 V, R_S = 50 Ω	25°C	Any			10	mV
				0°C to 70°C				12	
		TLC251AC		25°C	Any			5	
				0°C to 70°C				6.5	
		TLC251BC		25°C	Any			2	
				0°C to 70°C				3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C	Any		1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C	Any		1		pA
				0°C to 70°C				600	
V_{ICR}	Common-mode input voltage range			25°C	Any	0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	Any	450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C	Low		20		V/mV
					High		10		
CMRR	Common-mode rejection ratio		R_S = 50 Ω, V_O = 0.2 V, V_{IC} = V_{IC} min	25°C	Any	60	77		dB
I_{DD}	Supply current		V_O = 0.2 V, No load	25°C	Low		5	17	μA
					High		150	190	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias R_L = 1 MΩ, for medium bias R_L = 100 kΩ, and for high bias R_L = 10 kΩ.

‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1	Unity-gain bandwidth	C_L = 100 pF	Low		12		kHz
			High		75		
SR	Slew rate at unity gain	See Figure 1	Low		0.001		V/μs
			High		0.01		
	Overshoot factor	See Figure 1	Low		35%		
			High		30%		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	BIAS	MIN	TYP	MAX	UNIT
B_1 Unity-gain bandwidth	A_V = 40 dB, C_L = 100 pF, R_S = 50 Ω	Low		0.1		MHz
		Medium		0.7		
		High		2.3		
SR Slew rate at unity gain	See Figure 1	Low		0.04		V/μs
		Medium		0.6		
		High		4.5		
Overshoot factor	See Figure 1	Low		30%		
		Medium		35%		
		High		35%		
ϕ_m Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 100 pF	Low		43°		
		Medium		43°		
		High		50°		
V_n Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	Low		70		nV/√Hz
		Medium		38		
		High		30		

PARAMETER MEASUREMENT INFORMATION

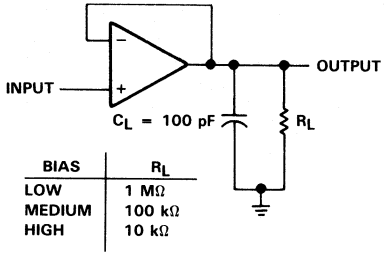


FIGURE 1. UNITY-GAIN AMPLIFIER

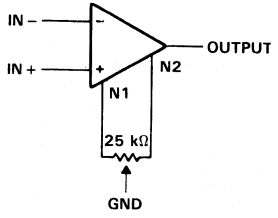


FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
BIAS SELECT PIN VOLTAGE

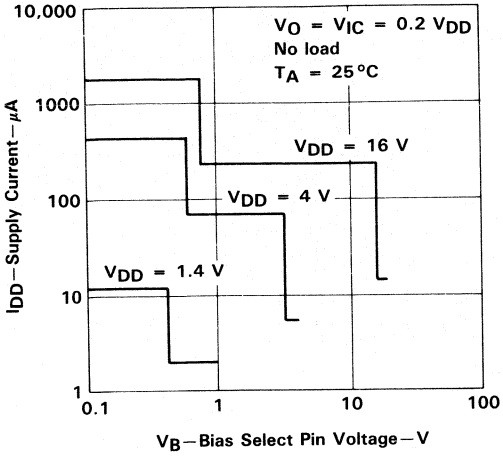


FIGURE 3

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

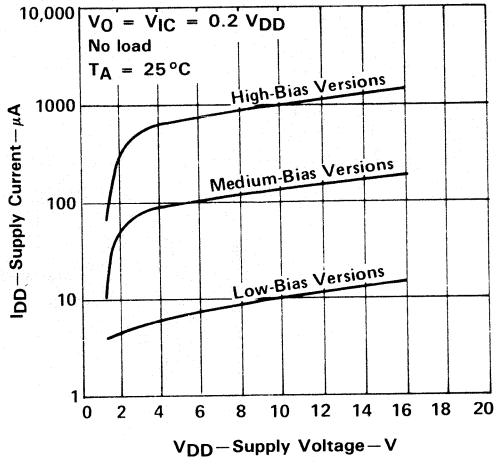


FIGURE 4

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

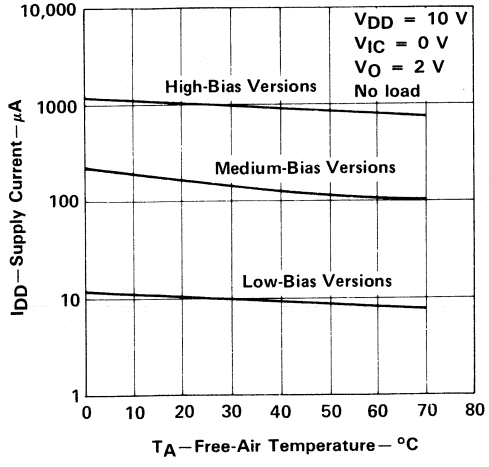


FIGURE 5

LOW BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

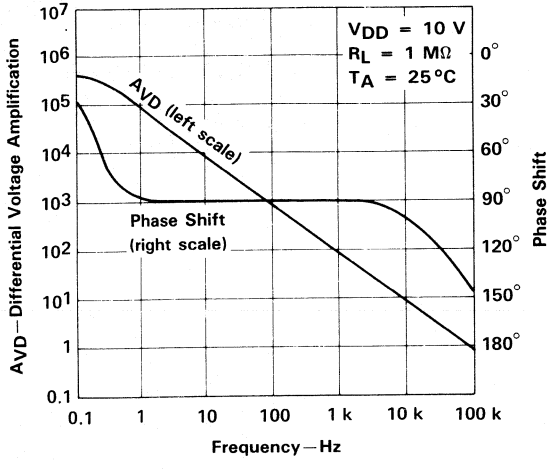


FIGURE 6

TYPICAL CHARACTERISTICS

MEDIUM BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

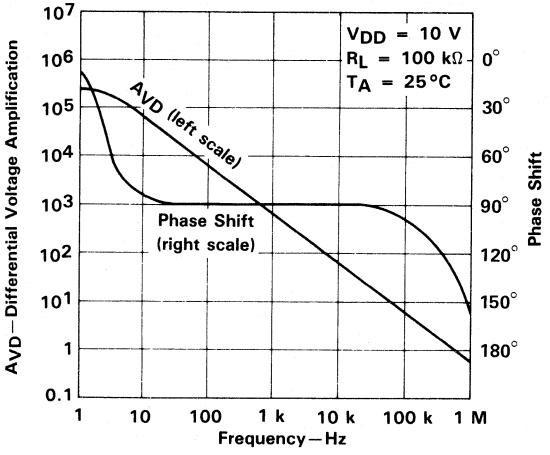


FIGURE 7

HIGH BIAS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

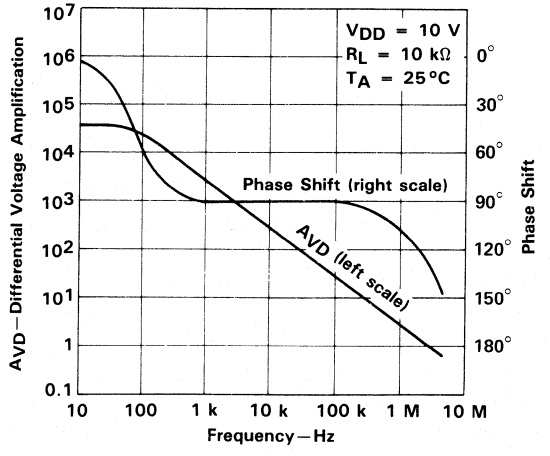


FIGURE 8

TYPICAL APPLICATION INFORMATION

atchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be applied simultaneously with, or before, application of any input signals.

using the bias select pin

The TLC251C series has a bias select pin that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 V to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium and low-bias modes at V_{DD} = 1.4 V are typically 2 μA, and in the high mode are typically 12 μA. The following table shows the recommended bias select pin connections at V_{DD} = 10 V:

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION†	TYPICAL I_{DD}‡
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

†The Bias Select pin may also be controlled by external circuitry to conserve power, etc. For information regarding the bias select pin, see Figure 3 in the typical characteristics curves.
‡For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected to the device GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At an I_{DD} setting of 1000 μA (high bias), the nulling range will allow the maximum offset specified to be trimmed to zero. In low or medium bias or when the amplifier is used below 4 V, total nulling may not be possible for all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

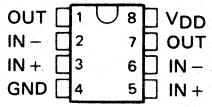
circuit layout precautions

The user is cautioned that when ever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

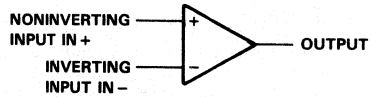
D2752, JUNE 1983—REVISED SEPTEMBER 1988

- A Suffix Versions Offer 5-mV V_{IO}
- B Suffix Versions Offer 2-mV V_{IO}
- Wide Range of Supply Voltages 1.4 V to 16 V
- True Single-Supply Operation
- Common-Mode Input Voltage Includes the Negative Rail
- Low Noise . . . 30 nV$\sqrt{\text{Hz}}$ Typ at f = 1 kHz (High-Bias Versions)

D, JG, OR P PACKAGE
(TOP VIEW)



symbol (each amplifier)



lescription

The TLC252C, TLC25L2C, and TLC25M2C are low-cost, low-power dual operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5 or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC252C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC252C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC252C series devices. Remote and inaccessible equipment

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)
0°C to 70°C	10 mV	TLC252CD	TLC252CP	TLC252CJG
	5 mV	TLC252ACD	TLC252ACP	TLC252ACJG
	2 mV	TLC252BCD	TLC252BCP	TLC252BCJG
	10 mV	TLC25L2CD	TLC25L2CP	TLC25L2CJG
	5 mV	TLC25L2ACD	TLC25L2ACP	TLC25L2ACJG
	2 mV	TLC25L2BCD	TLC25L2BCP	TLC25L2BCJG
	10 mV	TLC25M2CD	TLC25M2CP	TLC25M2CJG
	5 mV	TLC25M2ACD	TLC25M2ACP	TLC25M2ACJG
	2 mV	TLC25M2BCD	TLC25M2BCP	TLC25M2BCJG

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC252CDR).

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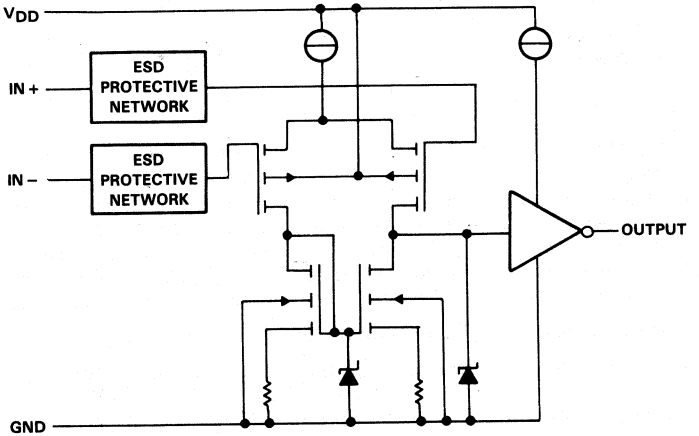
description (continued)

applications are possible using their low-voltage and low-power capabilities. The TLC252C series is wel suited to solve the difficult problems associated with single-battery and solar-cell-powered applications This series includes devices that are characterized for the commercial temperature range and are availabl in 8-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperture range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
JG	825 mW	6.6 mW/°C	528 mW
P	1000 mW	8.0 mW/°C	640 mW

ecommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1.4 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

lectrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Input offset voltage	TLC25_2C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		50	500		25	280		V/mV
				0°C to 70°C	7.5			50			15			
C_{MRR}	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	65	88		65	88		65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C		2000	4000		20	46		300	600	μA
				0°C to 70°C			4400			66			800	

All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
The output will swing to the potential of the ground pin.

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_2C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_2AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_2BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		300	375		25	34		200	250	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 100 pF, R_S = 50 Ω		2.2			0.11			0.635		MHz
SR	Slew rate at unity gain	See Figure 1		4.6			0.05			0.56		V/μs
	Overshoot factor	See Figure 1		35%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 100 pF		49°			38°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25			68			32		$nV/\sqrt{Hz}$
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

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operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

	TEST CONDITIONS	TEST CONDITIONS	TLC252_C			TLC25L2_C			TLC25M2_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

PARAMETER MEASUREMENT INFORMATION

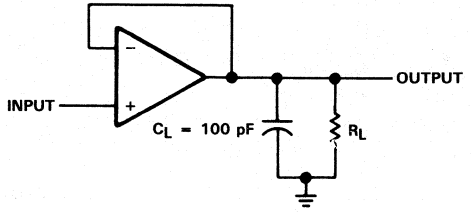


FIGURE 1. UNITY-GAIN AMPLIFIER

TYPICAL CHARACTERISTICS

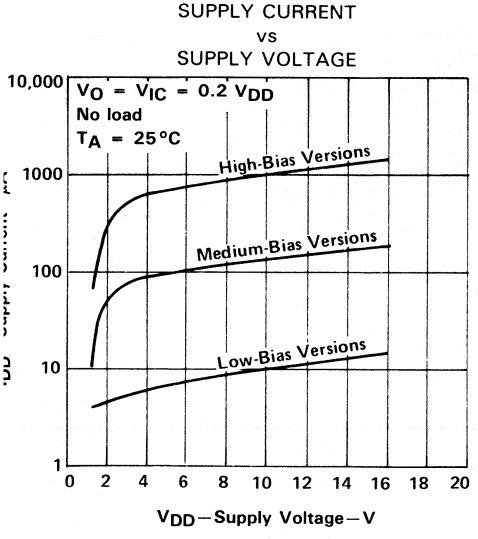


FIGURE 2

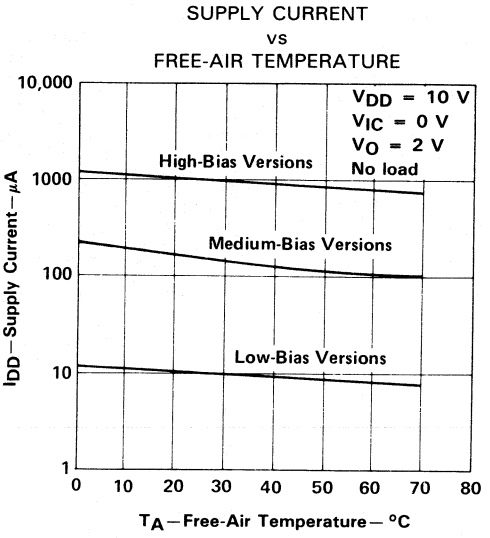


FIGURE 3

TYPICAL CHARACTERISTICS

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

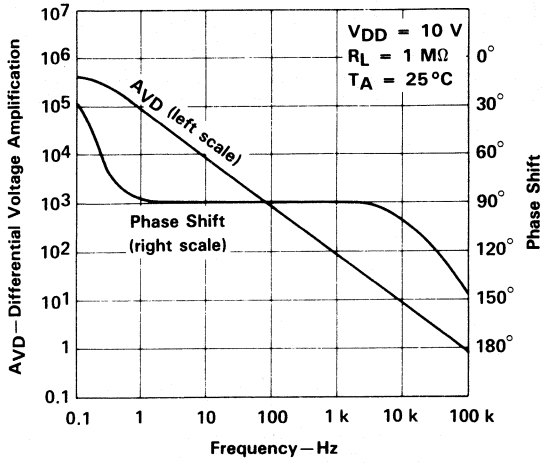


FIGURE 4

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

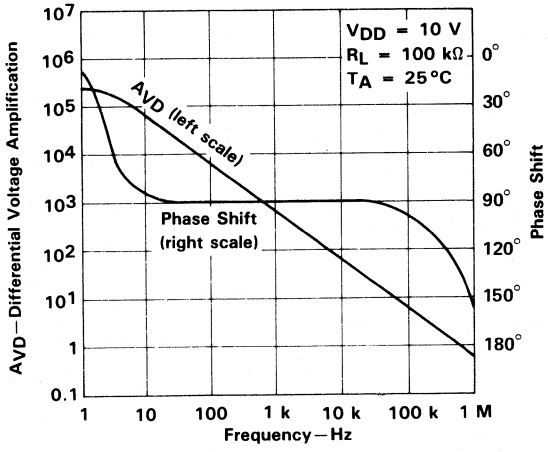


FIGURE 5

TYPICAL CHARACTERISTICS

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs FREQUENCY

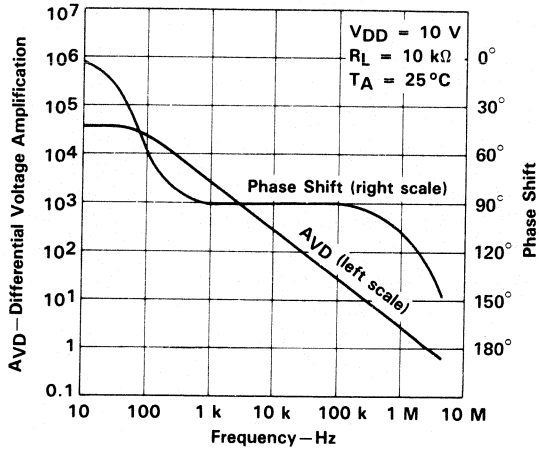


FIGURE 6

TYPICAL APPLICATION INFORMATION

latchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

output stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

supply configurations

Even though the TLC252C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

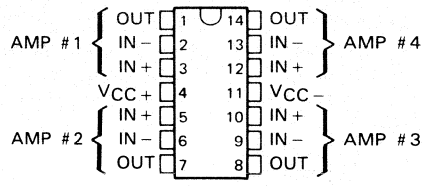
circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

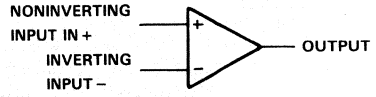
D2753, JUNE 1983—REVISED OCTOBER 1988

- **A Suffix Versions Offer 5-mV V_{IO}**
- **B Suffix Versions Offer 2-mV V_{IO}**
- **Wide Range of Supply Voltages 1.4 V to 16 V**
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Includes the Negative Rail**
- **Low Noise . . . 30 nV$\sqrt{Hz}$ Typ at f = 1 kHz (High-Bias Versions)**

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each amplifier)



Description

The TLC254C, TLC25L4C, and TLC25M4C are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These devices utilize the Texas Instruments silicon gate LinCMOS™ process, giving them stable input offset voltages that are available in selected grades of 2, 5, or 10 mV maximum, very high input impedances, and extremely low input offset and bias currents. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this series is ideally suited for battery-powered or energy-conserving applications. The series offers operation down to a 1.4-V supply, is stable at unity gain, and has excellent noise characteristics.

The TLC254C series is characterized for operation from 0°C to 70°C

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC254C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	10 mV	TLC254CD	TLC254CJ	TLC254CN
	5 mV	TLC254ACD	TLC254ACJ	TLC254ACN
	2 mV	TLC254BCD	TLC254BCJ	TLC254BCN
	10 mV	TLC25L4CD	TLC25L4CJ	TLC25L4CN
	5 mV	TLC25L4ACD	TLC25L4ACJ	TLC25L4ACN
	2 mV	TLC25L4BCD	TLC25L4BCJ	TLC25L4BCN
	10 mV	TLC25M4CD	TLC25M4CJ	TLC25M4CN
	5 mV	TLC25M4ACD	TLC25M4ACJ	TLC25M4ACN
	2 mV	TLC25M4BCD	TLC25M4BCJ	TLC25M4BCN

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC254CDR).

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description (continued)

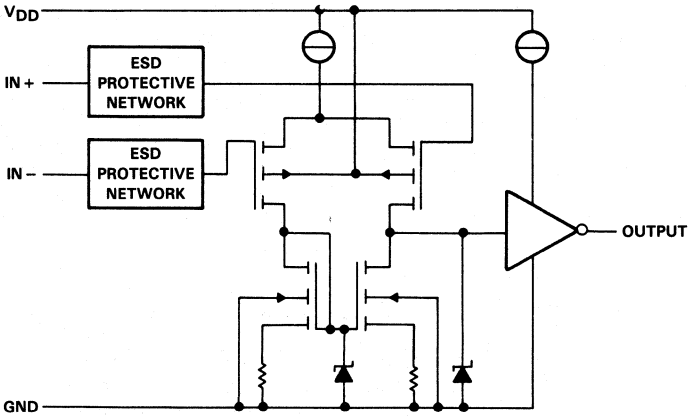
buffering are all easily designed with the TLC254C series devices. Remote and inaccessible equipmen applications are possible using their low-voltage and low-power capabilities. The TLC254C series is we suited to solve the difficult problems associated with single-battery and solar-cell-powered applications This series includes devices that are characterized for the commercial temperature range and are availabl in 14-pin plastic and ceramic dual-in-line (DIP) packages and the small outline (D) package.

DEVICE FEATURES

PARAMETER	TLC25L4C (LOW BIAS)	TLC25M4C (MEDIUM BIAS)	TLC254C (HIGH BIAS)
Supply current (Typ)	40 μA	600 μA	4000 μA
Slew rate (Typ)	0.04 V/μs	0.6 V/μs	4.5 V/μs
Input offset voltage (Max)			
TLC254C, TLC25L4C, TLC25M4C	10 mV	10 mV	10 mV
TLC254AC, TLC25L4AC, TLC25M4AC	5 mV	5 mV	5 mV
TLC254BC, TLC25L4BC, TLC25M4BC	2 mV	2 mV	2 mV
Offset voltage drift (Typ)	0.1 μV/month†	0.1 μV/month†	0.1 μV/month†
Offset voltage temperature coefficient (Typ)	0.7 μV/°C	2 μV/°C	5 μV/°C
Input bias current (Typ)	1 pA	1 pA	1 pA
Input offset current (Typ)	1 pA	1 pA	1 pA

† The long-term drift value applies after the first month.

schematic (each amplifier)



ıbsolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage range (any input) . . . . . −0.3 V to 18 V
Duration of short-circuit at (or below) 25°C free-air temperature (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal, with respect to the inverting input terminal.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

ecommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 1 V	0		0.2	V
	V_{DD} = 5 V	−0.2		4	
	V_{DD} = 10 V	−0.2		9	
	V_{DD} = 16 V	−0.2		14	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Input offset voltage	TLC25_4C	V_O = 1.4 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
αV_{IO}	Average temperature coefficient of input offset voltage			25°C to 70°C		5			0.7			2		μV/°C
I_{IO}	Input offset current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_{IC} = 5 V, V_O = 5 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	−0.2 to 9			−0.2 to 9			−0.2 to 9			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	8	8.6		8	8.6		8	8.6		V
				0°C to 70°C	7.8			7.8			7.8			
A_{VD}	Large-signal differential voltage amplification		V_O = 1 to 6 V, R_S = 50 Ω	25°C	10	40		50	500		25	280		V/mV
				0°C to 70°C	7.5			50			15			
CMRR	Common-mode rejection ratio		V_O = 1.4 V, V_{IC} = V_{ICR} min	25°C	65	88		65	88		65	88		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)		V_{DD} = 5 to 10 V, V_O = 1.4 V	25°C	65	82		70	88		70	88		dB
I_{OS}	Short-circuit output current		V_O = 0, V_{ID} = 100 mV	25°C		−55			−55			−55		mA
			V_O = V_{DD}, V_{ID} = −100 mV			15			15			15		
I_{DD}	Supply current		No load, V_O = 5 V, V_{IC} = 5 V	25°C		4000	8000		40	92		600	1200	μA
				0°C to 70°C			8800			132			1600	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

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electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC25_4C	V_O = 0.2 V, R_S = 50 Ω	25°C			10			10			10	mV
				0°C to 70°C			12			12			12	
		TLC25_4AC		25°C			5			5			5	
				0°C to 70°C			6.5			6.5			6.5	
		TLC25_4BC		25°C			2			2			2	
				0°C to 70°C			3			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1			1			1		μV/°C
I_{IO}	Input offset current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			300			300			300	
I_{IB}	Input bias current		V_O = 0.2 V	25°C		1			1			1		pA
				0°C to 70°C			600			600			600	
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OM}	Peak output voltage swing‡		V_{ID} = 100 mV	25°C	450	700		450	700		450	700		mV
A_{VD}	Large-signal differential voltage amplification		V_O = 100 to 300 mV, R_S = 50 Ω	25°C		10			20			20		V/mV
CMRR	Common-mode rejection ratio		V_O = 0.2 V, V_{IC} = V_{ICR} min	25°C	60	77		60	77		60	77		dB
I_{DD}	Supply current		No load, V_O = 0.2 V	25°C		600	750		50	68		400	500	μA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following value: For low bias R_L = 1 MΩ; for medium bias R_L = 100 kΩ; and for high bias R_L = 10 kΩ.
‡ The output will swing to the potential of the ground pin.

operating characteristics, V_{DD} = 10 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 100 pF, R_S = 50 Ω		2.2			0.11			0.635		MHz
SR	Slew rate at unity gain	See Figure 1		4.6			0.05			0.56		V/μs
	Overshoot factor	See Figure 1		30%			30%			35%		
ϕ_m	Phase margin at unity gain	A_V = 40 dB, R_S = 100 Ω, C_L = 100 pF		49°			38°			43°		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω		25			68			32		$nV/\sqrt{Hz}$
V_{o1}/V_{o2}	Cross talk attenuation	A_V = 100		120			120			120		dB

operating characteristics, V_{DD} = 1.4 V, T_A = 25°C

TEST CONDITIONS		TEST CONDITIONS	TLC254_C			TLC25L4_C			TLC25M4_C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
B_1	Unity-gain bandwidth	A_V = 40 dB, C_L = 10 pF, R_S = 50 Ω		75			12			12		kHz
SR	Slew rate at unity gain	See Figure 1		0.01			0.001			0.001		V/μs
	Overshoot factor	See Figure 1		30%			35%			35%		

PARAMETER MEASUREMENT INFORMATION

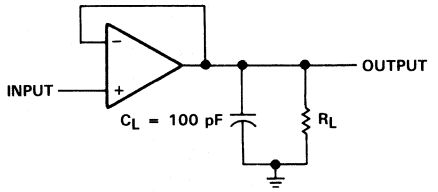

FIGURE 1. UNITY-GAIN AMPLIFIER

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

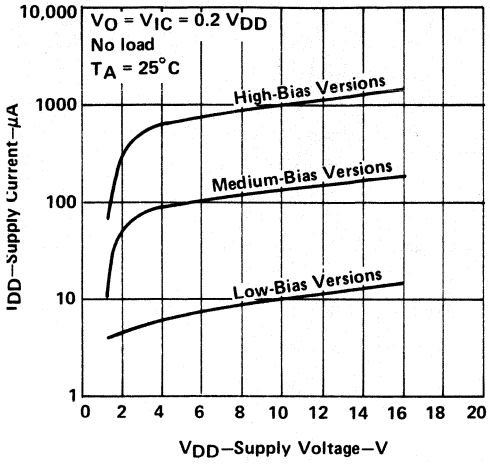


FIGURE 2

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

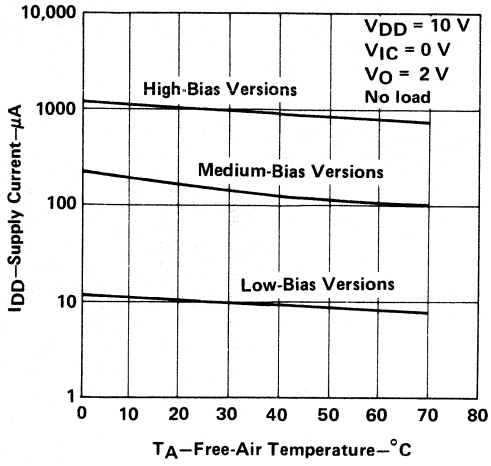


FIGURE 3

LOW-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

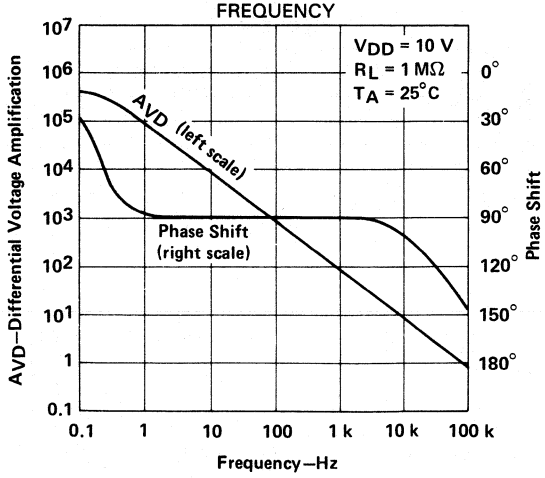


FIGURE 4

TYPICAL CHARACTERISTICS

MEDIUM-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

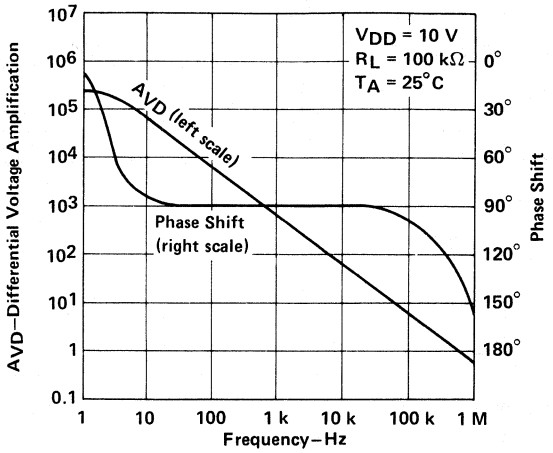


FIGURE 5

HIGH-BIAS VERSIONS
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
and PHASE SHIFT
vs
FREQUENCY

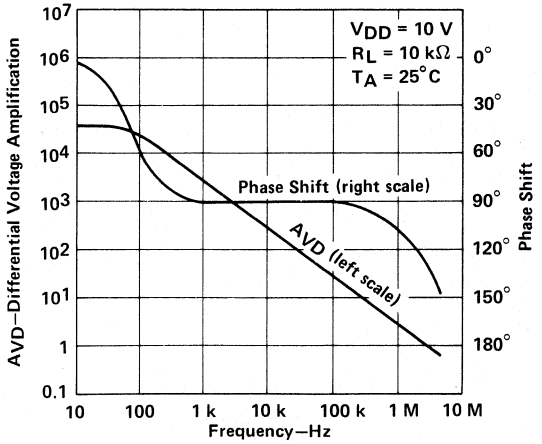


FIGURE 6

TYPICAL APPLICATION INFORMATION

ıtchup avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNPN structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the op amp supplies should be established simultaneously with, or before, application of any input signals.

ıutput stage considerations

The amplifier's output stage consists of a source follower connected pullup transistor and an open drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection, and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the GND pin potential.

ıupply configurations

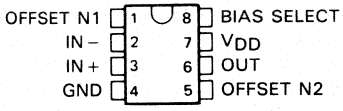
Even though the TLC254C series is characterized for single-supply operation, it can be used effectively in a split supply configuration if the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

ıircuit layout precautions

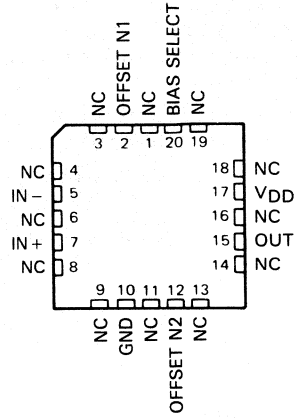
The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive DC leakages.

- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 5 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV $\sqrt{Hz}$ at f = 1 kHz (High-Bias Mode)**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC271 operational amplifier combines a wide range of input offset voltage grades with low offset voltage drift, and high input impedance. In addition, the TLC271 offers a bias select mode which allows the user to select the best combination of power dissipation and AC performance for a particular application. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 mV	TLC271BCD	—	TLC271BCJG	TLC271BCP
	5 mV	TLC271ACD	—	TLC271ACJG	TLC271ACP
	10 mV	TLC271CD	—	TLC271CJG	TLC271CP
−40°C to 85°C	2 mV	TLC271BID	—	TLC271BIJG	TLC271BIP
	5 mV	TLC271AID	—	TLC271AIJG	TLC271AIP
	10 mV	TLC271ID	—	TLC271IJG	TLC271IP
−55°C to 125°C	10 mV	—	TLC271MFK	TLC271MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC271BCDR)

DEVICE FEATURES TYPICAL at V_{DD} = 5 V, T_A = 25°C				
	BIAS-SELECT MODE			UNIT
	HIGH	MEDIUM	LOW	
P_D	3375	525	50	μW
SR	3.6	0.4	0.03	V/μs
V_n	25	32	68	nV/$\sqrt{Hz}$
B_1	1.7	0.5	0.09	MHz
A_{VD}	23	170	480	V/mV

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description (continued)

Using the bias select option, these cost-effective devices can be "programmed" to span a wide range of applications which previously required BiFET, NFET or bipolar technology. Three offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC271 (10 mV) to the TLC271B (2 mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC271. The devices also exhibit low-voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and output are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC271 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

bias select feature

The TLC271 offers a bias select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The trade-offs between bias levels involve AC performance and power dissipation (see Table 1).

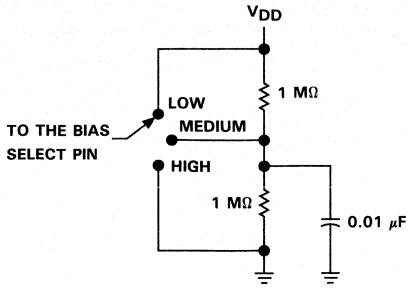
TABLE 1. EFFECT OF BIAS SELECTION ON PERFORMANCE

TYPICAL PARAMETER VALUES T_A = 25°C, V_{DD} = 5 V		MODE			UNITS
		HIGH-BIAS R_L = 10 kΩ	MEDIUM-BIAS R_L = 100 kΩ	LOW-BIAS R_L = 1 MΩ	
P_D	Power dissipation	3.4	0.5	0.05	mW
SR	Slew rate	3.6	0.4	0.03	V/μs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	1.7	0.5	0.09	MHz
ϕ_m	Phase margin	46°	40°	34°	
A_{VD}	Large-signal differential voltage amplification	23	170	480	V/mV

bias selection

Bias selection is achieved by connecting the bias select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias select pin be connected to the mid-point between the supply rails. This proceduce is simple in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the mid-point may be used if it is within the voltages specified in the following table.

ıias selection (continued)



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to $V_{DD}-1$ V
HIGH	GND

FIGURE 1. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

ıigh-bias mode

In the high-bias mode, the TLC271 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices, but at only a fraction of the power dissipation. Unity-gain bandwidth is typically greater than 1 MHz.

nedium-bias mode

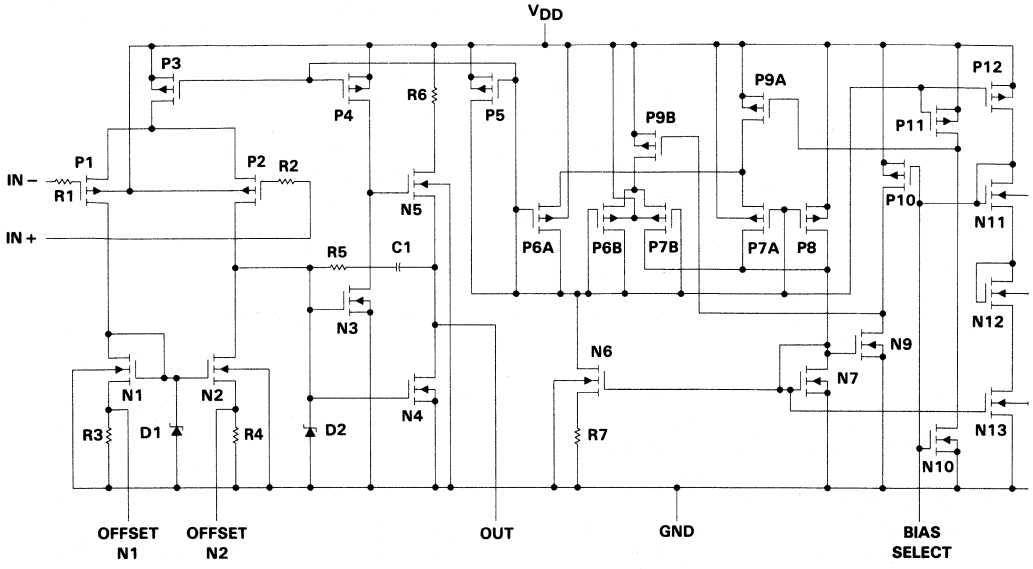
The TLC271 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

ow-bias mode

In the low-bias mode, the TLC271 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

ORDER OF CONTENTS

equivalent schematic



bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . ±30 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

OTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

ecommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		5		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		2.1			2.2		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
			−55°C	3	3.8		7.8	8.5		
			125°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
			−55°C	3.5	35		7	50		
			125°C	3.5	16		7	27		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
			−55°C	60	81		60	87		
			125°C	60	84		60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
			−55°C	60	90		60	90		
			125°C	60	97		60	97		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
			−55°C		1000	2500		1475	3000	
			125°C		475	1100		625	1400	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

TEXAS INSTRUMENTS
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HIGH-BIAS MODE

Electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.34	2		0.39	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				−40°C	3	3.8		7.8	8.5		
				85°C	3	3.8		7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				−40°C	3.5	32		7	46		
				85°C	3.5	19		7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				−40°C	60	81		60	87		
				85°C	60	86		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				−40°C	60	92		60	92		
				85°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
				−40°C		950	2200		1375	2500	
				85°C		525	1200		725	1600	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.34	2		0.39	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.8			2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 10 kΩ	25°C	3.2	3.8		8	8.5		V
				0°C	3	3.8		7.8	8.5		
				70°C	3	3.8		7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 10 kΩ, See Note 6	25°C	5	23		10	36		V/mV
				0°C	4	27		7.5	42		
				70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	80		65	85		dB
				0°C	60	84		60	88		
				70°C	60	85		60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	65	95		65	95		dB
				0°C	60	94		60	94		
				70°C	60	96		60	96		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = 0	25°C		−1.4			−1.9		μA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		675	1600		950	2000	μA
				0°C		775	1800		1125	2200	
				70°C		575	1300		750	1700	

†Full range is −0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		49°		
				−55°C		52°		
				125°C		44°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		49°		
				−40°C		52°		
				85°C		46°		

HIGH-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 99	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 98	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		49°		
				0°C		50°		
				70°C		46°		

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

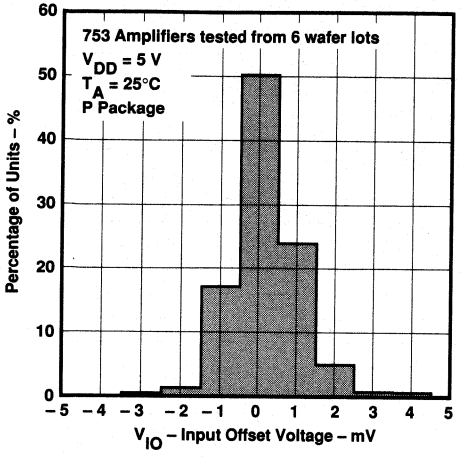

FIGURE 2

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

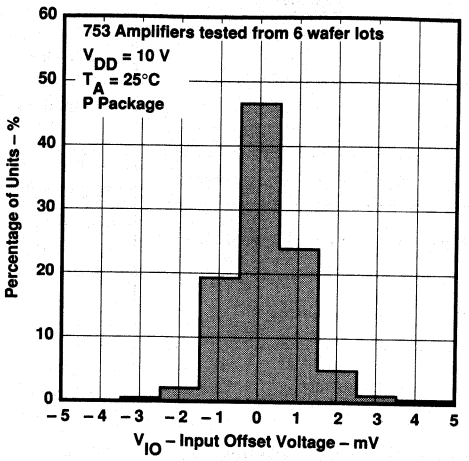

FIGURE 3

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

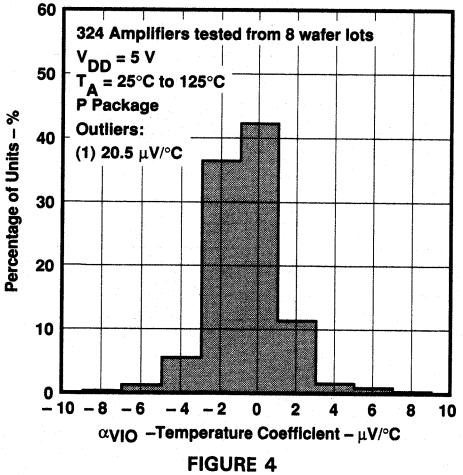

FIGURE 4

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

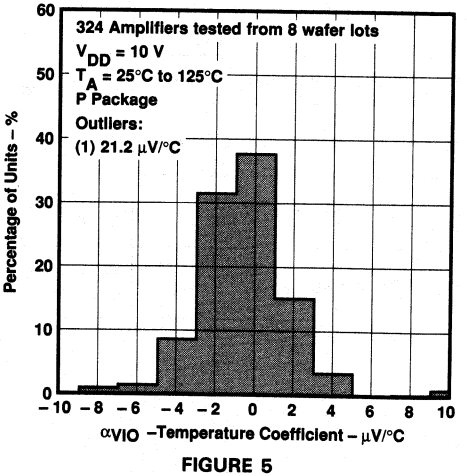

FIGURE 5

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

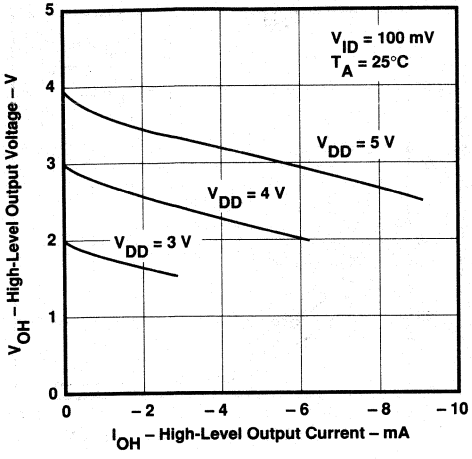

FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

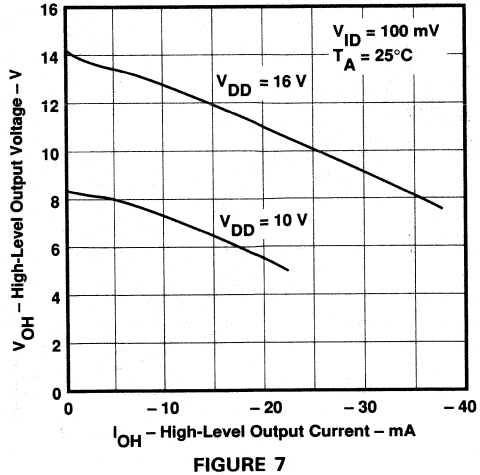

FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

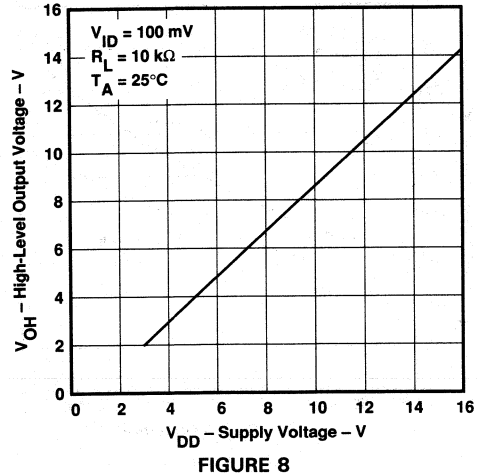

FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

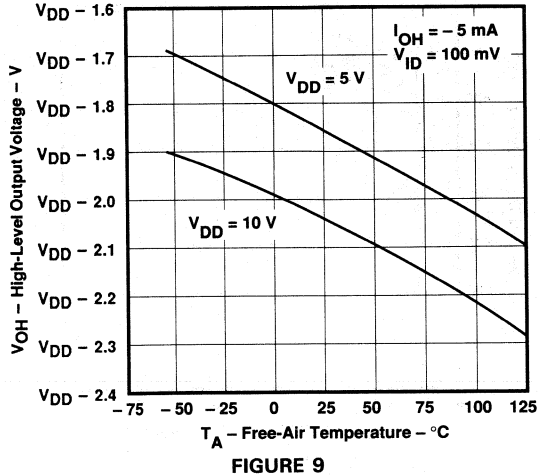

FIGURE 9

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

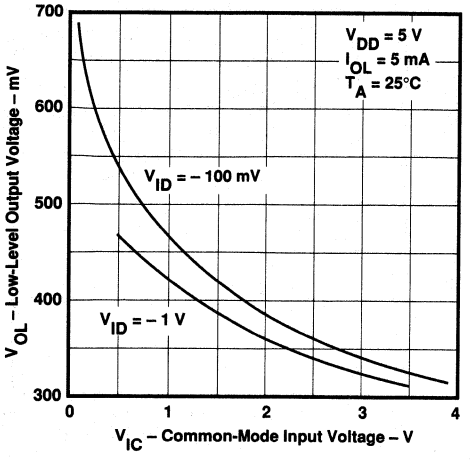

FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

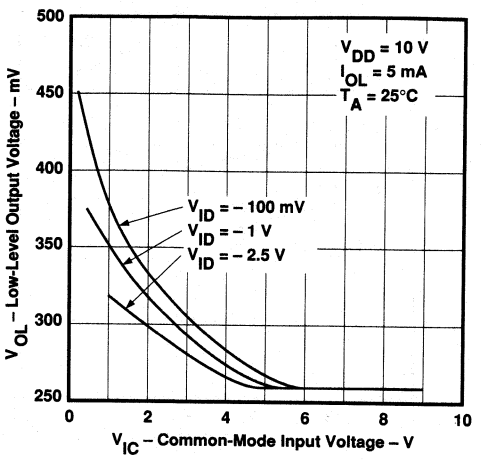

FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

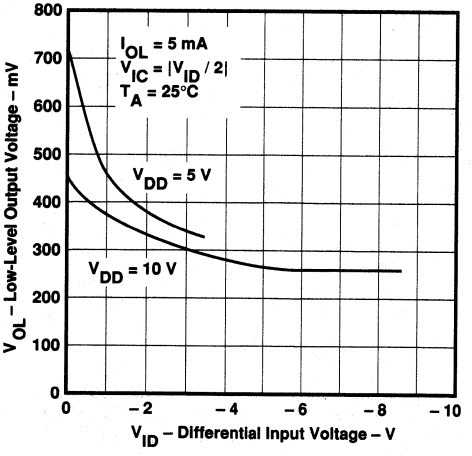

FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

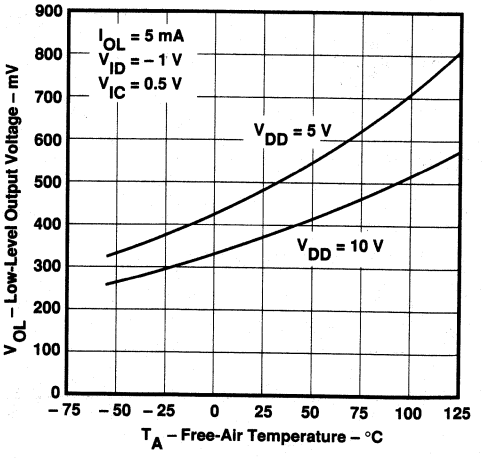

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

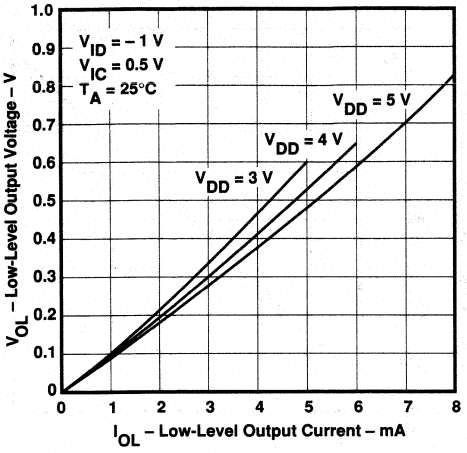

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

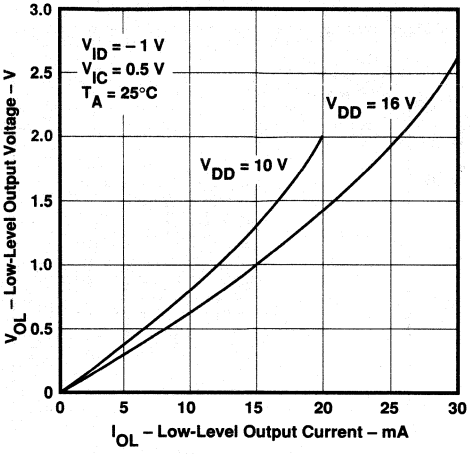

FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

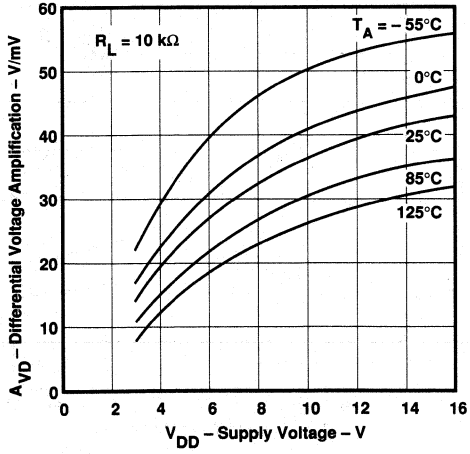

FIGURE 16

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

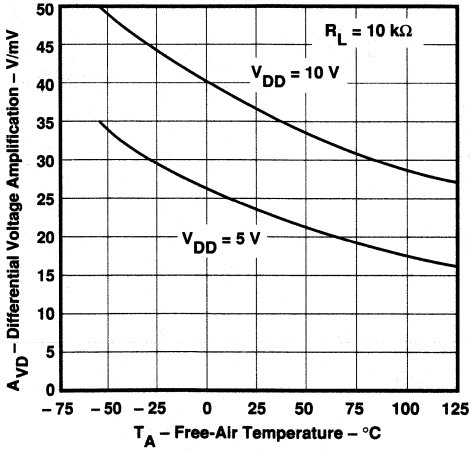

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

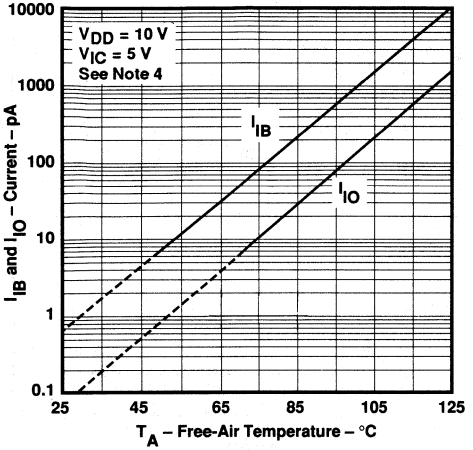

FIGURE 18

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

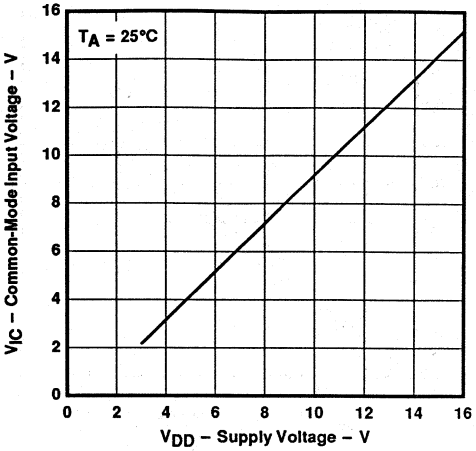

FIGURE 19

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

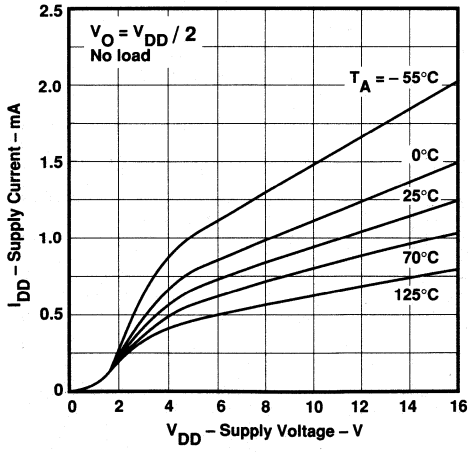

FIGURE 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

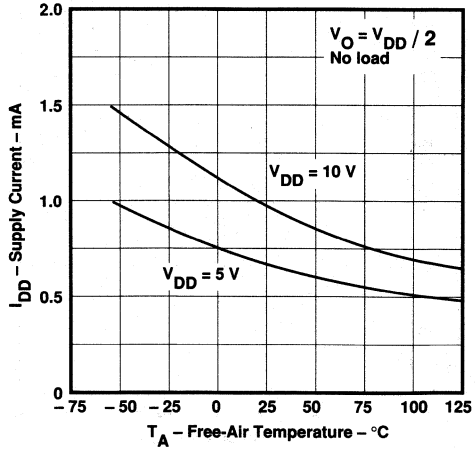

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

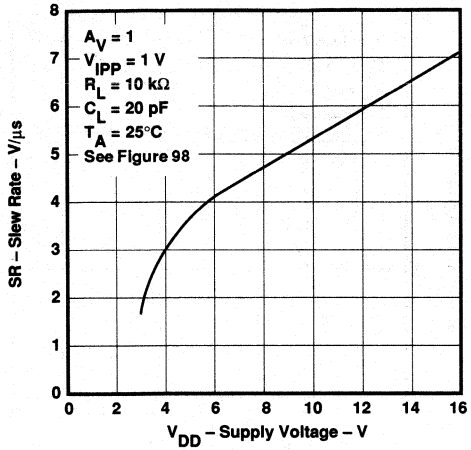

FIGURE 22

SLEW RATE
vs
FREE-AIR TEMPERATURE

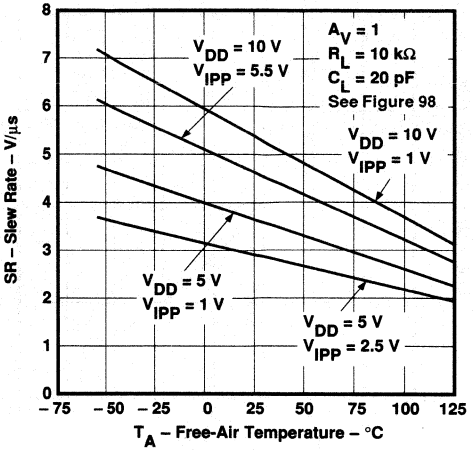

FIGURE 23

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

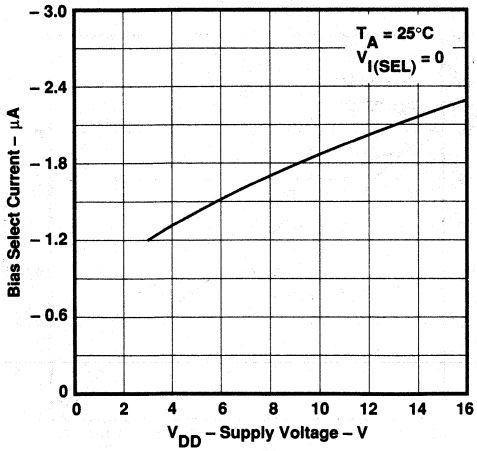

FIGURE 24

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

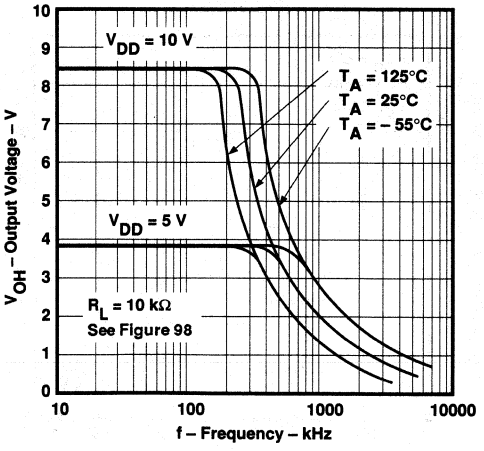

FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

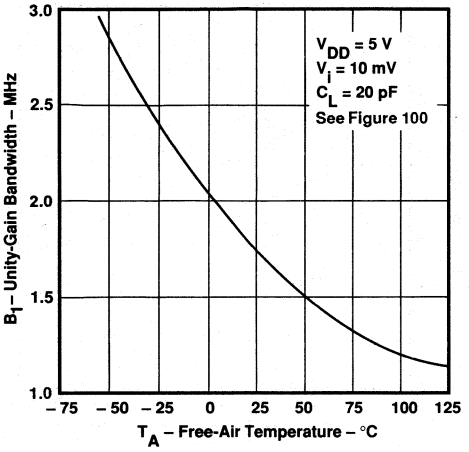

FIGURE 26

UNDITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

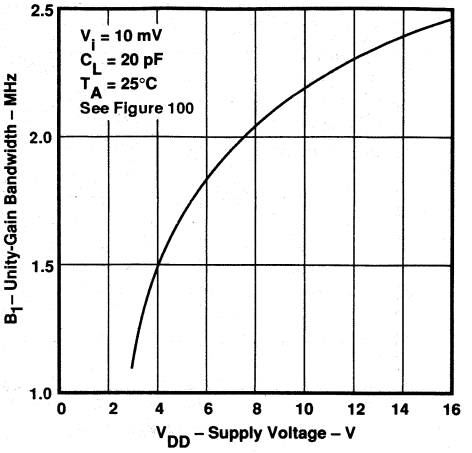

FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

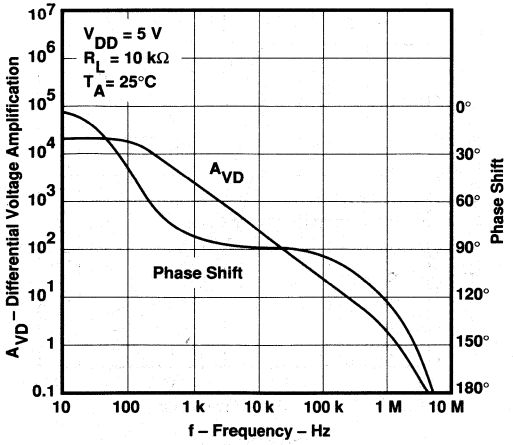

FIGURE 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

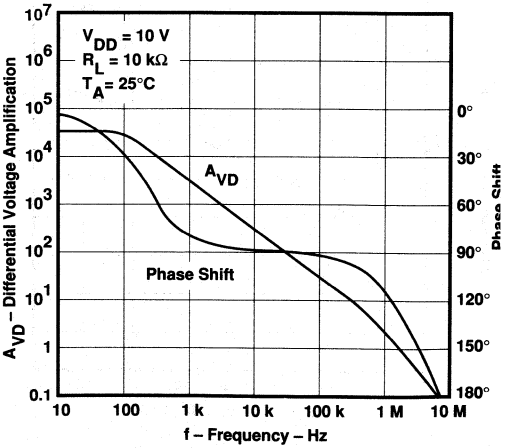

FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

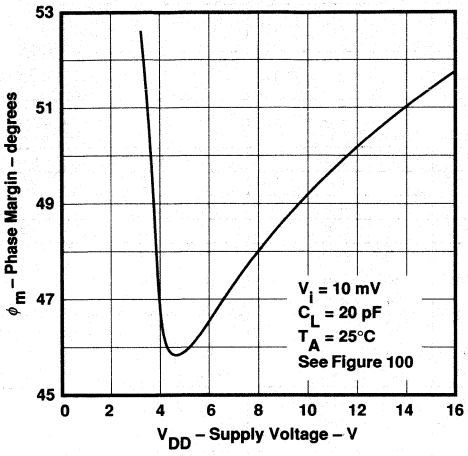

FIGURE 30

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

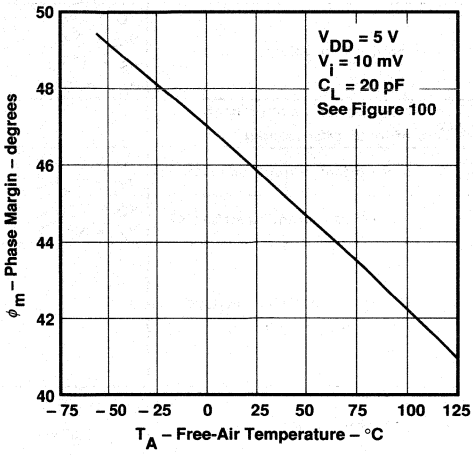

FIGURE 31

PHASE MARGIN
vs
CAPACITIVE LOAD

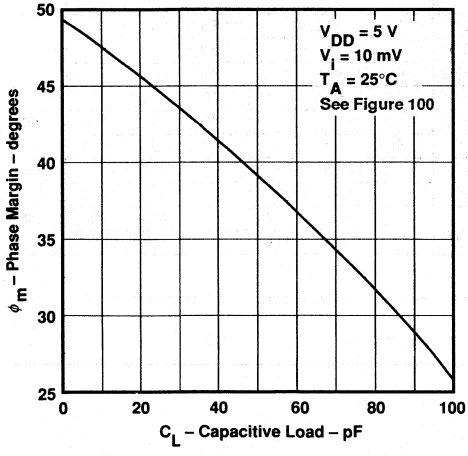

FIGURE 32

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

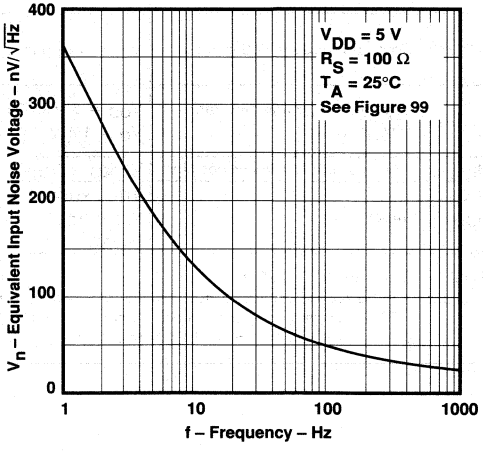

FIGURE 33

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
			−55°C	3	3.9		7.8	8.6		
			125°C	3	4		7.8	8.8		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
			−55°C	15	290		15	420		
			125°C	15	120		15	190		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
			−55°C	60	89		60	93		
			125°C	60	91		60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
			−55°C	60	91		60	91		
			125°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD}/2	25°C		−130			−160		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		105	280		143	300	μA
			−55°C		170	440		245	500	
			125°C		70	180		90	240	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

lectrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.25	2		0.26	2	
				Full range			3.5			3.5	
$^{x}V_{IO}$	Average temperature coefficient of input offset voltage			25°C to 85°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				−40°C	3	3.9		7.8	8.7		
				85°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				−40°C	15	270		15	390		
				85°C	15	130		15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				−40°C	60	90		60	93		
				85°C	60	90		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				−40°C	60	91		60	91		
				85°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}/2	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		105	280		143	300	μA
				−40°C		158	400		225	450	
				85°C		80	200		103	260	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.25	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.7			2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 100 kΩ	25°C	3.2	3.9		8	8.7		V
				0°C	3	3.9		7.8	8.7		
				70°C	3	4		7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 100 kΩ, See Note 6	25°C	25	170		25	275		V/mV
				0°C	15	200		15	320		
				70°C	15	140		15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	91		65	94		dB
				0°C	60	91		60	94		
				70°C	60	92		60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	93		70	93		dB
				0°C	60	92		60	92		
				70°C	60	94		60	94		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}/2	25°C		−130			−160		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		105	280		143	300	μA
				0°C		125	320		173	400	
				70°C		85	220		110	280	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−55°C		43°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−55°C		47°		
				125°C		39°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				−40°C		46°		
				85°C		41°		

MEDIUM-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 98	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		43°		
				0°C		44°		
				70°C		42°		

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

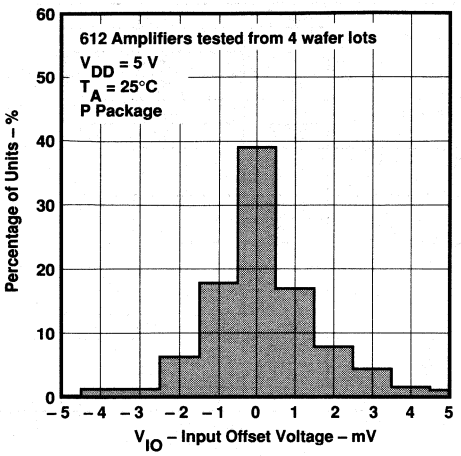

FIGURE 34

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

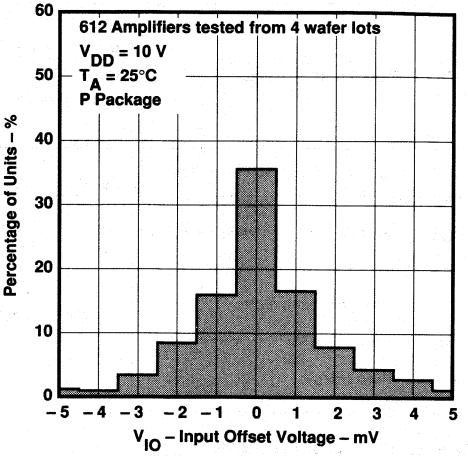

FIGURE 35

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

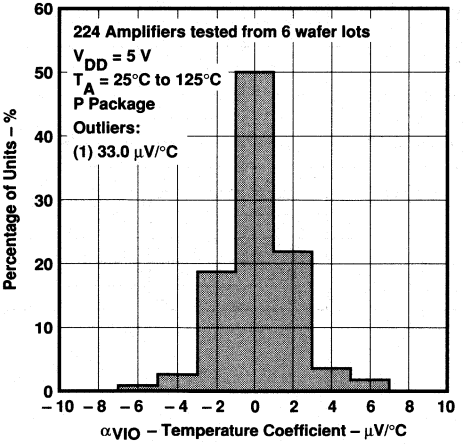

FIGURE 36

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

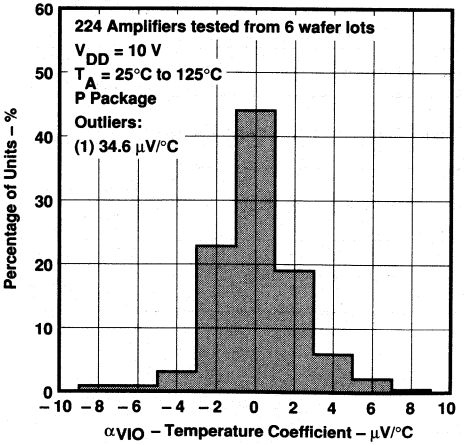

FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

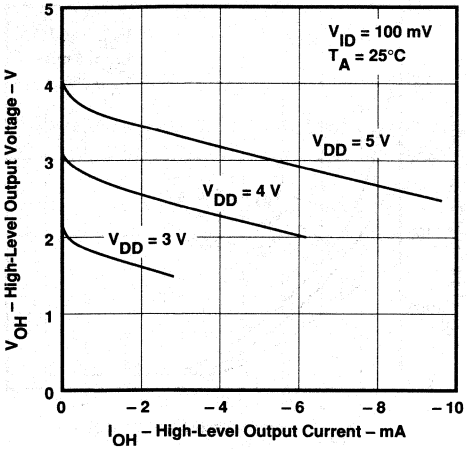

FIGURE 38

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

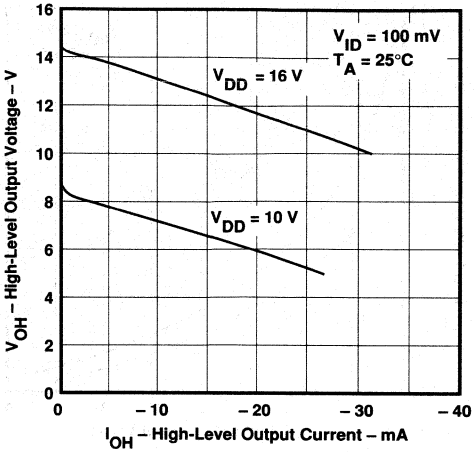

FIGURE 39

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

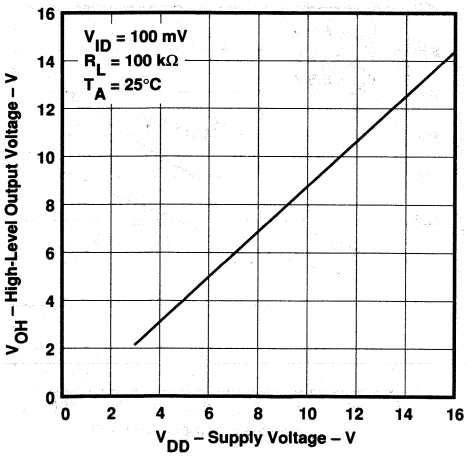

FIGURE 40

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

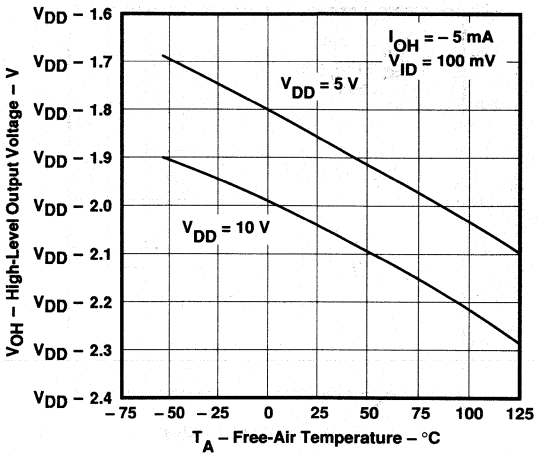

FIGURE 41

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

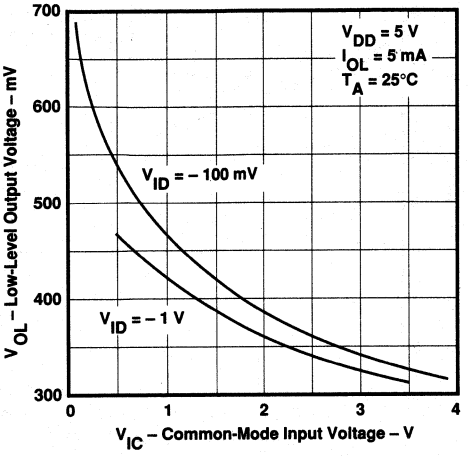

FIGURE 42

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

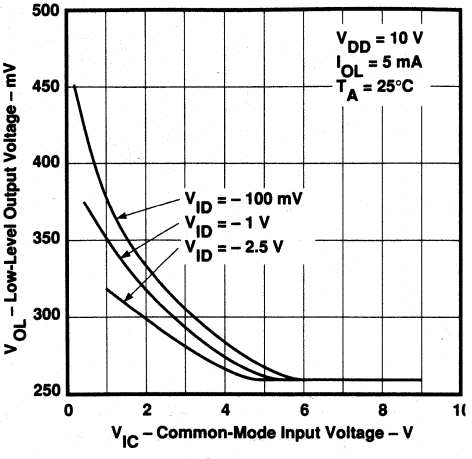

FIGURE 43

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

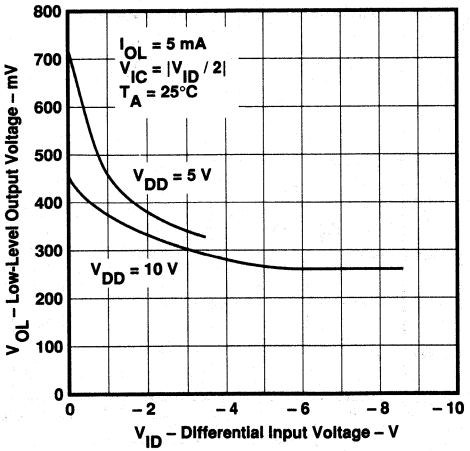

FIGURE 44

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

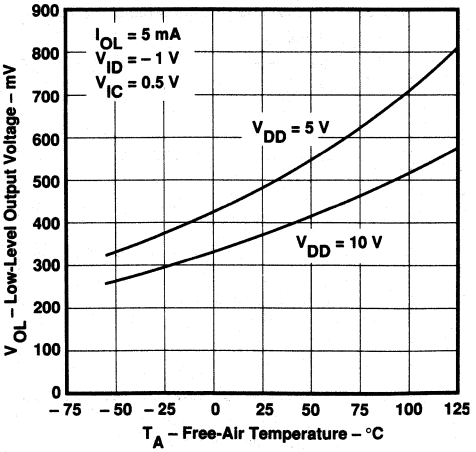

FIGURE 45

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

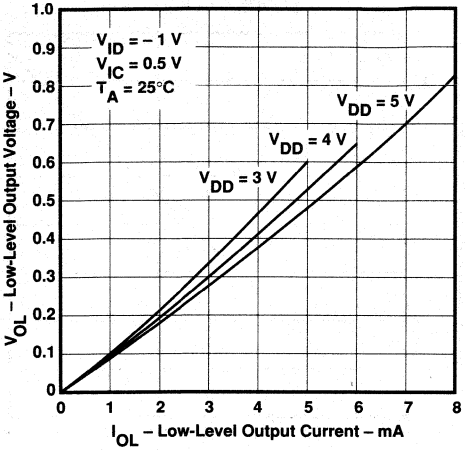

FIGURE 46

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

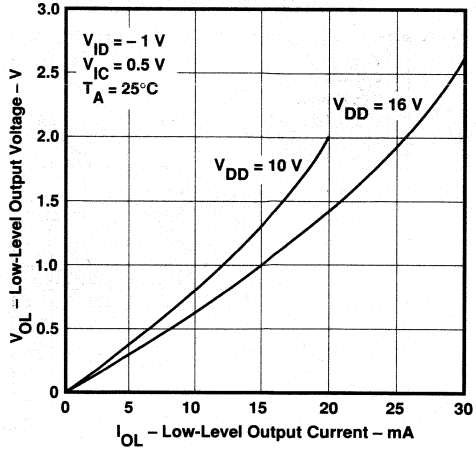

FIGURE 47

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

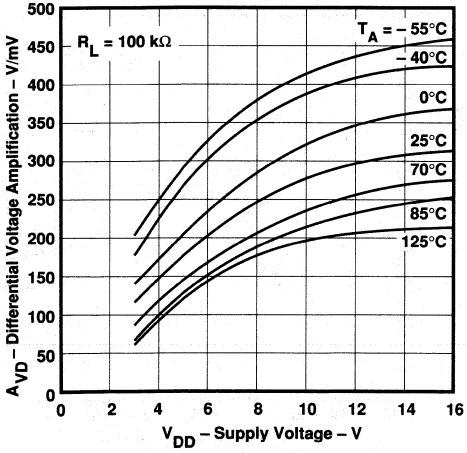

FIGURE 48

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

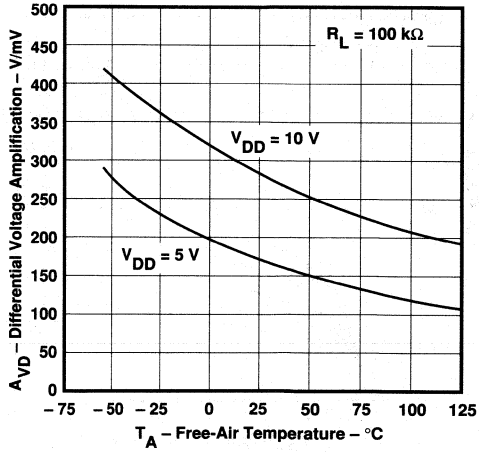

FIGURE 49

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

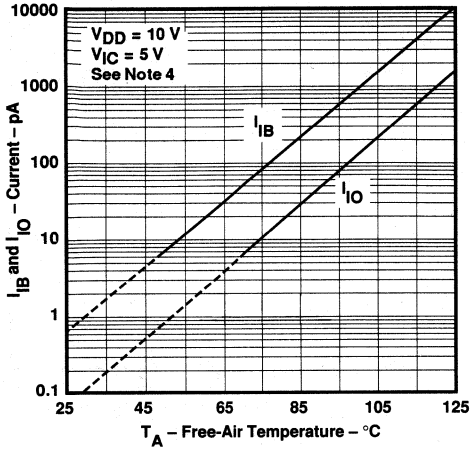

FIGURE 50

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

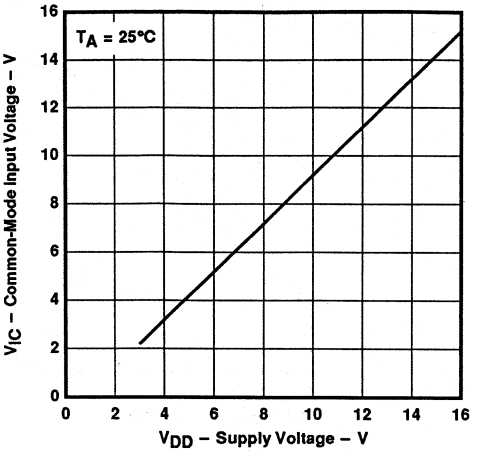

FIGURE 51

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

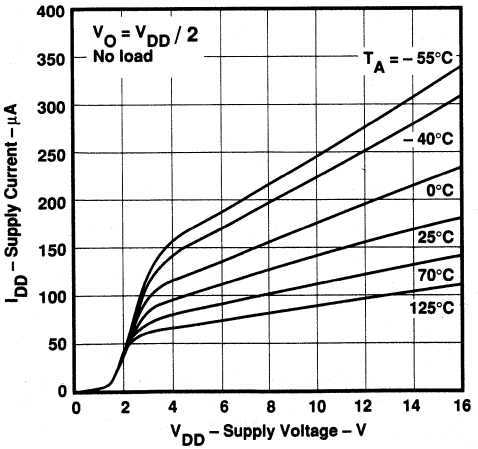

FIGURE 52

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

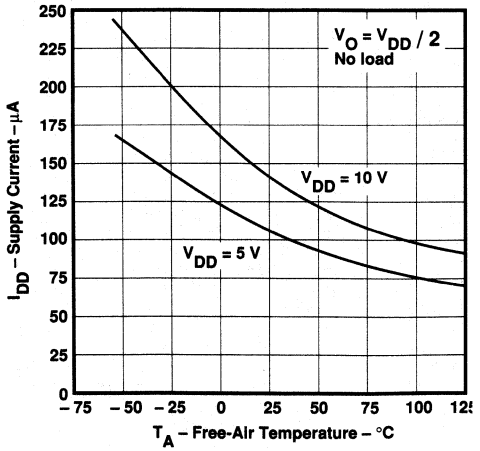

FIGURE 53

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

NOTE 4: The typical values of input bias current and input offset current and input offset current below 5 pA were determined mathematically

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

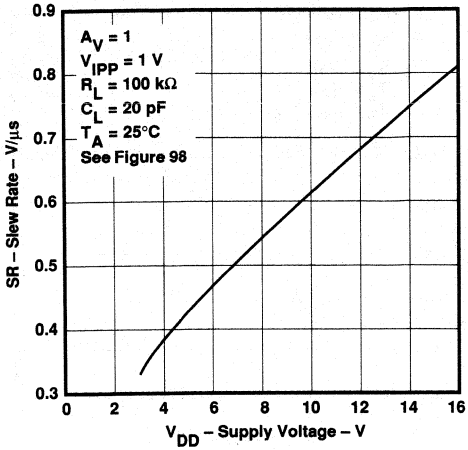

FIGURE 54

SLEW RATE
vs
FREE-AIR TEMPERATURE

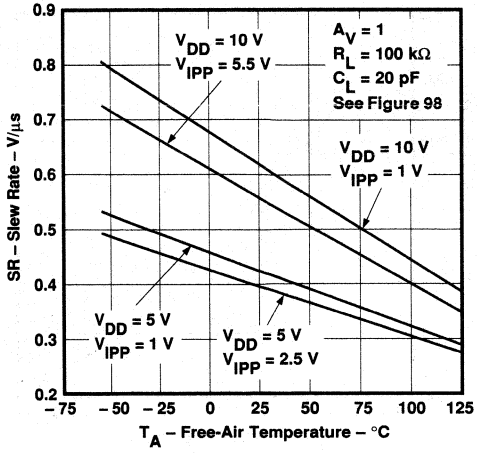

FIGURE 55

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

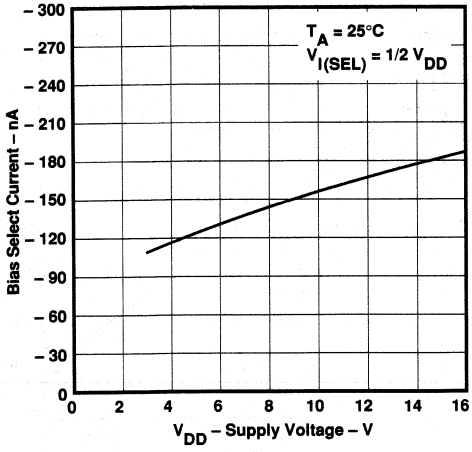

FIGURE 56

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

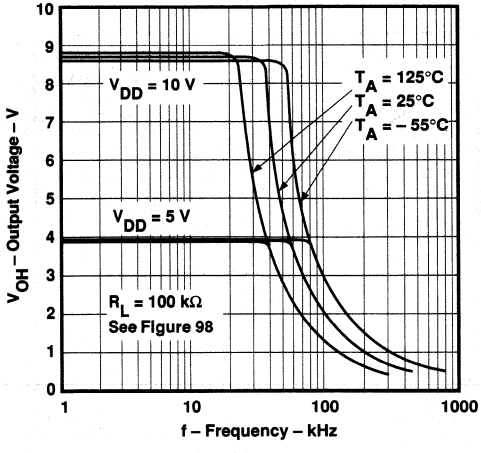

FIGURE 57

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

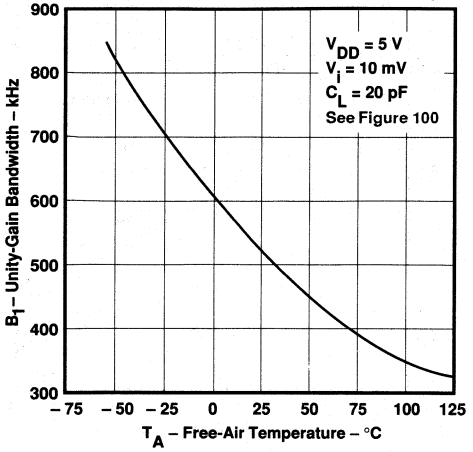

FIGURE 58

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

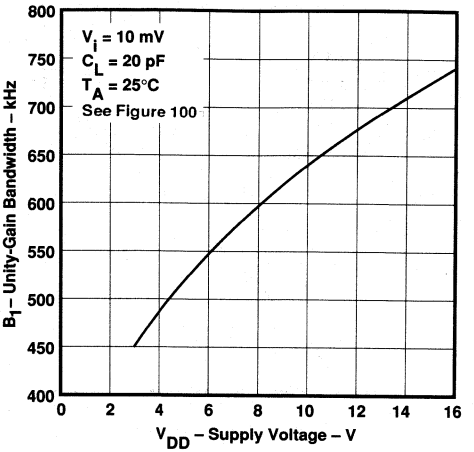

FIGURE 59

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

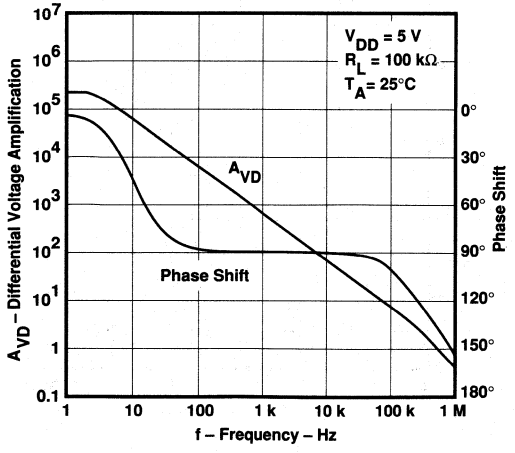

FIGURE 60

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

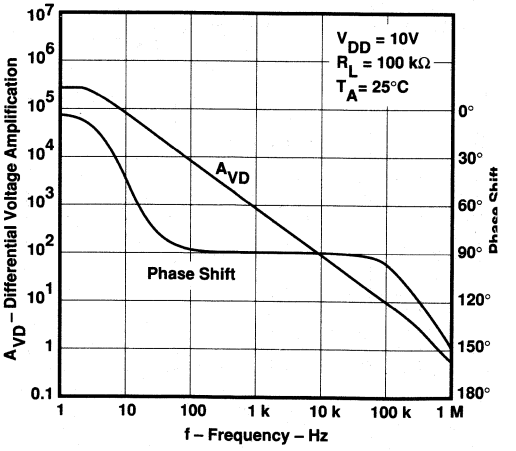

FIGURE 61

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

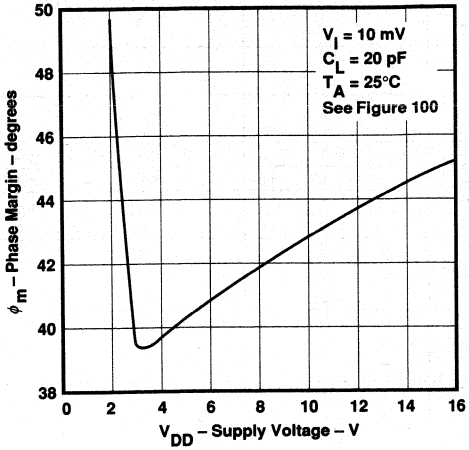

FIGURE 62

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

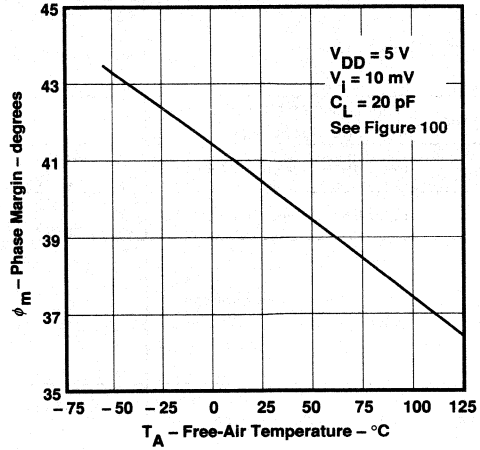

FIGURE 63

PHASE MARGIN
vs
CAPACITIVE LOAD

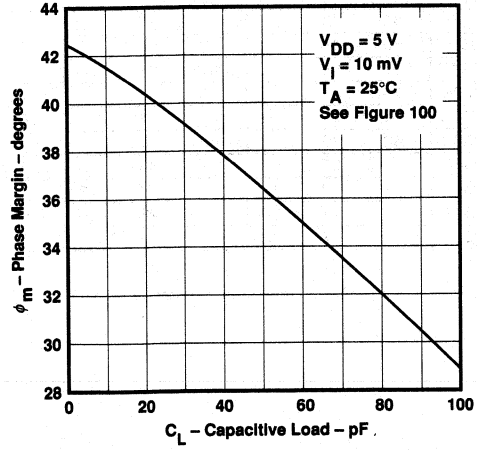

FIGURE 64

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

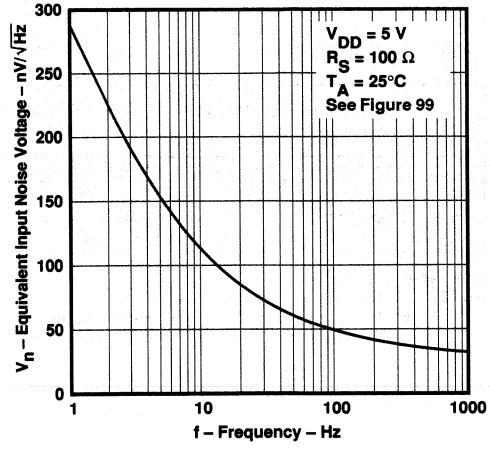

FIGURE 65

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			−55°C	3	4.1		7.8	8.8		
			125°C	3	4.2		7.8	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
			−55°C		0	50		0	50	
			125°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			−55°C	25	1000		25	1775		
			125°C	25	200		25	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
			−55°C	60	95		60	97		
			125°C	60	85		60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
			−55°C	60	97		60	97		
			125°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin	$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
			−55°C		17	30		28	48	
			125°C		7	12		9	15	

†Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

Electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271I	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			13			13	
		TLC271AI		25°C		0.9	5		0.9	5	
				Full range			7			7	
		TLC271BI		25°C		0.24	2		0.26	2	
				Full range			3.5			3.5	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				−40°C	3	4.1		7.8	8.9		
				85°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				−40°C		0	50		0	50	
				85°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				−40°C	50	900		50	1550		
				85°C	50	330		50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				−40°C	60	95		60	97		
				85°C	60	95		60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				−40°C	60	97		60	97		
				85°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
				−40°C		16	27		25	43	
				85°C		7	13		10	18	

†Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

LOW-BIAS MODE

electrical characteristics at specified free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	V_{DD} = 5 V			V_{DD} = 10 V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC271C	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
				Full range			12			12	
		TLC271AC		25°C		0.9	5		0.9	5	
				Full range			6.5			6.5	
		TLC271BC		25°C		0.24	2		0.26	2	
				Full range			3			3	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.1			0.1		pA
				70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6			0.7		pA
				70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)			25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
				Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
				0°C	3	4.1		7.8	8.9		
				70°C	3	4.2		7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV, I_{OL} = 0	25°C		0	50		0	50	mV
				0°C		0	50		0	50	
				70°C		0	50		0	50	
A_{VD}	Large-signal differential voltage amplification		R_L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
				0°C	50	700		50	1030		
				70°C	50	380		50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min	25°C	65	94		65	97		dB
				0°C	60	95		60	97		
				70°C	60	95		60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	70	97		70	97		dB
				0°C	60	97		60	97		
				70°C	60	98		60	98		
$I_{I(SEL)}$	Input current to bias select pin		$V_{I(SEL)}$ = V_{DD}	25°C		65			95		nA
I_{DD}	Supply current		V_O = V_{DD}/2, V_{IC} = V_{DD}/2, No load	25°C		10	17		14	23	μA
				0°C		12	21		18	33	
				70°C		8	14		11	20	

†Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

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LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				−55°C		39°		
				125°C		25°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				−55°C		43°		
				125°C		29°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				−40°C		42°		
				85°C		32°		

LOW-BIAS MODE

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		34°		
				0°C		36°		
				70°C		30°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 98	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 99	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 98	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 100	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 100	25°C		38°		
				0°C		40°		
				70°C		34°		

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

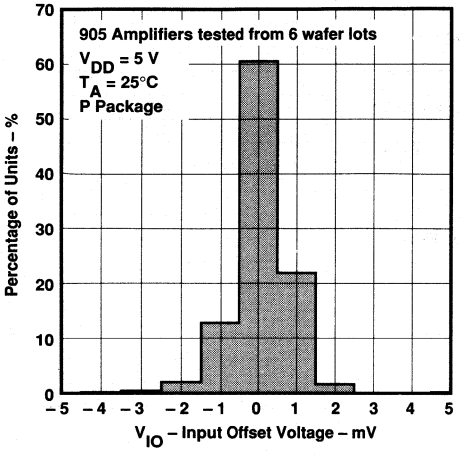


FIGURE 66

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE

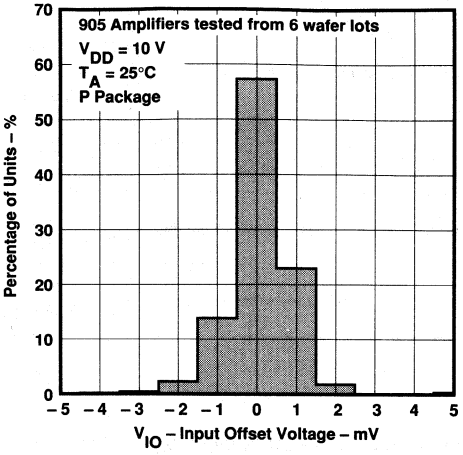


FIGURE 67

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

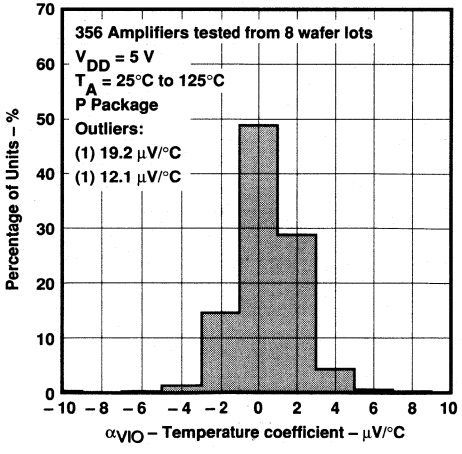


FIGURE 68

DISTRIBUTION OF TLC271
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

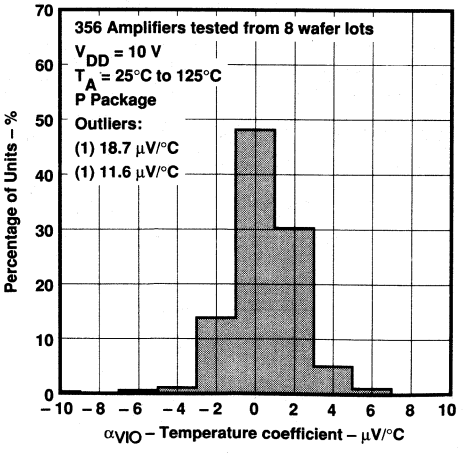


FIGURE 69

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

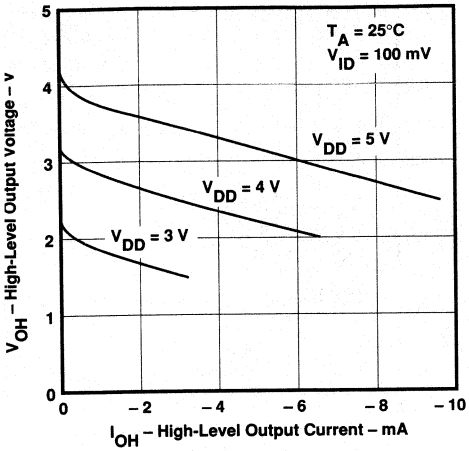


FIGURE 70

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

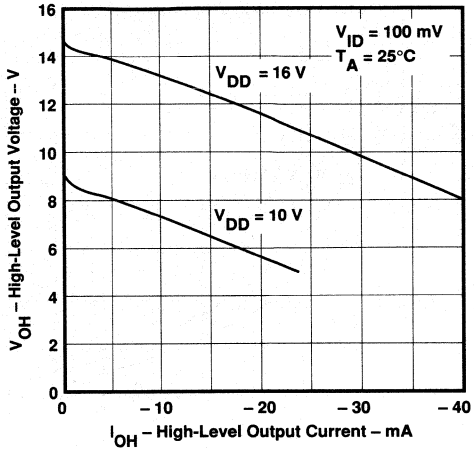


FIGURE 71

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

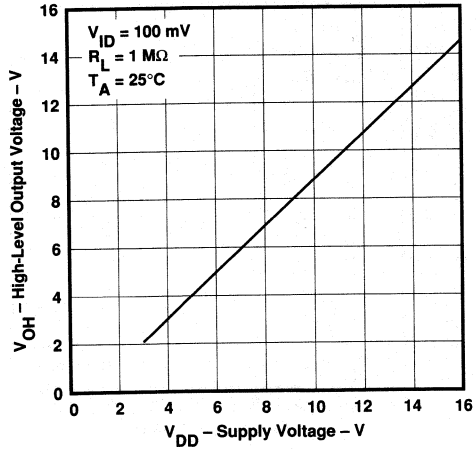


FIGURE 72

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

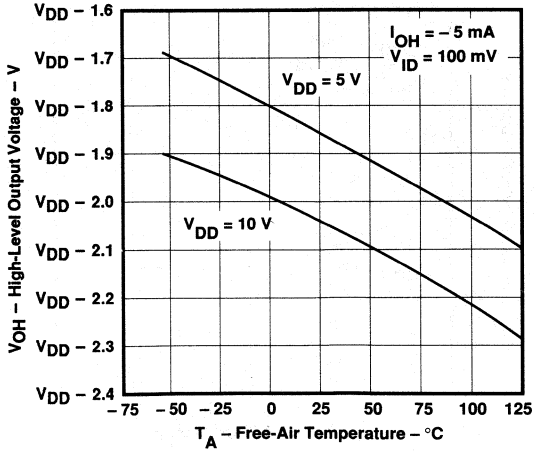


FIGURE 73

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

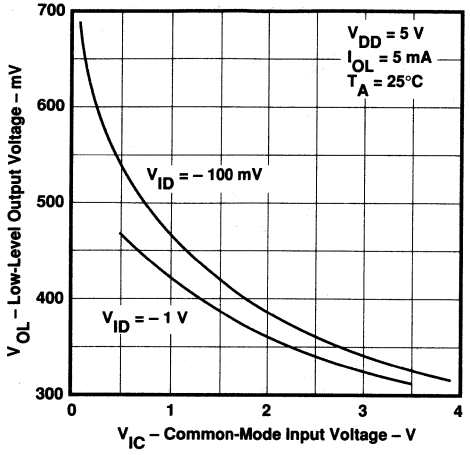


FIGURE 74

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

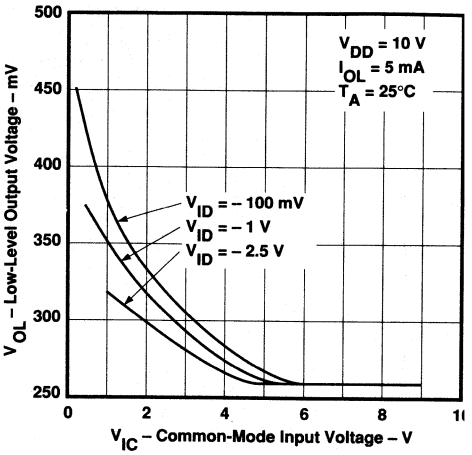


FIGURE 75

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

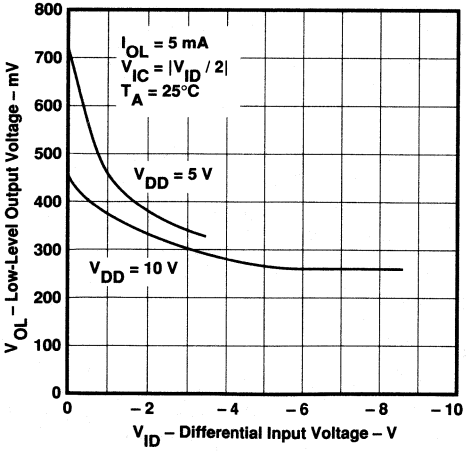


FIGURE 76

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

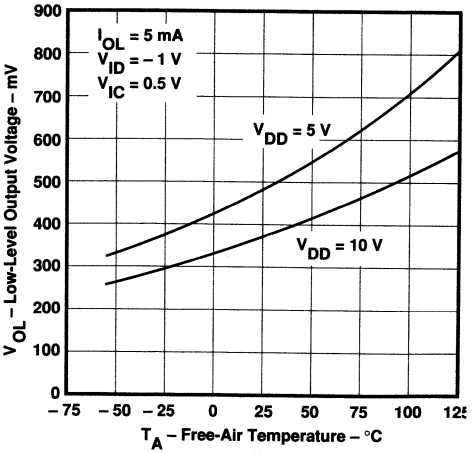


FIGURE 77

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

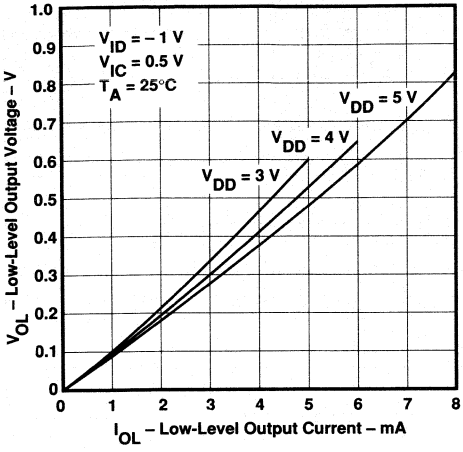


FIGURE 78

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

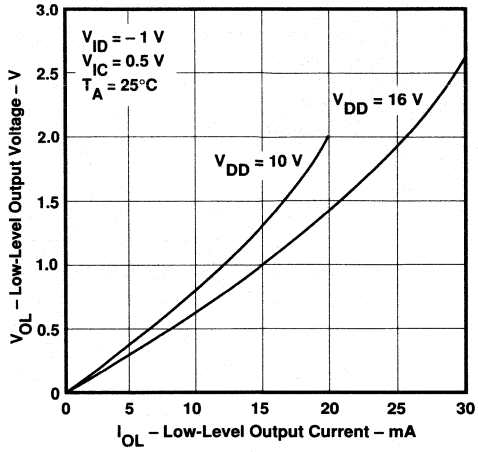


FIGURE 79

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

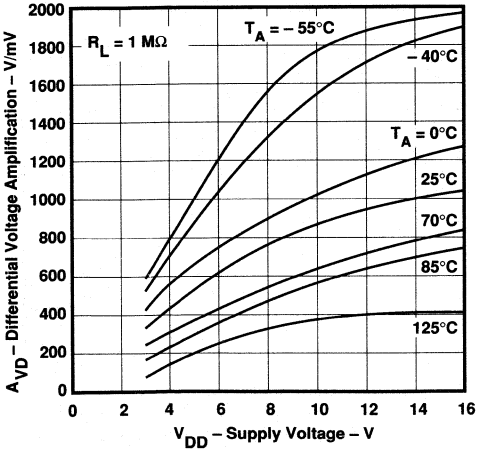


FIGURE 80

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

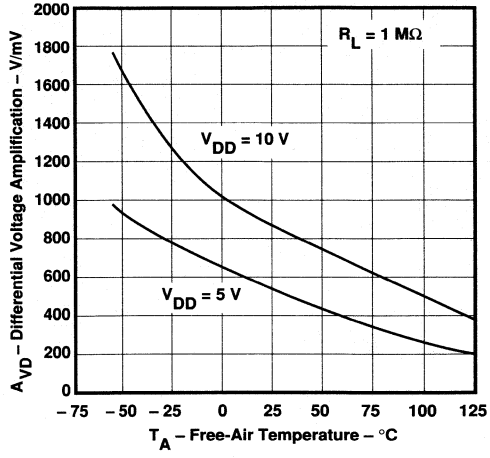


FIGURE 81

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

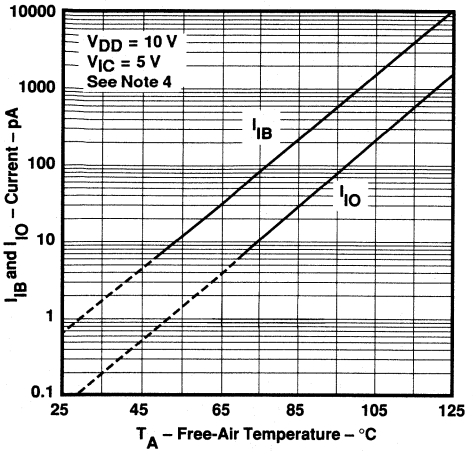


FIGURE 82

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

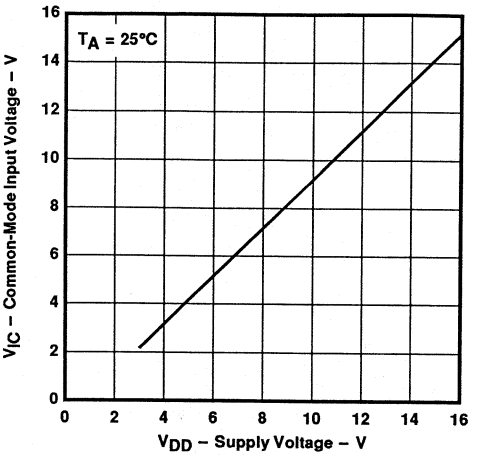


FIGURE 83

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

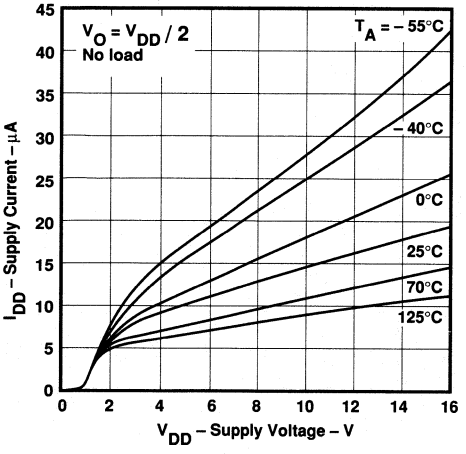


FIGURE 84

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

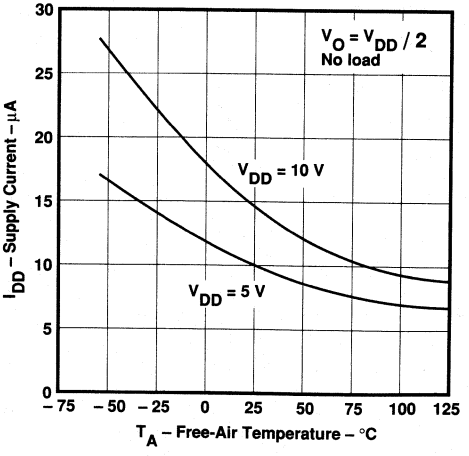


FIGURE 85

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

SLEW RATE
vs
SUPPLY VOLTAGE

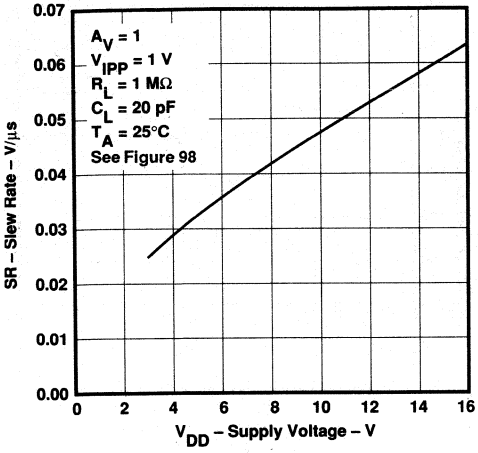


FIGURE 86

SLEW RATE
vs
FREE-AIR TEMPERATURE

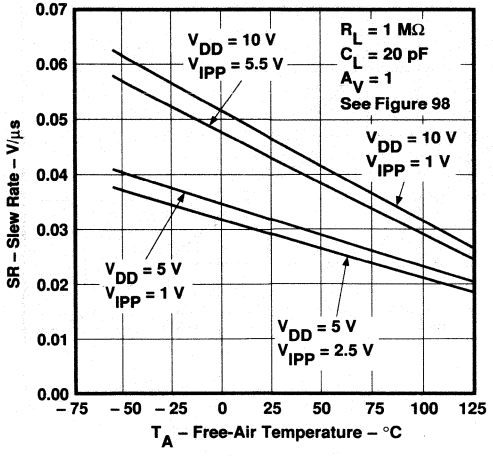


FIGURE 87

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

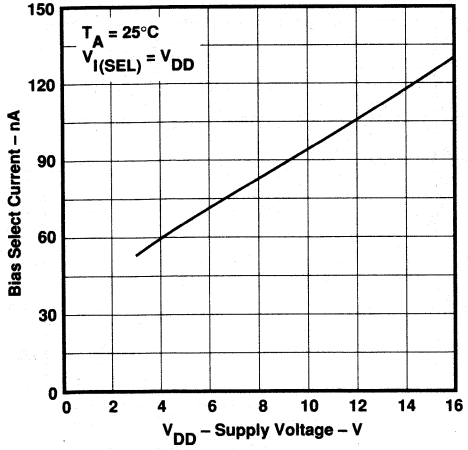


FIGURE 88

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

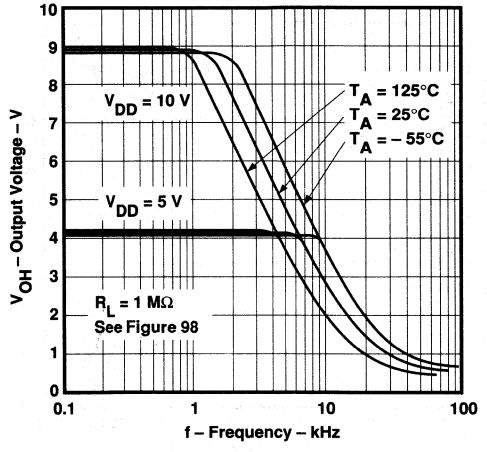


FIGURE 89

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

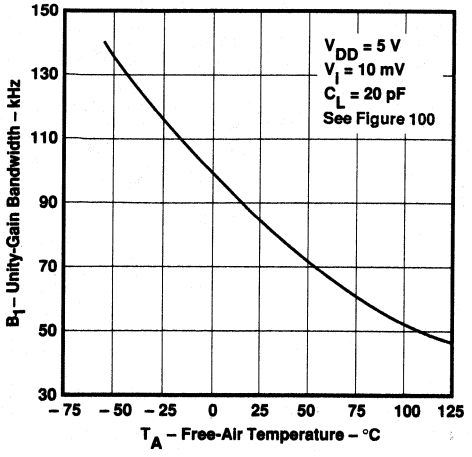


FIGURE 90

UNDITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

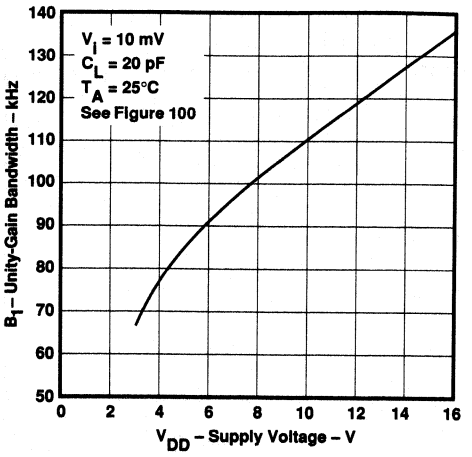


FIGURE 91

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

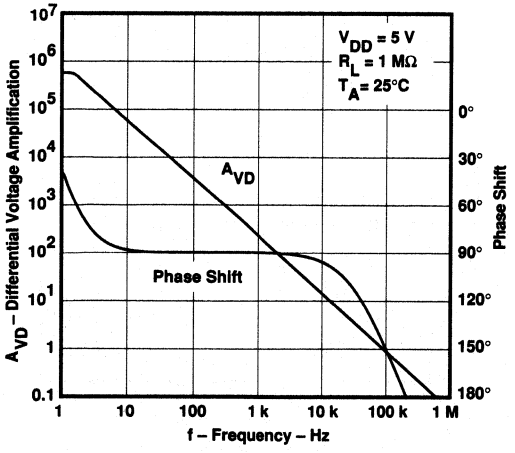


FIGURE 92

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

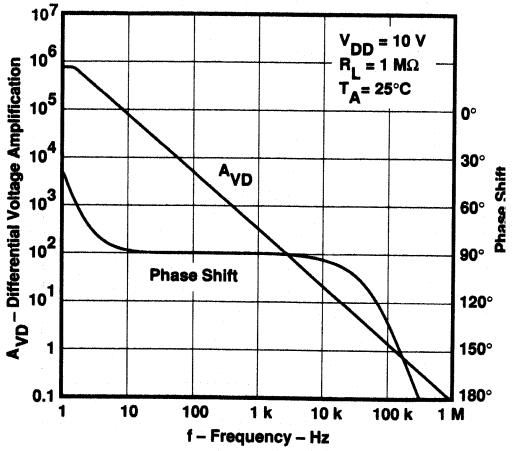


FIGURE 93

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)†

PHASE MARGIN
vs
SUPPLY VOLTAGE

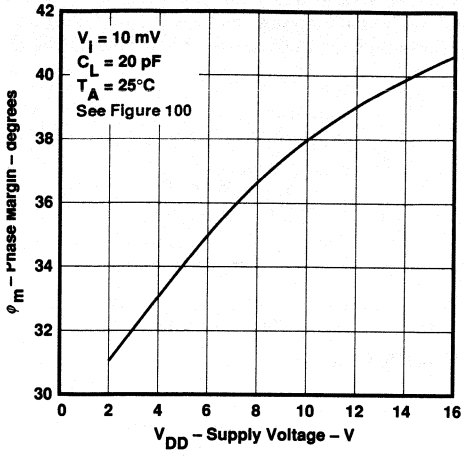


FIGURE 94

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

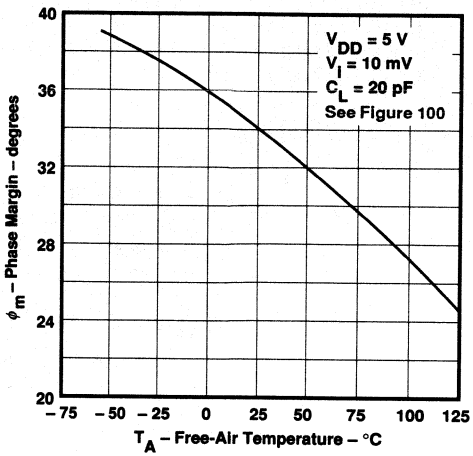


FIGURE 95

PHASE MARGIN
vs
CAPACITIVE LOAD

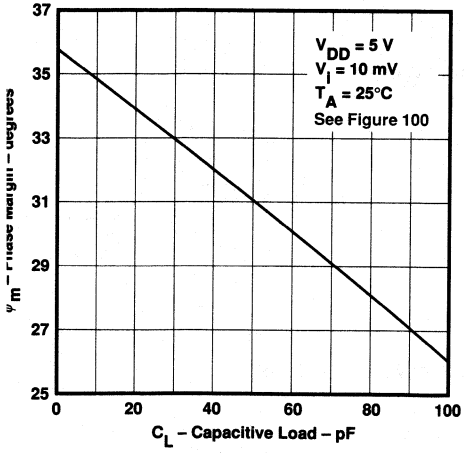


FIGURE 96

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

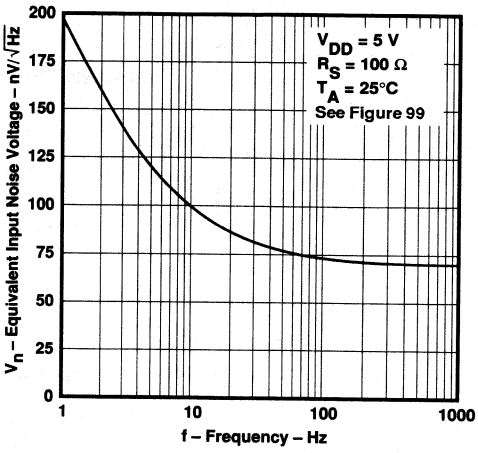


FIGURE 97

ata at high and low temperatures are applicable only within the rated operating free-air temperature ranges of various devices.

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

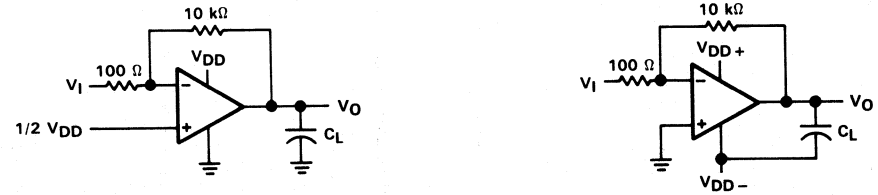
Because the TLC271 is optimized for single-supply operation, circuit configurations used for the variou tests often present some inconvenience since the input signal, in many cases, must be offset from grounc This inconvenience can be avoided by testing the device with split supplies and the output load tied t the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The us of either circuit will give the same result.

(a) Single-Supply (b) Split-Supply

FIGURE 98. UNITY-GAIN AMPLIFIER

(a) Single-Supply (b) Split-Supply

FIGURE 99. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 100. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

ıput bias current

Because of the high input impedance of the TLC271 op amp, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 101). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the ''open-socket'' leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an ''open-socket'' reading is not feasible using this method.

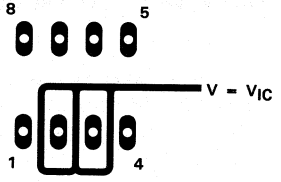


FIGURE 101. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE PACKAGE)

ɔw-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

ıput offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

ıll-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 98. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 102). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

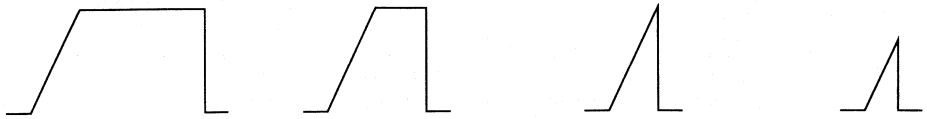


FIGURE 102. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

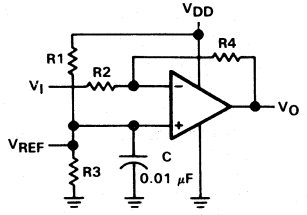
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC271 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 103). The low input bias current consumption of the TLC271 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.



$$V_{REF} = V_{DD} \frac{R3}{R1 + R3}$$

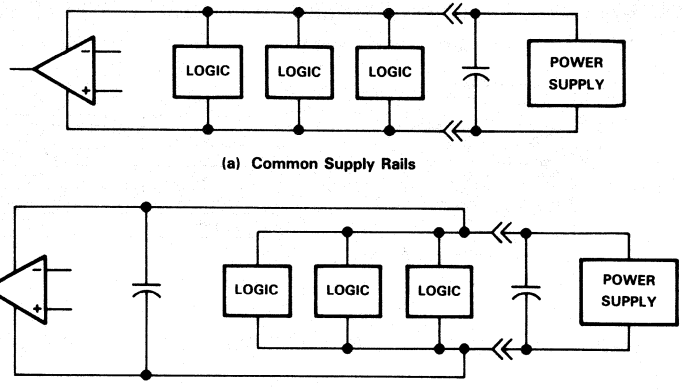
$$V_O = \left(V_{REF} - V_I\right) \frac{R4}{R2} + V_{REF}$$

FIGURE 103. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE

TYPICAL APPLICATION DATA

The TLC271 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 104); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



(a) Common Supply Rails

(b) Separate Bypassed Supply Rails (preferred)

FIGURE 104. COMMON VERSUS SEPARATE SUPPLY RAILS

ɔut offset voltage nulling

The TLC271 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 105. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.

(a) Single-Supply

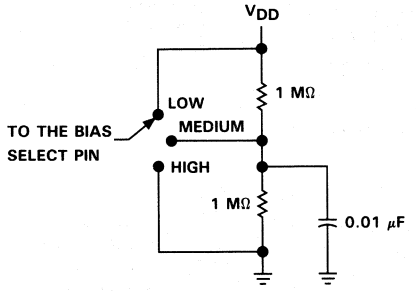
(b) Split-Supply

FIGURE 105. INPUT OFFSET VOLTAGE NULL CIRCUIT

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias select pin to one of the three voltage levels (see Figure 10€ For medium-bias applications, it is recommended that the bias select pin be connected to the mid-poi between the supply rails. This is a simple procedure in split-supply applications, since this point is groun In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicate The use of large-value resistors in the voltage divider will reduce the current drain of the divider from tl supply line. However, large-value resistors used in conjunction with a large-value capacitor will requi significant time to charge up to the supply midpoint after the supply is switched on. A voltage other th the mid-point may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} – 1 V
HIGH	GND

FIGURE 106. BIAS SELECTION FOR SINGLE-SUPPLY APPLICATIONS

input characteristics

The TLC271 is specified with a minimum and a maximum input voltage that, if exceeded at either inpu could cause the device to malfunction. Exceeding this specified range is a common problem, especial in single-supply operation. Note that the lower range limit includes the negative rail, while the upper ran limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.5 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC271 very goo input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage dr in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphor dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gat alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, includi the first month of operation.

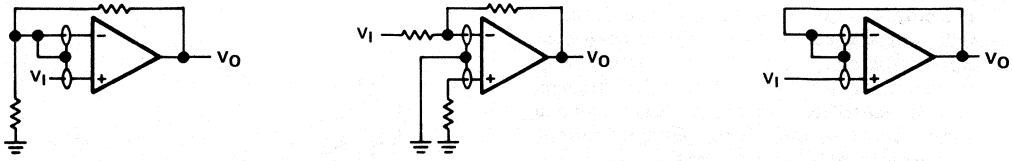
Because of the extremely high input impedance and resulting low bias current requirements, the TLC27 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and socke can easily exceed bias current requirements and cause a degradation in device performance. It is goo practice to include guard rings around inputs (similar to those of Figure 101 in the Parameter Measureme Information section). These guards should be driven from a low-impedance source at the same volta level as the common-mode input (see Figure 107).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

oise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC271 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 107. GUARD RING SCHEMES

eedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 108). The value of this capacitor is optimized empirically.

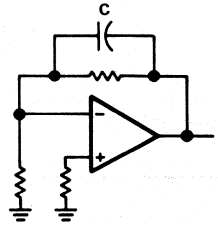


FIGURE 108. COMPENSATION FOR INPUT CAPACITANCE

lectrostatic discharge protection

The TLC271 incorporates an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse biased diode.

atchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC271 inputs and output were designed to withstand −110-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

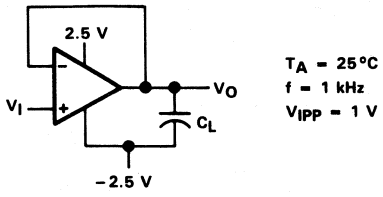
TYPICAL APPLICATION DATA

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

output characteristics

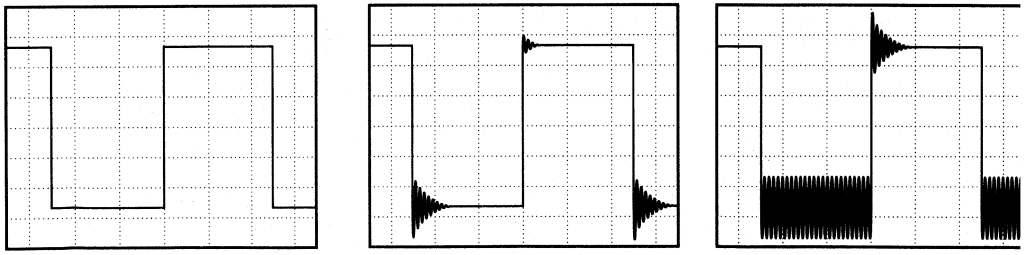
The output stage of the TLC271 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 110, 111, and 112). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



(d) Test Circuit

FIGURE 109. TEST CIRCUIT FOR OUTPUT CHARACTERISTICS



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

FIGURE 110. EFFECT OF CAPACITIVE LOADS IN HIGH-BIAS MODE

TEXAS INSTRUMENTS
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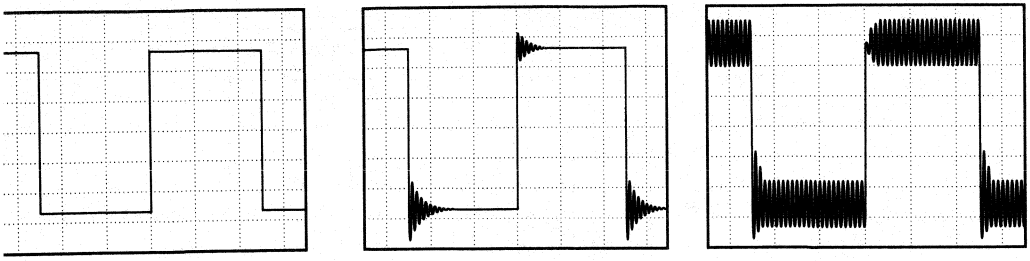
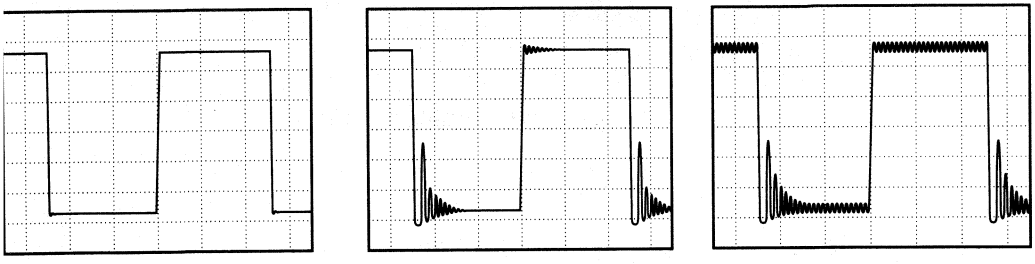
TYPICAL APPLICATION DATA



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

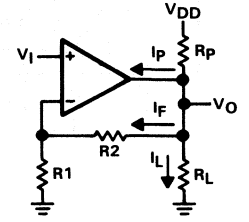
FIGURE 111. EFFECT OF CAPACITIVE LOADS IN MEDIUM-BIAS MODE



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

FIGURE 112. EFFECT OF CAPACITIVE LOADS IN LOW-BIAS MODE

Although the TLC271 possesses excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 113). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

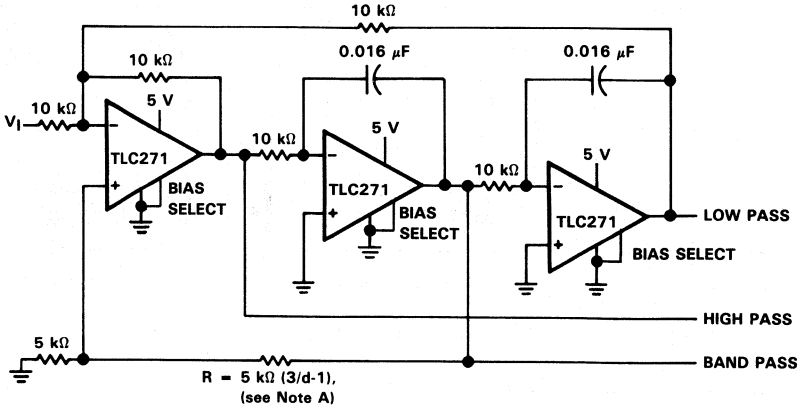


$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

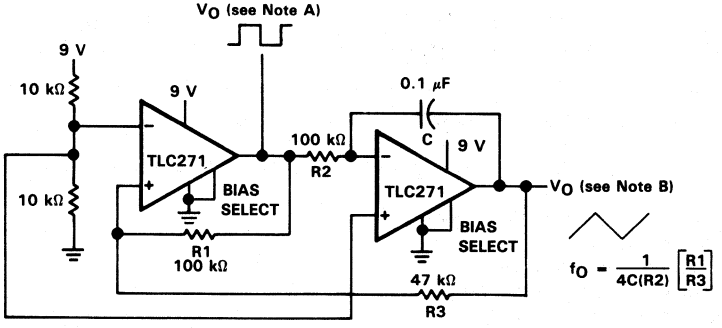
FIGURE 113. RESISTIVE PULLUP TO INCREASE V_{OH}

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_c = 1 kHz

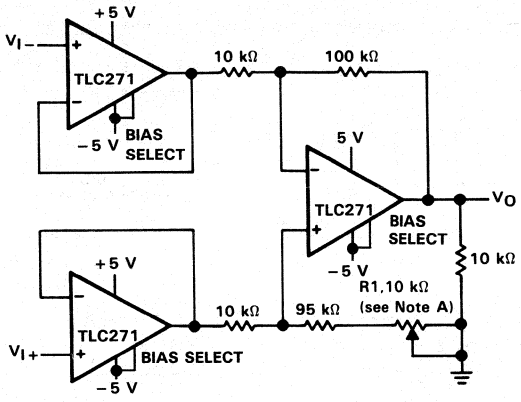
FIGURE 114. STATE VARIABLE FILTER



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 115. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 116. LOW-POWER INSTRUMENTATION AMPLIFIER

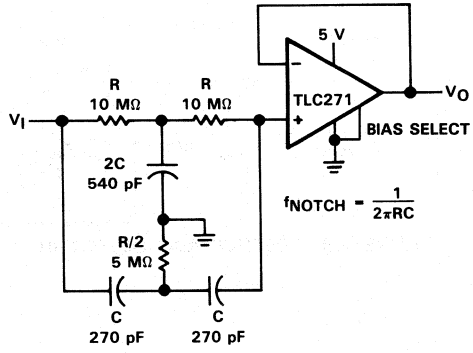
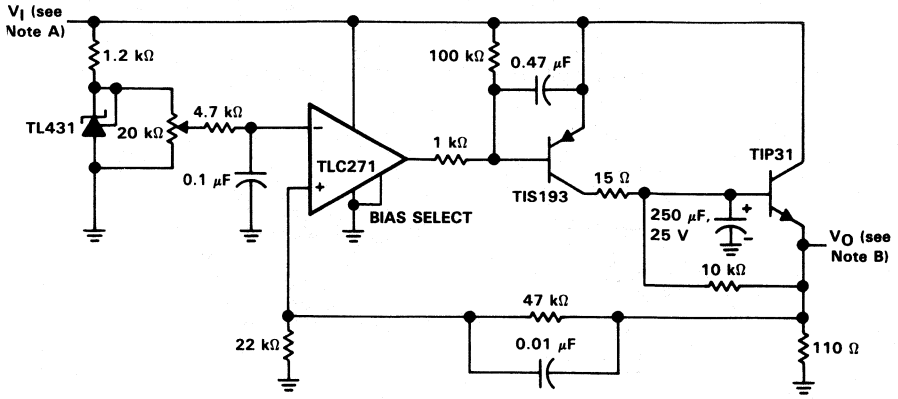


FIGURE 117. SINGLE-SUPPLY TWIN-T NOTCH FILTER

TYPICAL APPLICATION DATA (HIGH-BIAS MODE)



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

FIGURE 118. LOGIC-ARRAY POWER SUPPLY

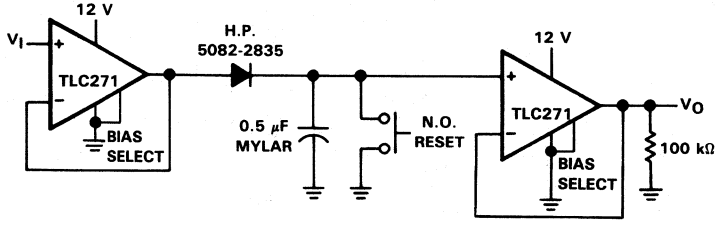
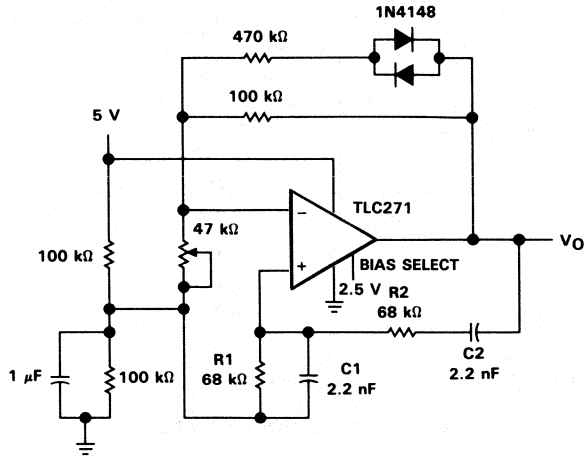


FIGURE 119. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 120. WIEN OSCILLATOR

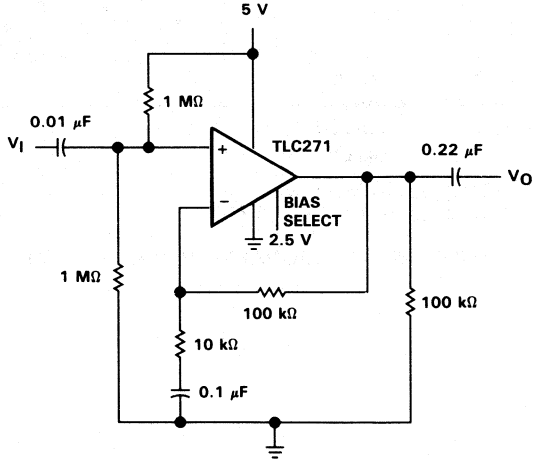
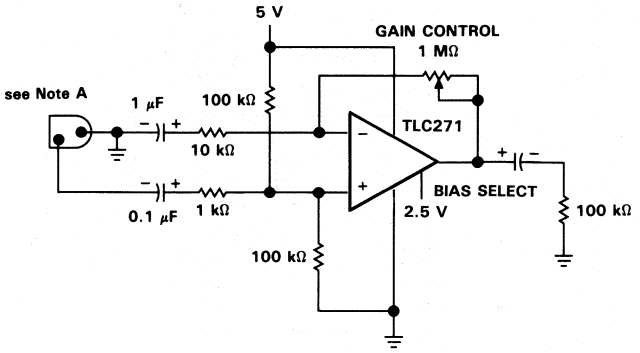


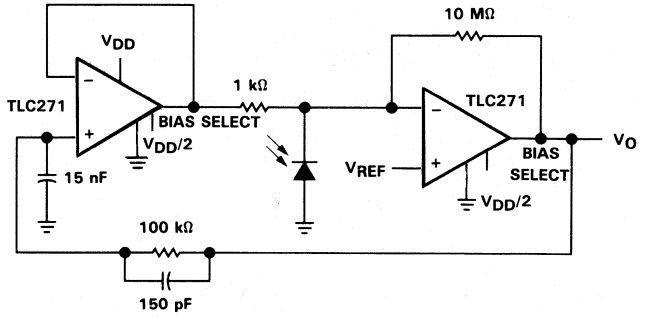
FIGURE 121. SINGLE-SUPPLY AC AMPLIFIER

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)



NOTE A.: Low to medium impedance dynamic mike

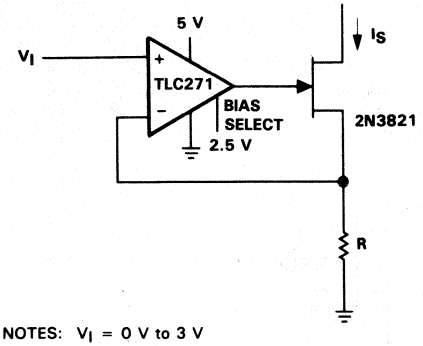
FIGURE 122. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 123. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA (MEDIUM-BIAS MODE)

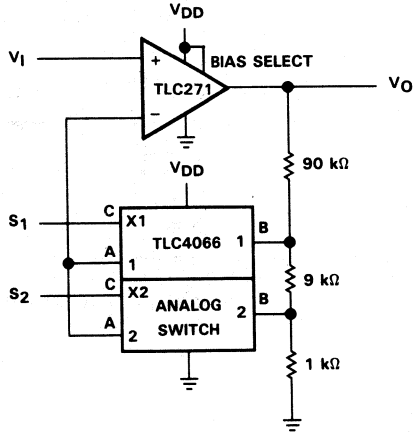


NOTES: V_I = 0 V to 3 V

$$I_S = \frac{V_I}{R}$$

FIGURE 124. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

FIGURE 125. AMPLIFIER WITH DIGITAL GAIN SELECTION

TYPICAL APPLICATION DATA (LOW-BIAS MODE)

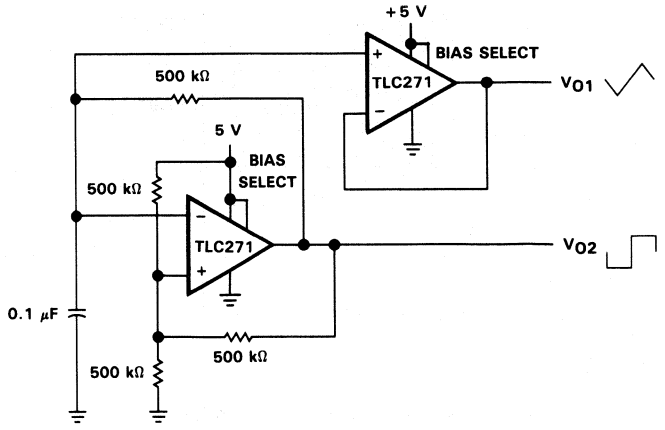
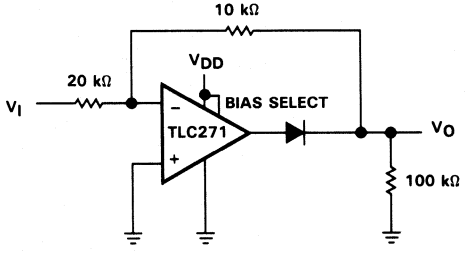


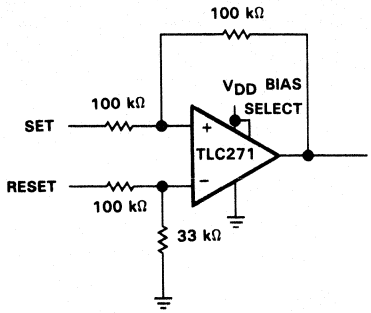
FIGURE 126. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

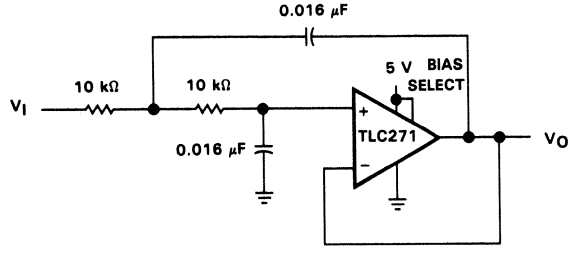
FIGURE 127. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA (LOW-BIAS MODE)



NOTE: V_{DD} = 5 V to 16 V

FIGURE 128. SET/RESET FLIP-FLOP



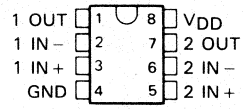
NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 129. TWO-POLE LOW-PASS BUTTERWORTH FILTER

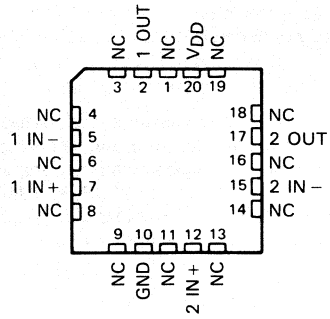
D3138, OCTOBER 1987—REVISED MARCH 1989

- **Trimmed Offset Voltage:**
  TLC277 . . . 500 μV Max at 25 °C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



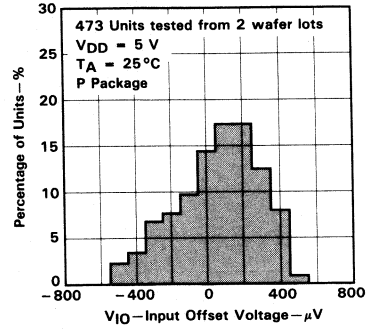
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLC277CD	—	TLC277CJG	TLC277CP
	2 mV	TLC272BCD	—	TLC272BCJG	TLC272BCP
	5 mV	TLC272ACD	—	TLC272ACJG	TLC272ACP
	10 mV	TLC272CD	—	TLC272CJG	TLC272CP
−40°C to 85°C	500 μV	TLC277ID	—	TLC277IJG	TLC277IP
	2 mV	TLC272BID	—	TLC272BIJG	TLC272BIP
	5 mV	TLC272AID	—	TLC272AIJG	TLC272AIP
	10 mV	TLC272ID	—	TLC272IJG	TLC272IP
−55°C to 125°C	500 μV	—	TLC277MFK	TLC277MJG	—
	10 mV	—	TLC272MFK	TLC272MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC277CDR).

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



LinCMOS is a trademark of Texas Instruments Incorporated

description

The TLC272 and TLC277 dual operational amplifiers combine a wide range of input offset voltage grade with low offset voltage drift, high input impedance, low noise, and speeds approaching that of genera purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltag stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effectiv devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offse voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) t the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejectio and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as we as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operationa amplifiers, without the power penalties of bipolar technology. General applications such as transduce interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designe with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making then ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltag range includes the negative rail.

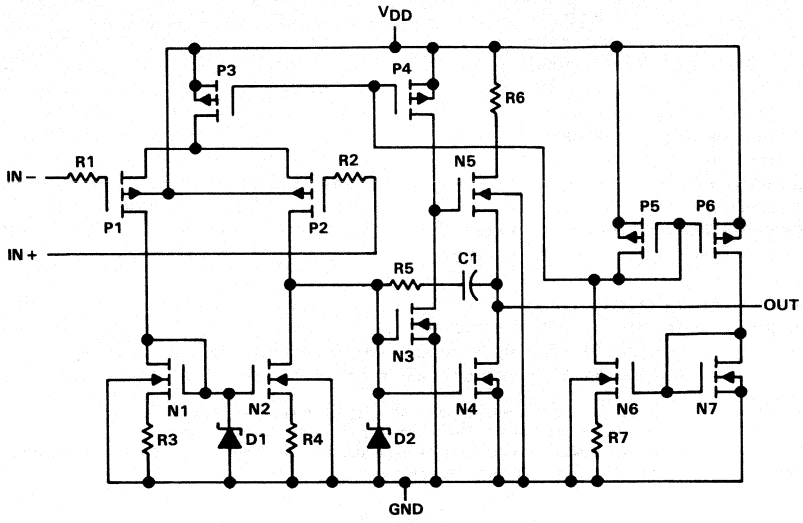
A wide range of packaging options is available, including small-outline and chip carrier versions for high density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustainin latchup.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures a voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercise in handling these devices as exposure to ESD may result in the degradation of the device parametri performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix device are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC277M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		200	500	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−55°C	3	3.8		
					125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−55°C	3.5	35		
					125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−55°C	60	81		
					125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					−55°C		2	5	
					125°C		1	2.2	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC277M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		250	800	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		
					125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		
					125°C	7	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−55°C	60	87		
					125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−55°C		3	6	
					125°C		1.3	2.8	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		230	2000	μV
					Full range			3500	
		TLC277I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		200	500	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					−40°C		1.9	4.4	
					85°C		1.1	2.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC272AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC272BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3500	
		TLC277I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		250	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		
					85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	46		
					85°C	7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		
					85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					−40°C		2.8	5	
					85°C		1.5	3.2	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		230	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		200	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	
					70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		250	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					0°C		2.3	4.4	
					70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

›perating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

›perating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.8		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

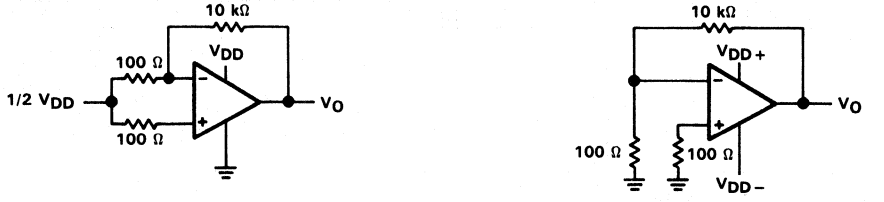
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

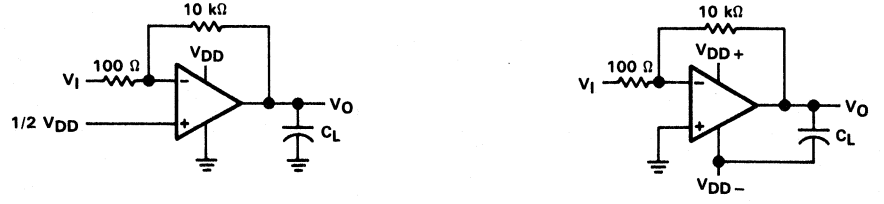
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

ıput bias current

Because of the high input impedance of the TLC272 and TLC277 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

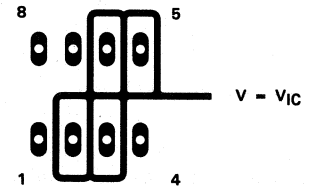


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE-PACKAGE)

ɔw-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

ıput offset voltage temperature coefficient

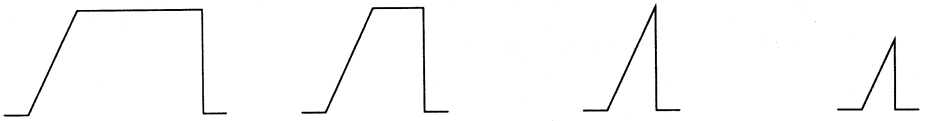
Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing is often specified two ways . . . full-linear response and full-peak response. The full-linear response i generally measured by monitoring the distortion level of the output while increasing the frequency of sinusoidal input signal until the maximum frequency is found above which the output contains significan distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response i specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves th use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude o the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a squar wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak outpu can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determinatio of the point at which the maximum peak-to-peak output is reached.



(a) $f = 1$ kHz (b) $B_{OM} > f > 1$ kHz (c) $f = B_{OM}$ (d) $f > B_{OM}$

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET device and require longer test times than their bipolar and BiFET counterparts. The problem becomes mor pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

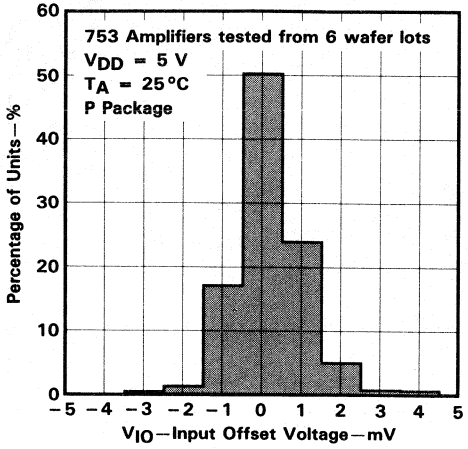


FIGURE 6

DISTRIBUTION OF TLC272
INPUT OFFSET VOLTAGE

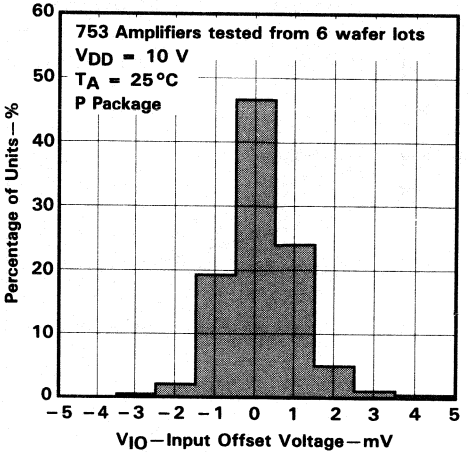


FIGURE 7

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

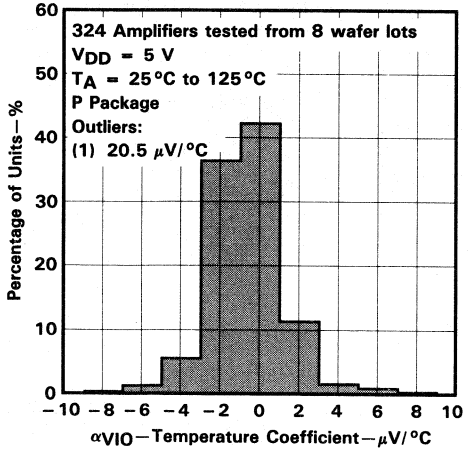


FIGURE 8

DISTRIBUTION OF TLC272 AND TLC277
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

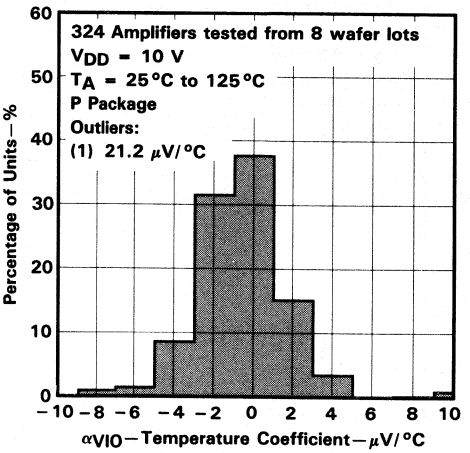


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

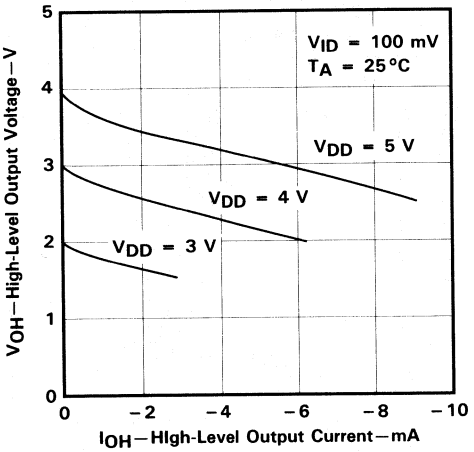


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

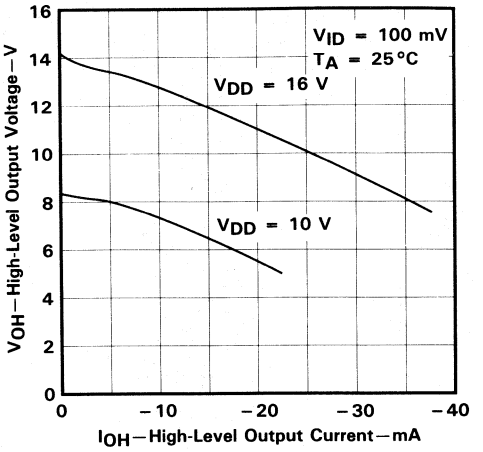


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

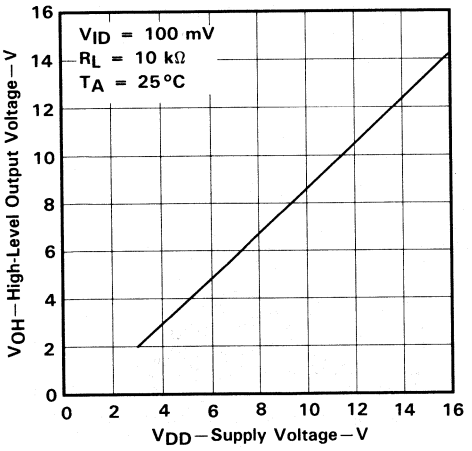


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

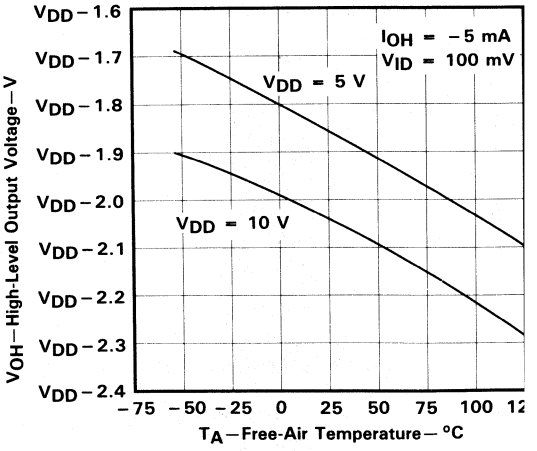


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

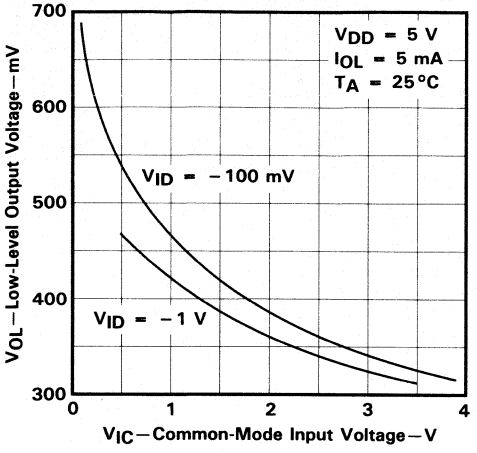


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

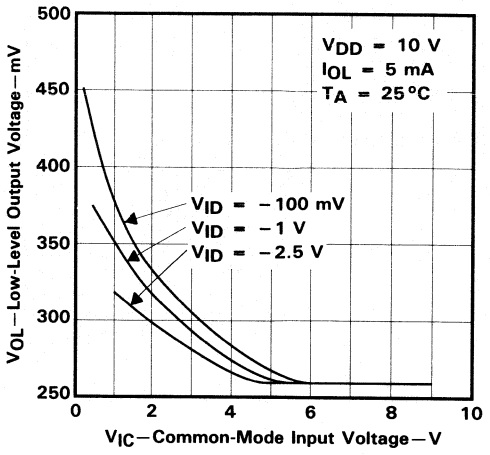


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

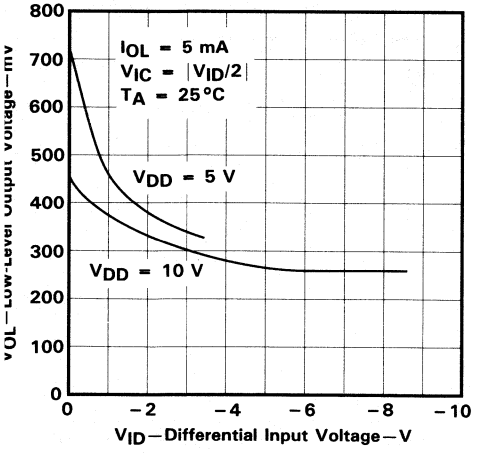


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

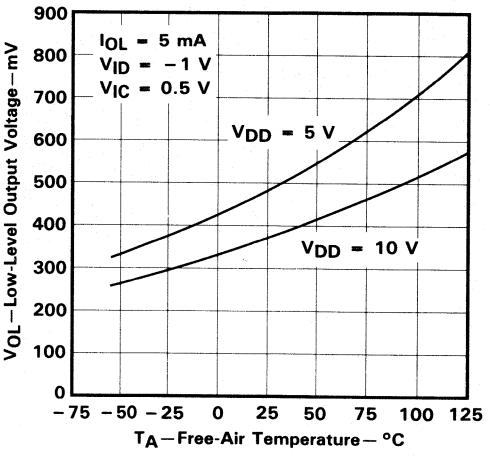


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

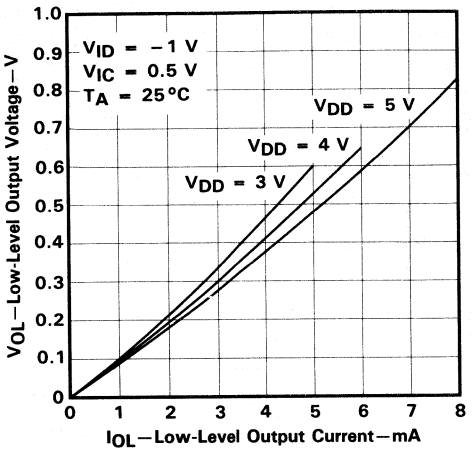


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

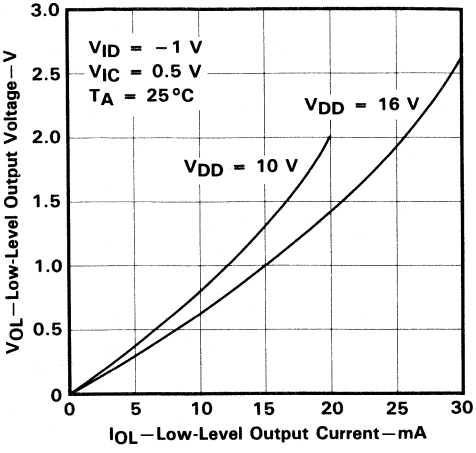


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

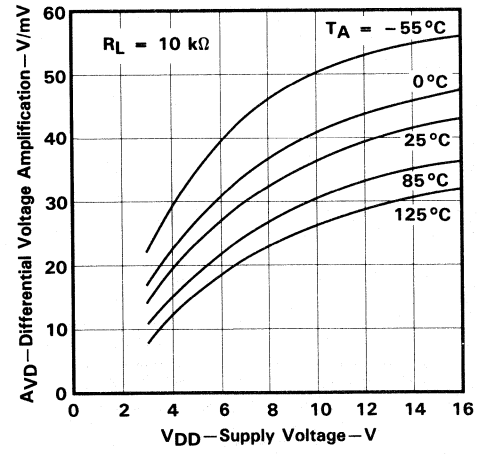


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

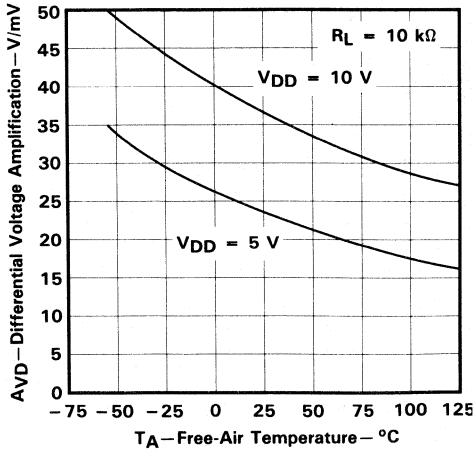


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

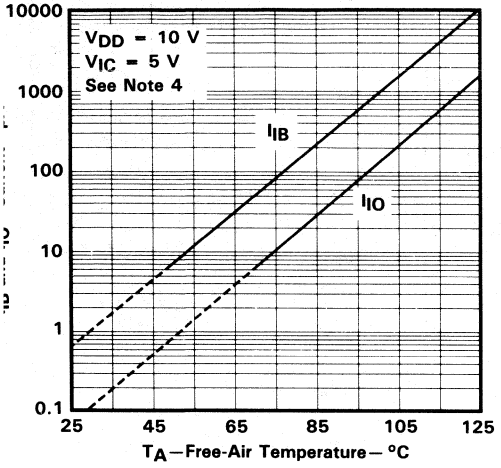


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

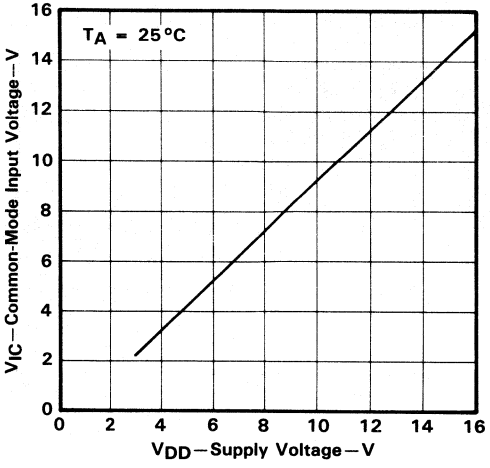


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

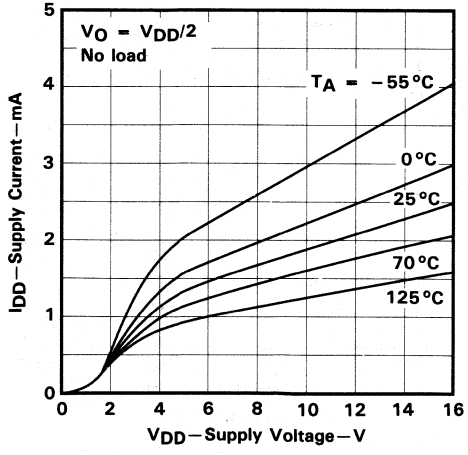


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

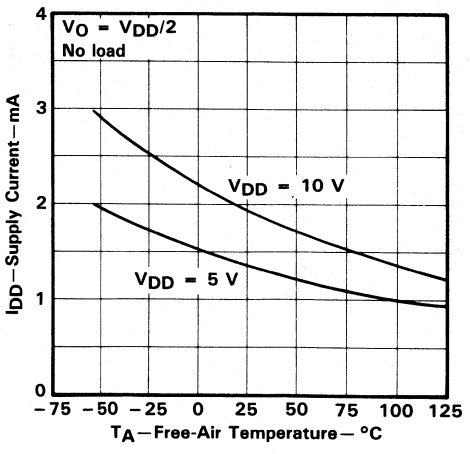


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

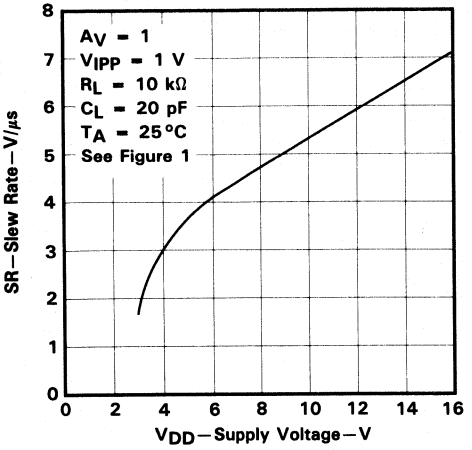


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

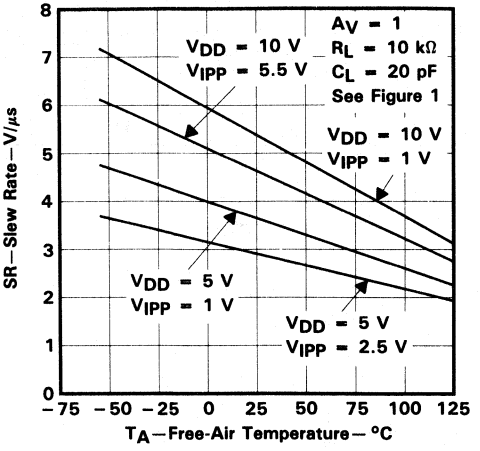


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

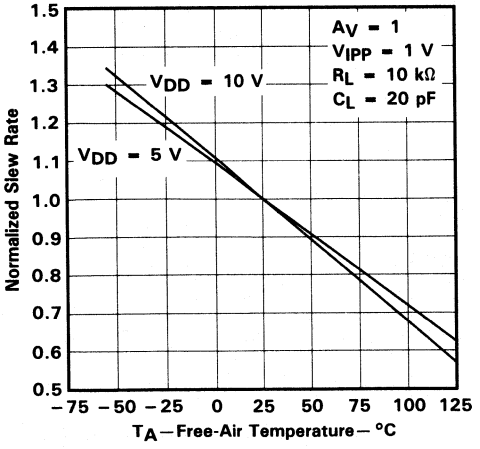


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

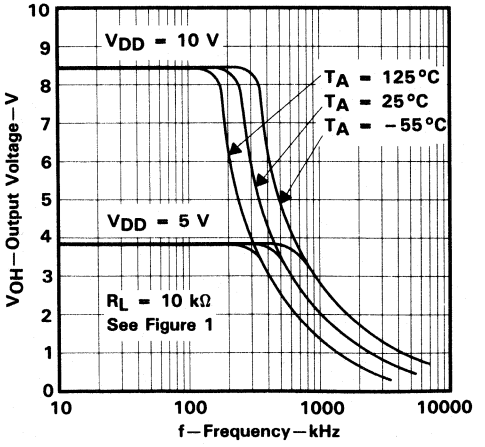


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

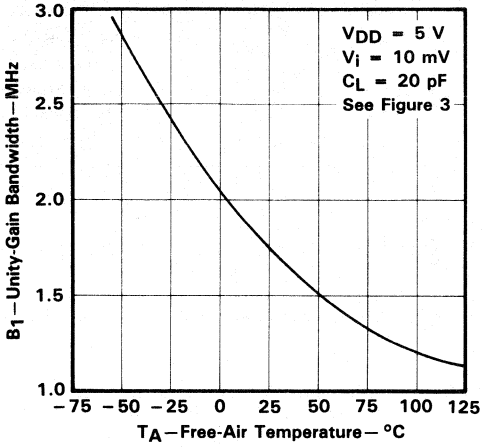


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

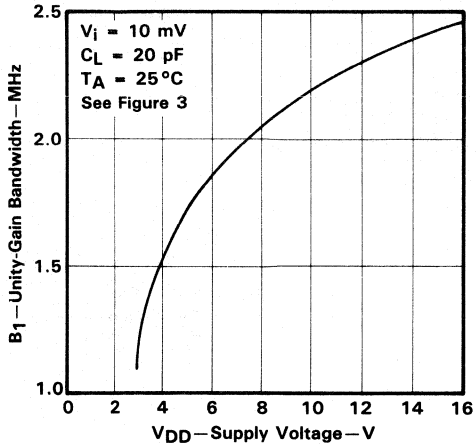


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

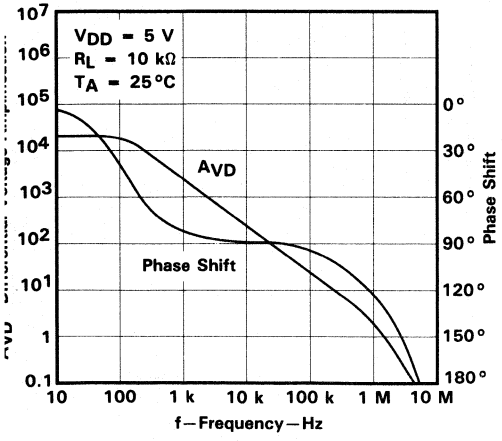


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

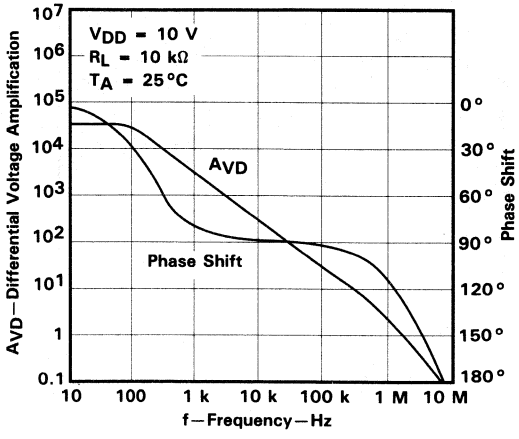


FIGURE 33

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

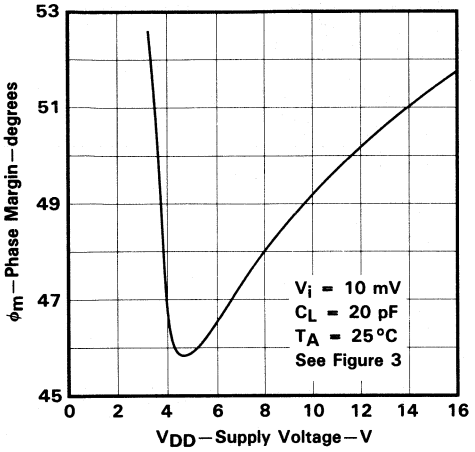


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

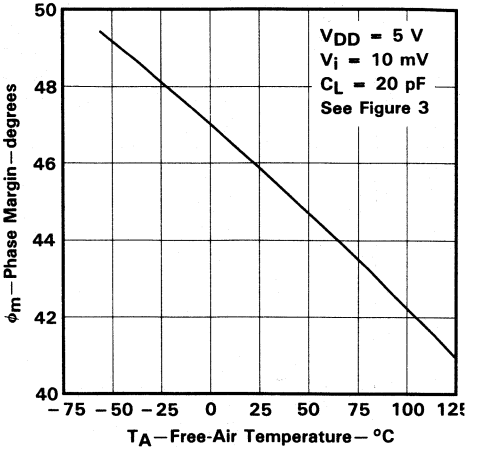


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

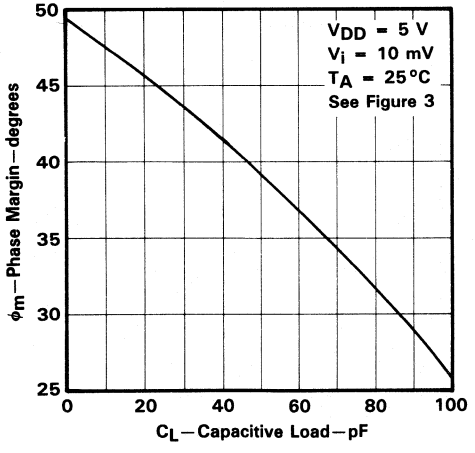


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

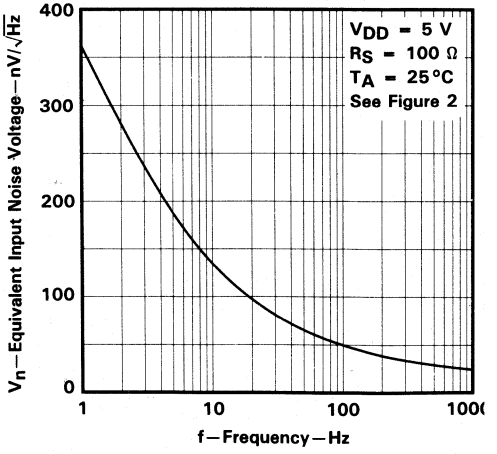


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

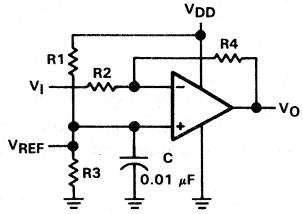
single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

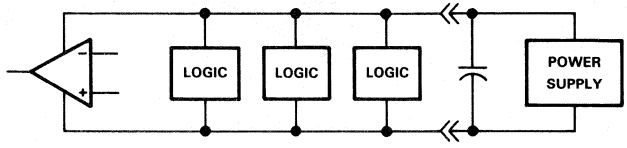
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



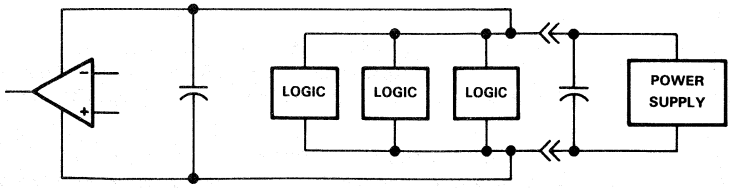
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A = 25°C$ and at $V_{DD}-1.5$ V at all other temperatures.

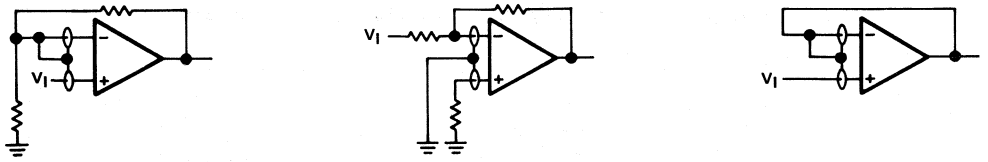
The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

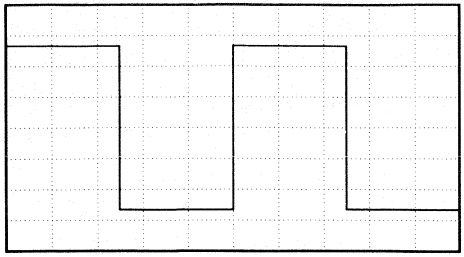
FIGURE 40. GUARD-RING SCHEMES

output characteristics

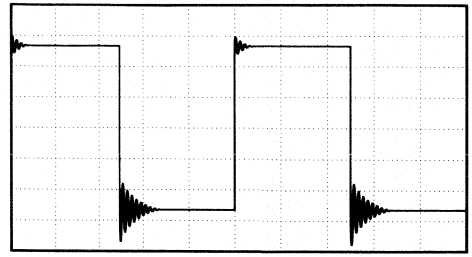
The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

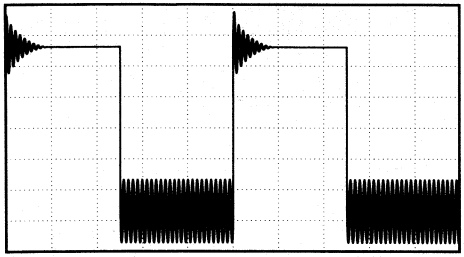
TYPICAL APPLICATION DATA



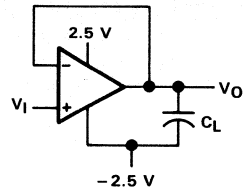
(a) C_L = 20 pF, R_L = No load



(b) C_L = 130 pF, R_L = No load



(c) C_L = 150 pF, R_L = No load



T_A = 25°C
f = 1 kHz
V_{IPP} = 1 V

(d) Test Circuit

FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

eedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA

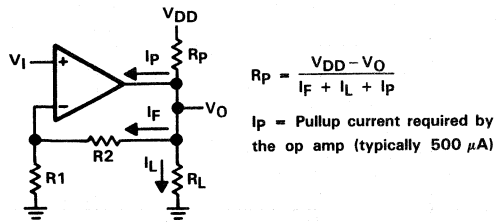


FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

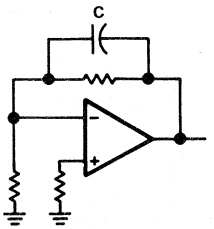


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

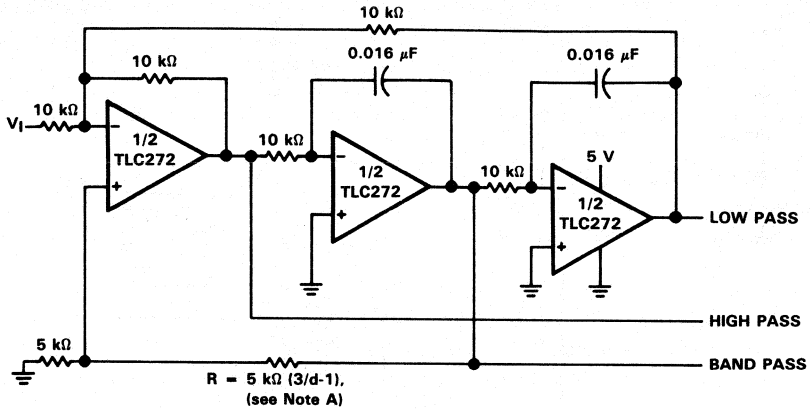
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_c = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

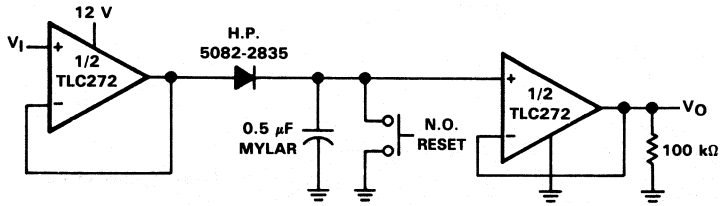
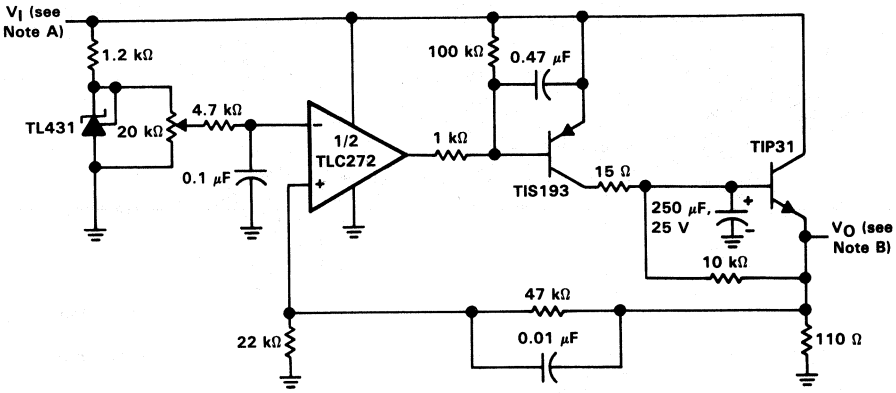


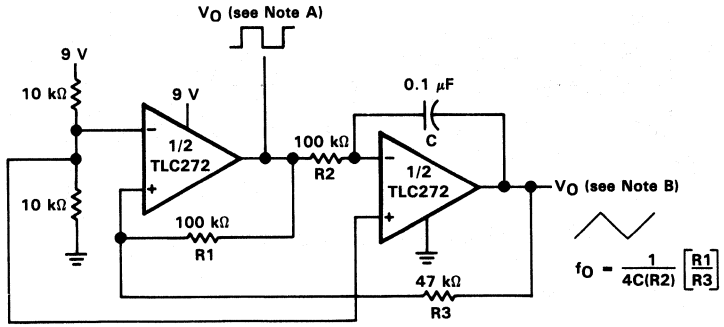
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

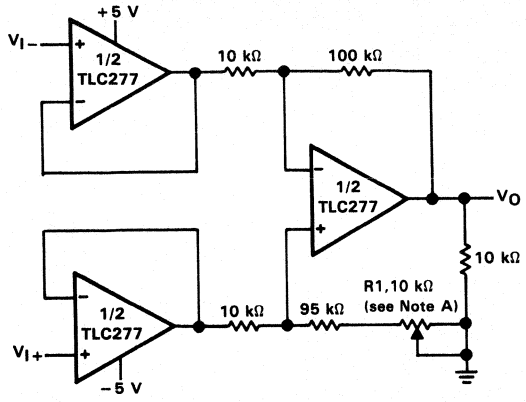
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

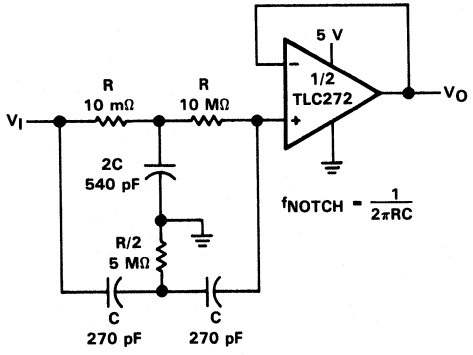
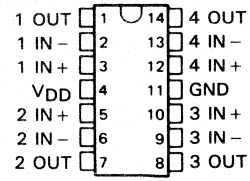


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

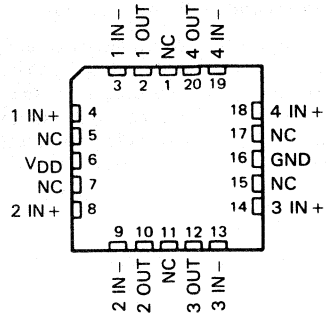
D3141, SEPTEMBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage:**
  TLC279 . . . 900 μV Max at 25 °C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



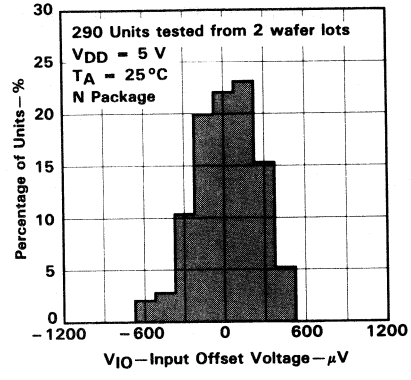
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC279CD	—	TLC279CJ	TLC279CN
	2 mV	TLC274BCD	—	TLC274BCJ	TLC274BCN
	5 mV	TLC274ACD	—	TLC274ACJ	TLC274ACN
	10 mV	TLC274CD	—	TLC274CJ	TLC274CN
−40°C to 85°C	900 μV	TLC279ID	—	TLC279IJ	TLC279IN
	2 mV	TLC274BID	—	TLC274BIJ	TLC274BIN
	5 mV	TLC274AID	—	TLC274AIJ	TLC274AIN
	10 mV	TLC274ID	—	TLC274IJ	TLC274IN
−55°C to 125°C	900 μV	—	TLC279MFK	TLC279MJ	—
	10 mV	—	TLC274MFK	TLC274MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC279CDR).

DISTRIBUTION OF TLC279
INPUT OFFSET VOLTAGE



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description

The TLC274 and TLC279 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching that of general purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC274 (10 mV) to the high-precision TLC279 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC274 and TLC279. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

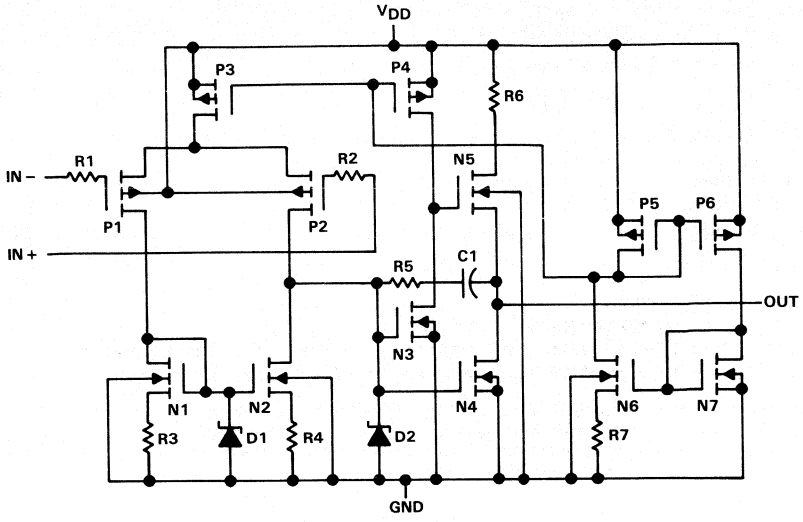
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC274 and TLC279 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±V_{DD}
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC279M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		320	900	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−55°C	3	3.8		
					125°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−55°C	3.5	35		
					125°C	3.5	16		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−55°C	60	81		
					125°C	60	84		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					−55°C		4	10	
					125°C		1.9	4.4	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC279M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		370	1200	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−55°C	7.8	8.5		
					125°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−55°C	7	50		
					125°C	7	27		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−55°C	60	87		
					125°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−55°C	60	90		
					125°C	60	97		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					−55°C		6.0	12	
					125°C		2.5	5.6	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		340	2000	μV
					Full range			3500	
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		320	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					−40°C	3	3.8		
					85°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					−40°C	3.5	32		
					85°C	3.5	19		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					−40°C	60	81		
					85°C	60	86		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					−40°C		3.8	8.8	
					85°C		2.1	4.8	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC274AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			7	
		TLC274BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		390	2000	μV
					Full range			3500	
		TLC279I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		370	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					−40°C	7.8	8.5		
					85°C	7.8	8.5		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					−40°C	7	47		
					85°C	7	31		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					−40°C	60	87		
					85°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					−40°C	60	92		
					85°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					−40°C		5.5	10	
					85°C		2.9	6.4	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC274AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		340	2000	μV
					Full range			3000	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		320	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.8		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		2.7	6.4	mA
					0°C		3.1	7.2	
					70°C		2.3	5.2	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC274C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC274AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC274BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		390	2000	μV
					Full range			3000	
		TLC279C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 10 kΩ	25°C		370	1200	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		3.8	8	mA
					0°C		4.5	8.8	
					70°C		3.2	6.8	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−55°C		4.7		
				125°C		2.3		
			V_{IPP} = 2.5 V	25°C		2.9		
				−55°C		3.7		
				125°C		2		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−55°C		400		
				125°C		230		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−55°C		2.9		
				125°C		1.1		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−55°C		49°		
				125°C		41°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−55°C		7.1		
				125°C		3.1		
			V_{IPP} = 5.5 V	25°C		4.6		
				−55°C		6.1		
				125°C		2.7		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−55°C		280		
				125°C		110		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−55°C		3.4		
				125°C		1.6		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−55°C		52°		
				125°C		44°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				−40°C		4.5		
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				−40°C		3.5		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				−40°C		380		
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				−40°C		2.6		
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				−40°C		49°		
				85°C		43°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				−40°C		6.7		
				85°C		4		
			V_{IPP} = 5.5 V	25°C		4.6		
				−40°C		5.8		
				85°C		3.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				−40°C		260		
				85°C		130		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				−40°C		3.1		
				85°C		1.7		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				−40°C		52°		
				85°C		46°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		3.6		V/μs
				0°C		4		
				70°C		3		
			V_{IPP} = 2.5 V	25°C		2.9		
				0°C		3.1		
				70°C		2.5		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		320		kHz
				0°C		340		
				70°C		260		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		1.7		MHz
				0°C		2		
				70°C		1.3		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		46°		
				0°C		47°		
				70°C		44°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 10 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		5.3		V/μs
				0°C		5.9		
				70°C		4.3		
			V_{IPP} = 5.5 V	25°C		4.6		
				0°C		5.1		
				70°C		3.8		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 10 kΩ,	C_L = 20 pF, See Figure 1	25°C		200		kHz
				0°C		220		
				70°C		140		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		2.2		MHz
				0°C		2.5		
				70°C		1.8		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		49°		
				0°C		50°		
				70°C		46°		

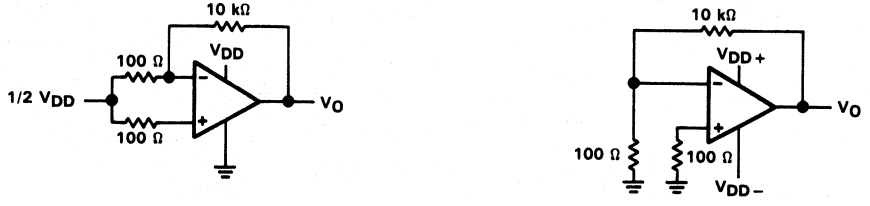
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC274 and TLC279 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

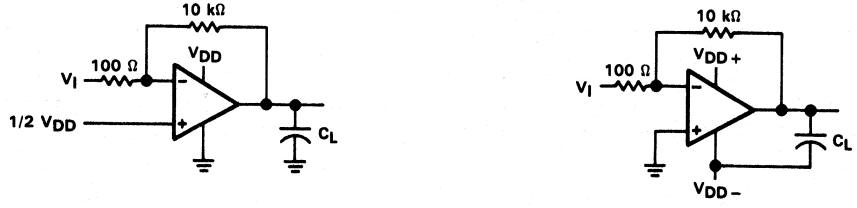
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC274 and TLC279 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

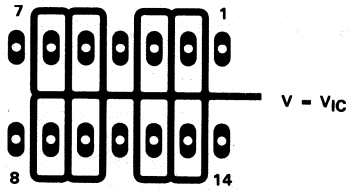


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (J AND N DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

nput offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

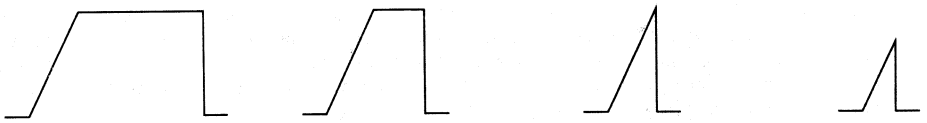


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

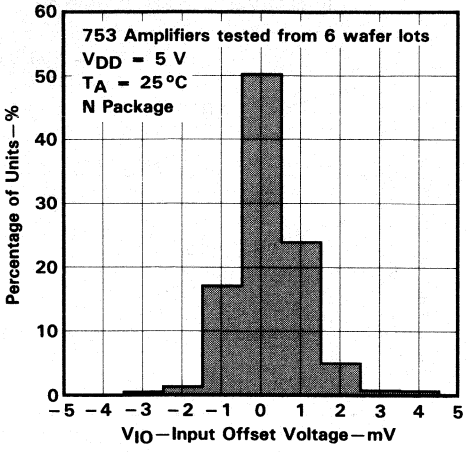


FIGURE 6

DISTRIBUTION OF TLC274
INPUT OFFSET VOLTAGE

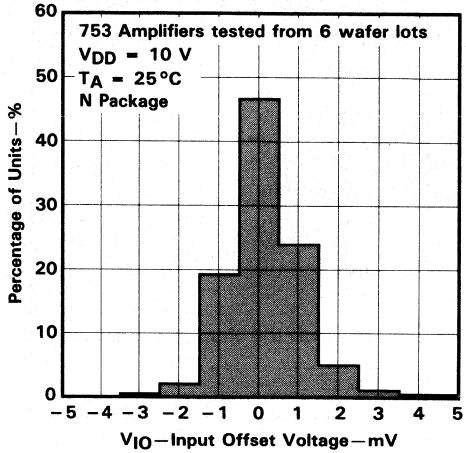


FIGURE 7

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

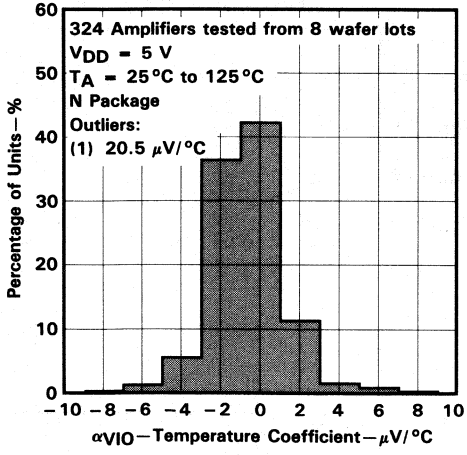


FIGURE 8

DISTRIBUTION OF TLC274 AND TLC279
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

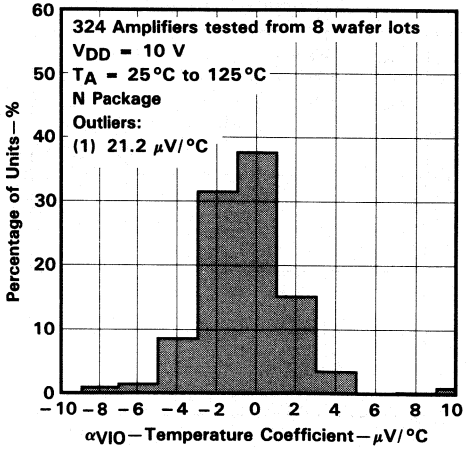


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

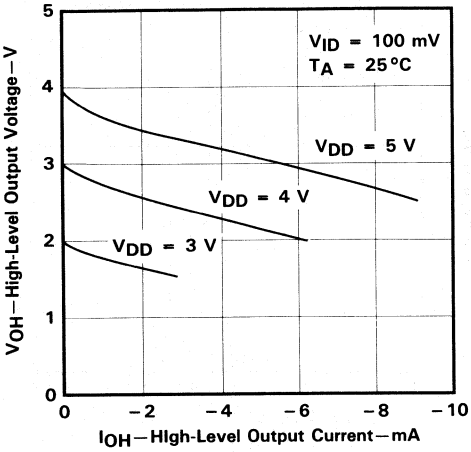


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

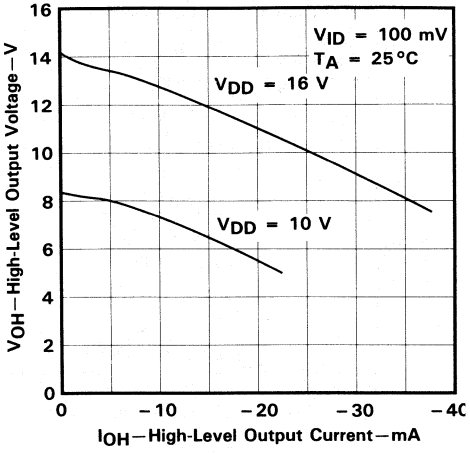


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

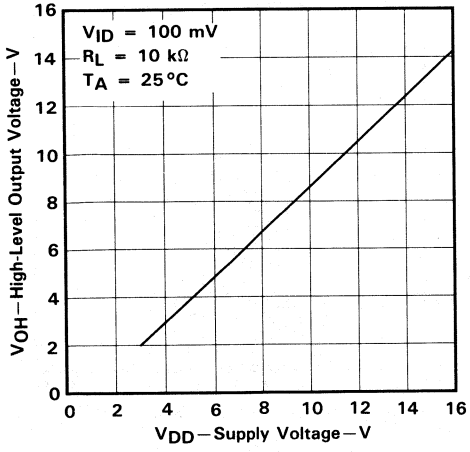


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

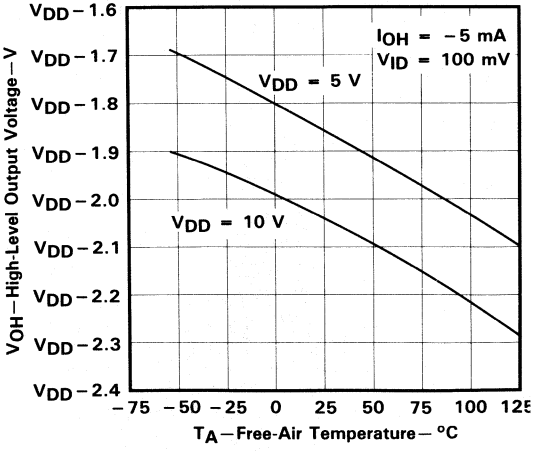


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

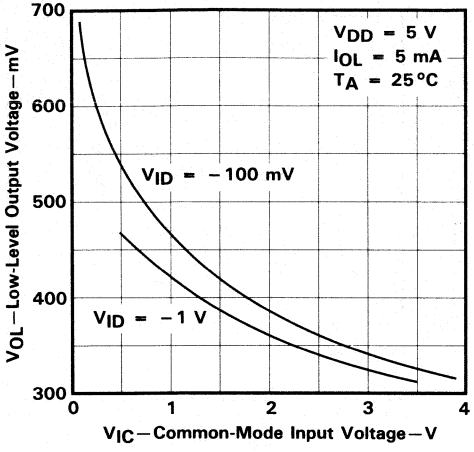


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

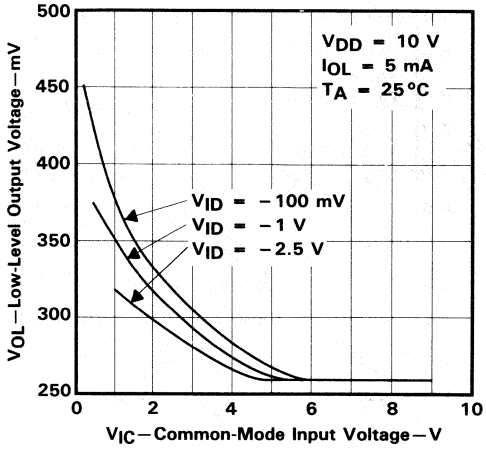


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

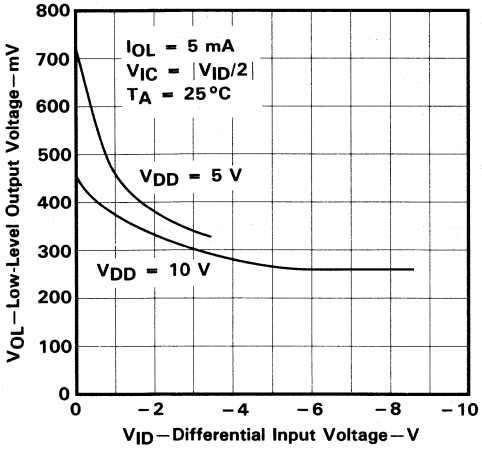


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

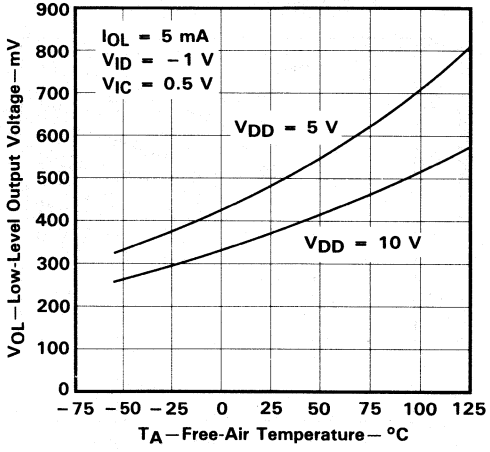


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

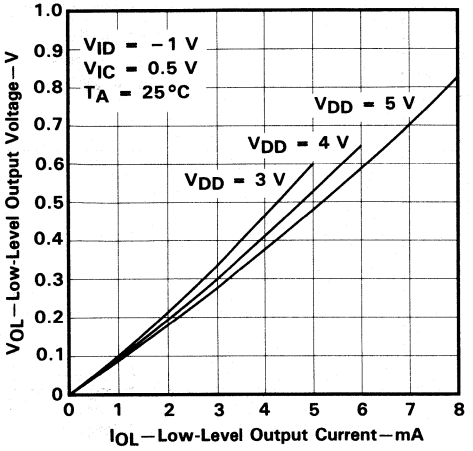


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

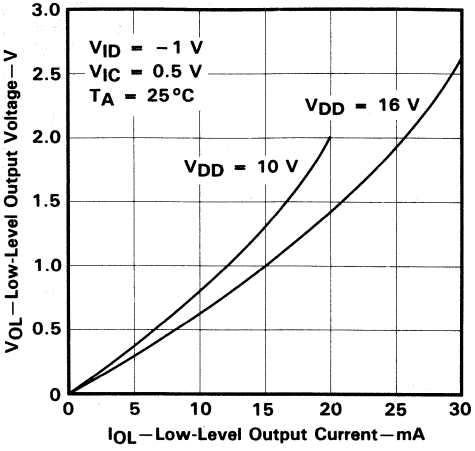


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

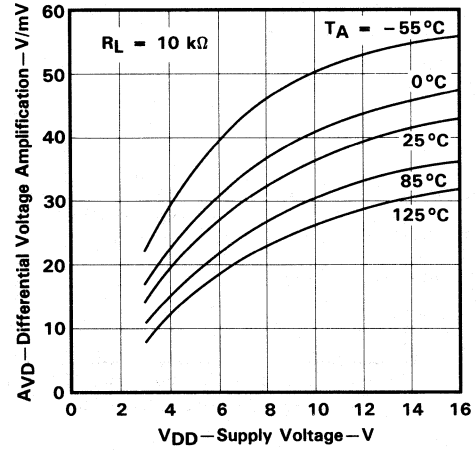


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

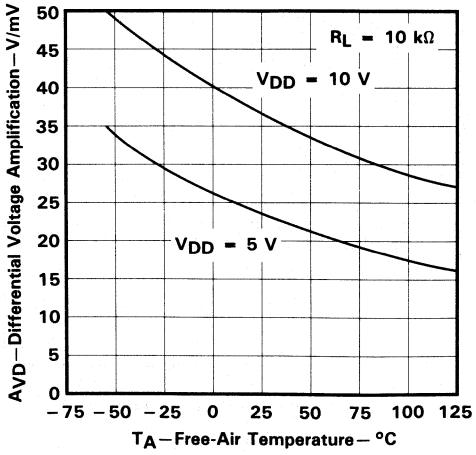


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

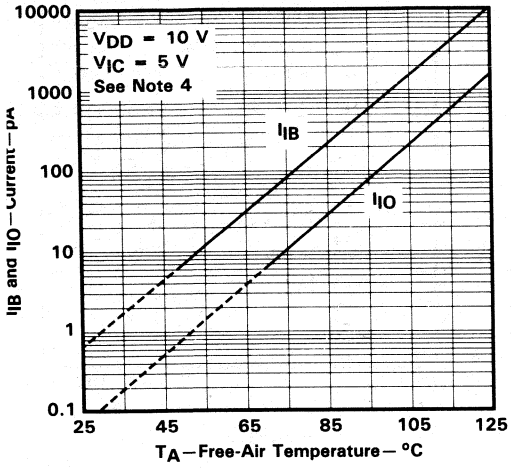


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

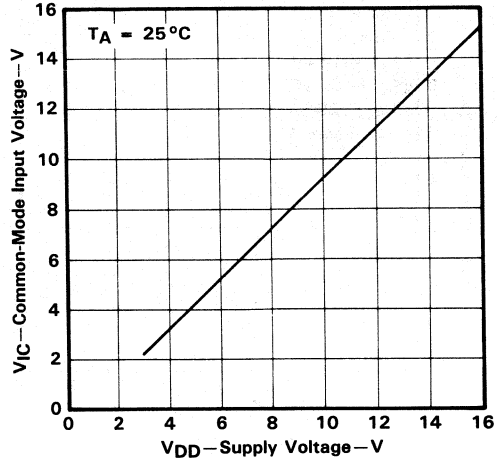


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

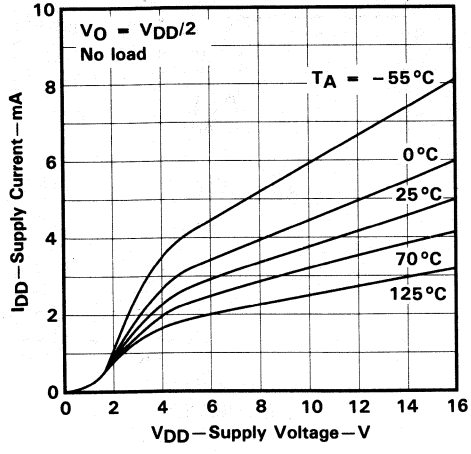


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

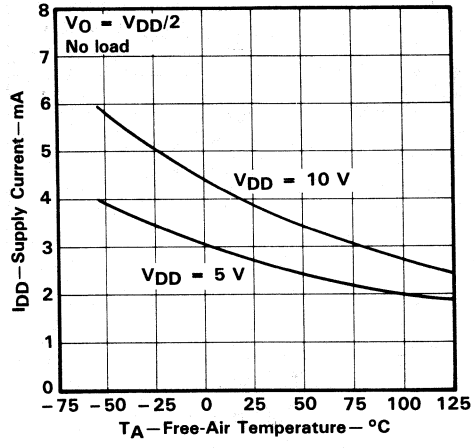


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

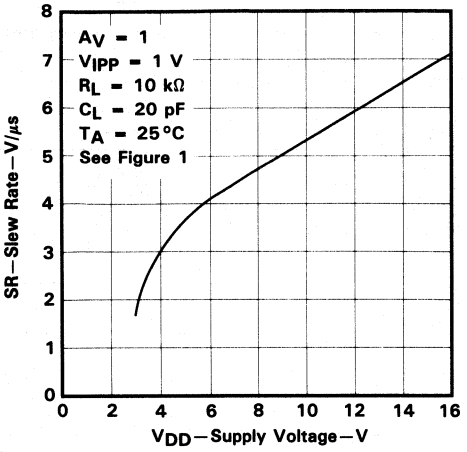


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

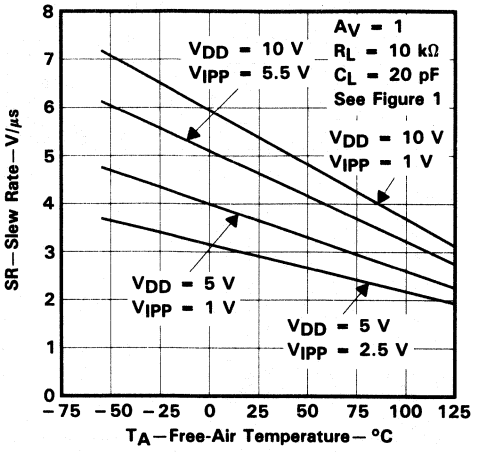


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

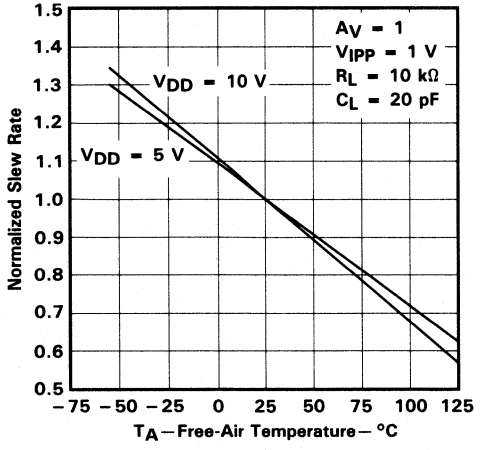


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

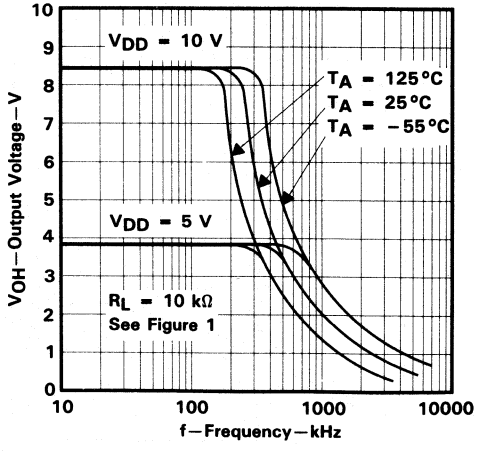


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

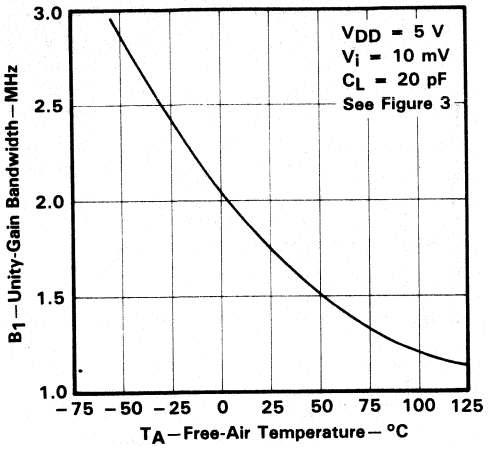


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

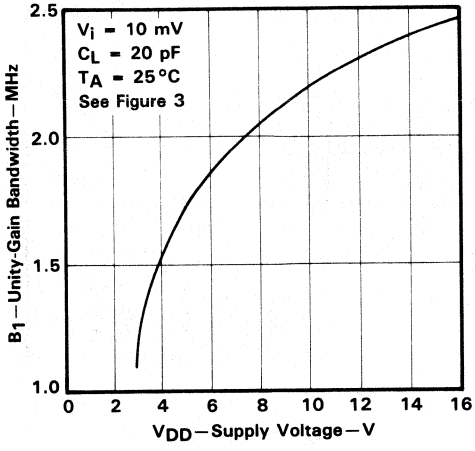


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

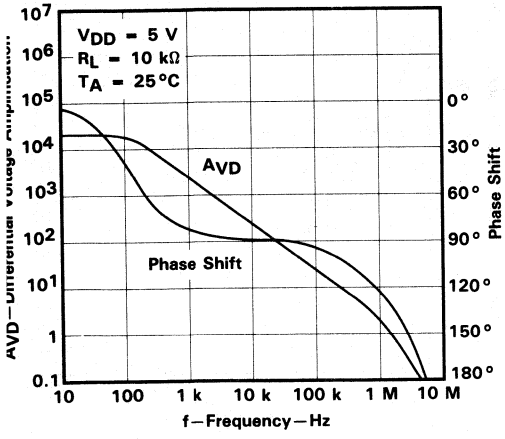


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

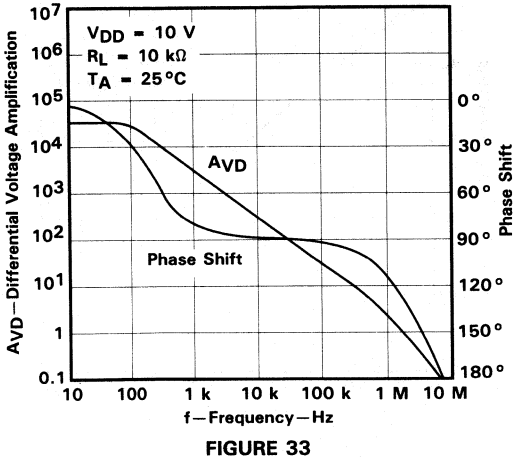


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

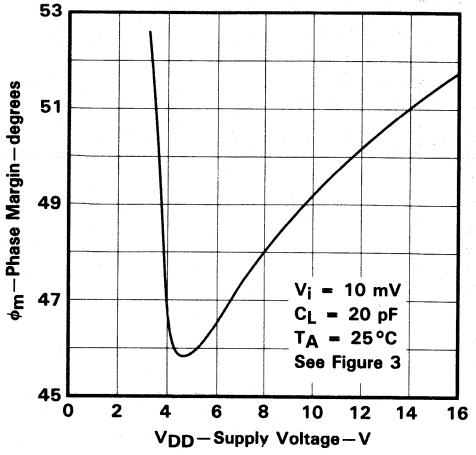


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

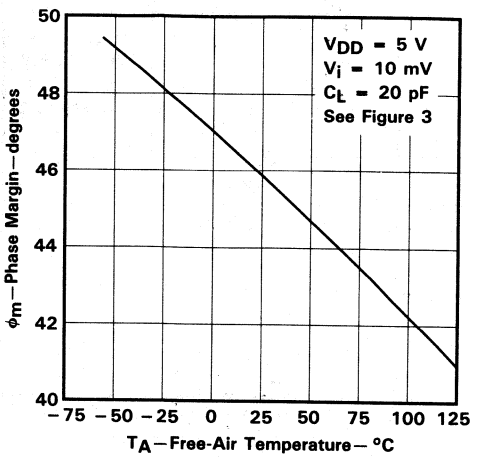


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

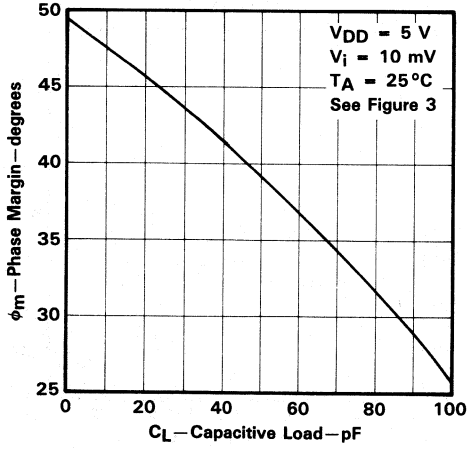


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

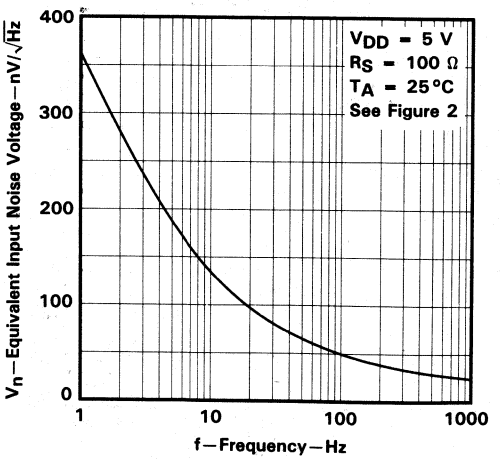


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

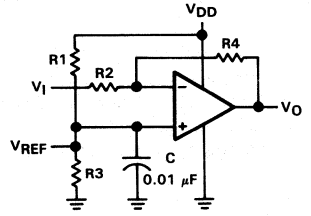
single-supply operation

While the TLC274 and TLC279 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC274 and TLC279 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC274 and TLC279 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

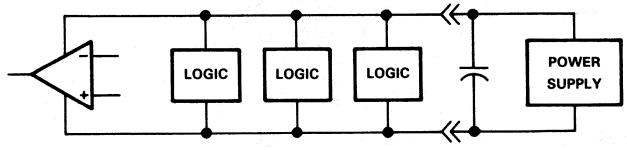
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



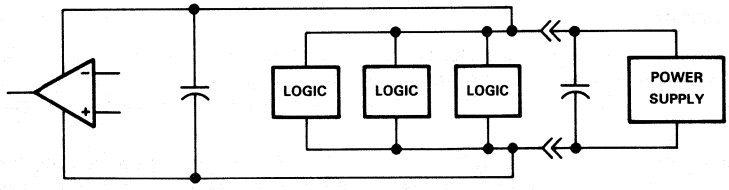
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC274 and TLC279 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A = 25°C$ and at $V_{DD}-1.5$ V at all other temperatures.

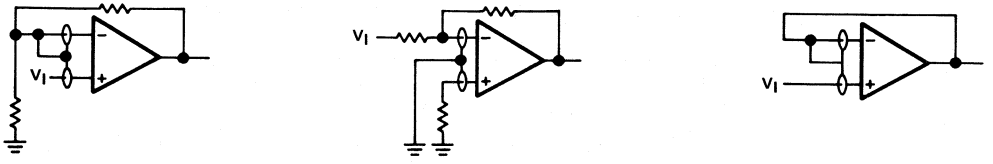
The use of the polysilicon-gate process and the careful input circuit design gives the TLC274 and TLC279 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC274 and TLC279 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC274 and TLC279 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

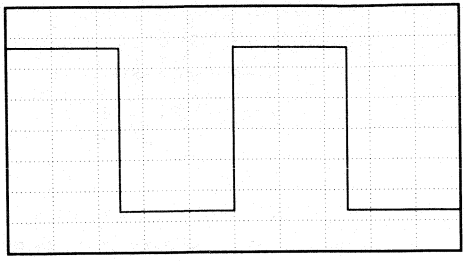
FIGURE 40. GUARD-RING SCHEMES

output characteristics

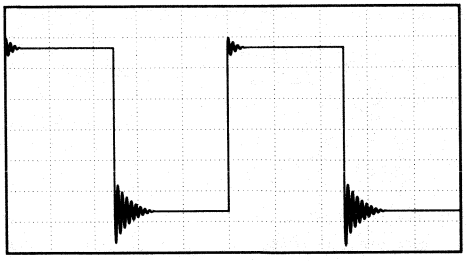
The output stage of the TLC274 and TLC279 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC274 and TLC279 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

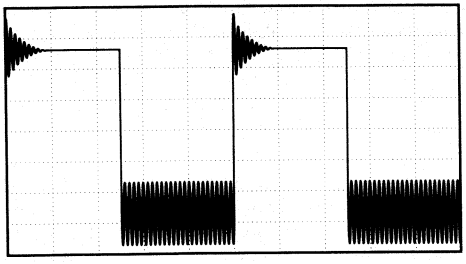
TYPICAL APPLICATION DATA



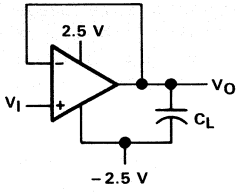
(a) C_L = 20 pF, R_L = No load



(b) C_L = 130 pF, R_L = No load



(c) C_L = 150 pF, R_L = No load



T_A = 25°C
f = 1 kHz
V_{IPP} = 1 V

(d) Test Circuit

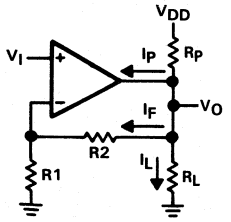
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC274 and TLC279 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

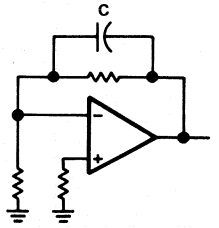


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC274 and TLC279 incorporate an internal electrostatic discharge (ESD) protection circuit tha prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2 Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias current to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC274 and TLC279 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Interna protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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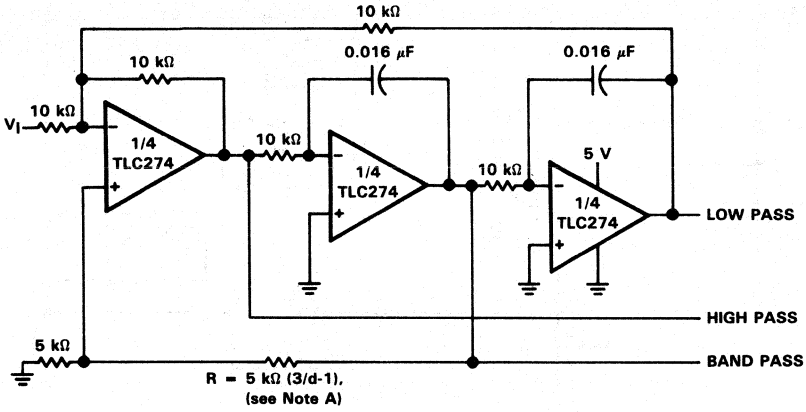
TYPICAL APPLICATION DATA



NOTES: A. d = damping factor, 1/Q
B. Normalized to 10 kΩ and f_C = 1 kHz

FIGURE 44. STATE VARIABLE FILTER

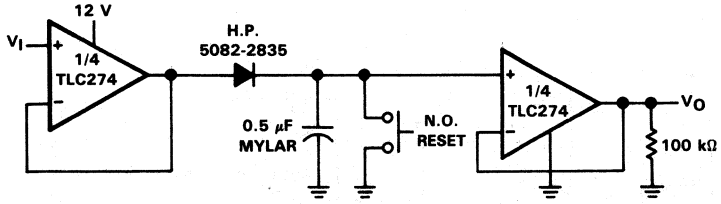
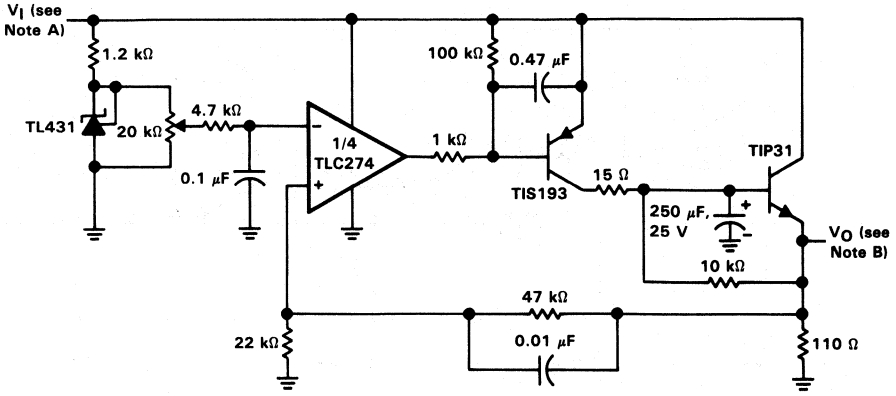


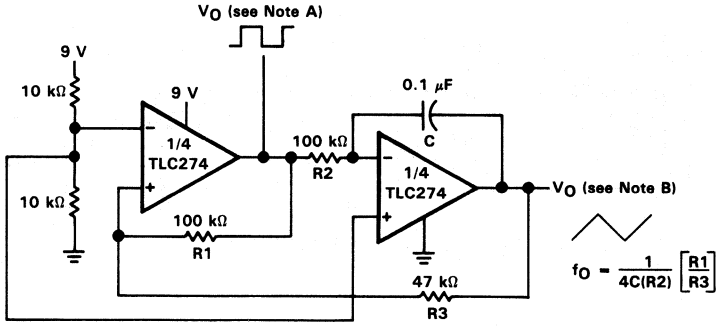
FIGURE 45. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA



NOTES: A. V_I = 3.5 to 15 V
B. V_O = 2.0 V, 0 to 1 A

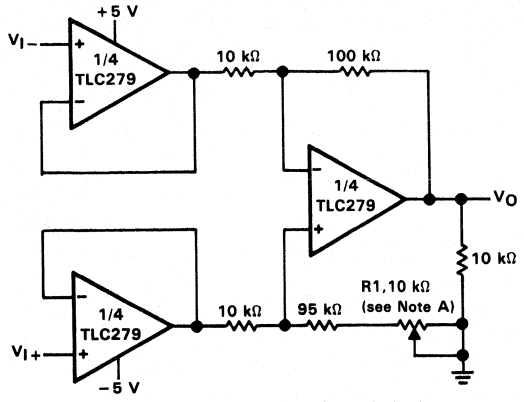
FIGURE 46. LOGIC ARRAY POWER SUPPLY



NOTES: A. V_{OPP} = 8 V
B. V_{OPP} = 4 V

FIGURE 47. SINGLE-SUPPLY FUNCTION GENERATOR

TYPICAL APPLICATION DATA



NOTE A: CMRR adjustment (must be noninductive).

FIGURE 48. LOW-POWER INSTRUMENTATION AMPLIFIER

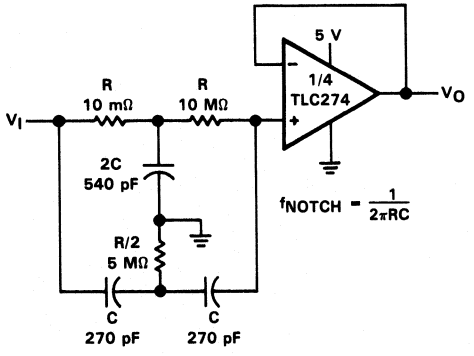
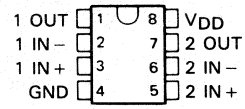


FIGURE 49. SINGLE-SUPPLY TWIN-T NOTCH FILTER

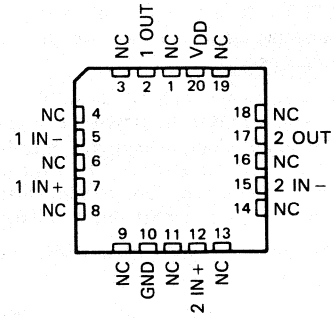
D3139, OCTOBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage: TLC27L7 . . . 500 μV Max at 25°C, V_{DD} = 5 V**
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range: −55°C to 125°C . . . 4 V to 16 V −40°C to 85°C . . . 4 V to 16 V 0°C to 70°C . . . 3 V to 16 V**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultralow Power . . . Typically 95 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



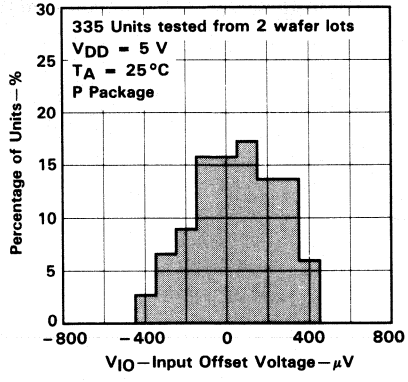
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	500 μV	TLC27L7CD	—	TLC27L7CJG	TLC27L7CP
	2 mV	TLC27L2BCD	—	TLC27L2BCJG	TLC27L2BCP
	5 mV	TLC27L2ACD	—	TLC27L2ACJG	TLC27L2ACP
	10 mV	TLC27L2CD	—	TLC27L2CJG	TLC27L2CP
−40°C to 85°C	500 μV	TLC27L7ID	—	TLC27L7IJG	TLC27L7IP
	2 mV	TLC27L2BID	—	TLC27L2BIJG	TLC27L2BIP
	5 mV	TLC27L2AID	—	TLC27L2AIJG	TLC27L2AIP
	10 mV	TLC27L2ID	—	TLC27L2IJG	TLC27L2IP
−55°C to 125°C	500 μV	—	TLC27L7MFK	TLC27L7MJG	—
	10 mV	—	TLC27L2MFK	TLC27L2MJG	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC27L7CDR).

DISTRIBUTION OF TLC27L7
INPUT OFFSET VOLTAGE



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description

The TLC27L2 and TLC27L7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L2 (10 mV) to the high-precision TLC27L7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L2 and TLC27L7. The devices also exhibit low voltage single-supply operation and ultra-low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27L2 and TLC27L7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

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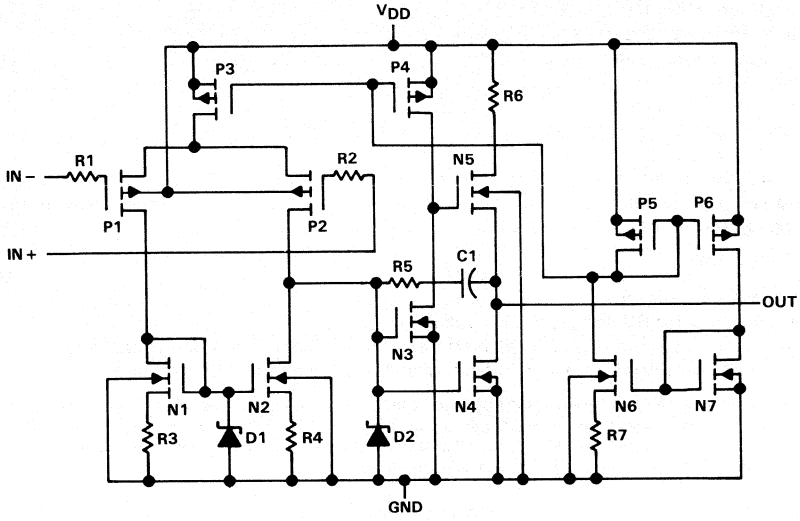
quivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±V_{DD}
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		170	500	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	500		V/mV
					−55°C	25	1000		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					−55°C		35	60	
					125°C		14	24	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		190	800	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					−55°C		56	96	
					125°C		18	30	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

TEXAS INSTRUMENTS
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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		190	800	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					−40°C		49	86	
					85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	mV
					Full range			7	
		TLC27L2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3500	
		TLC27L7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		190	800	μV
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					−40°C		49	86	
					85°C		20	36	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		204	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		170	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	500		V/mV
					0°C	50	700		
					70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		20	34	μA
					0°C		24	42	
					70°C		16	28	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		235	2000	μV
					Full range			3000	
		TLC27L7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		8	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	860		V/mV
					0°C	50	1025		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		29	46	μA
					0°C		36	66	
					70°C		22	40	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

perating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

perating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		29°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

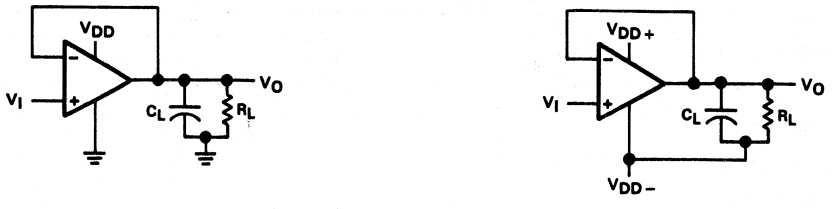
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

PARAMETER MEASUREMENT INFORMATION

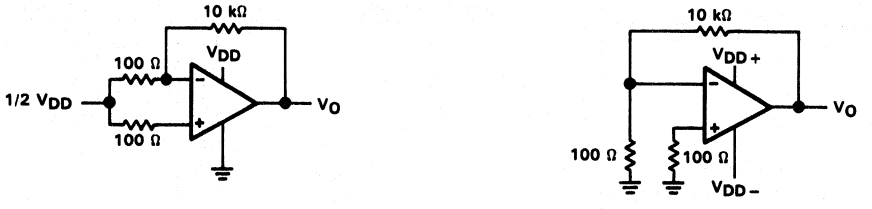
single-supply versus split-supply test circuits

Because the TLC27L2 and TLC27L7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



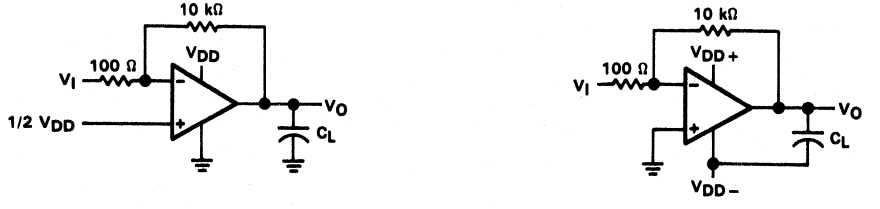
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC27L2 and TLC27L7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

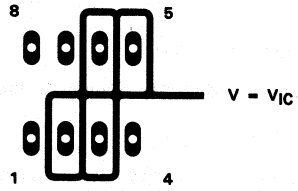


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

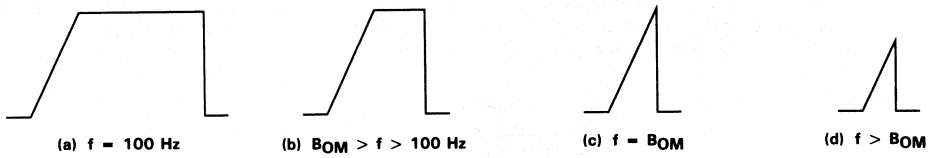


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

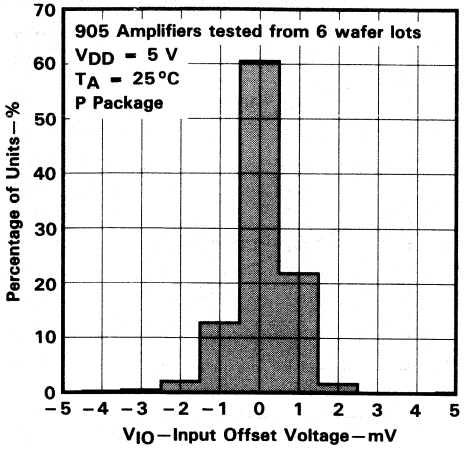


FIGURE 6

DISTRIBUTION OF TLC27L2
INPUT OFFSET VOLTAGE

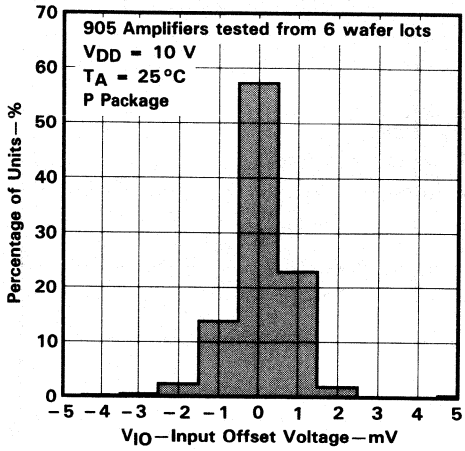


FIGURE 7

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

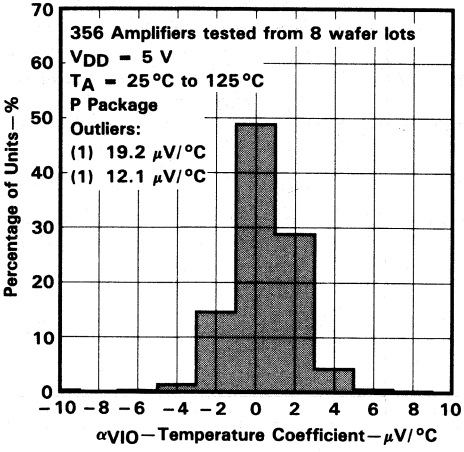


FIGURE 8

DISTRIBUTION OF TLC27L2 AND TLC27L7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

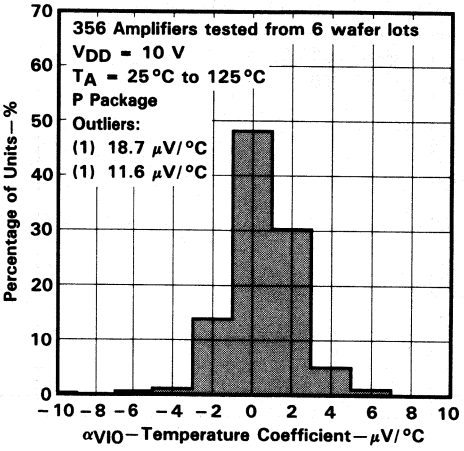


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

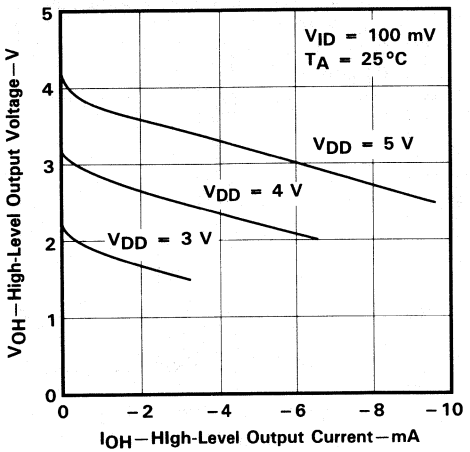


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

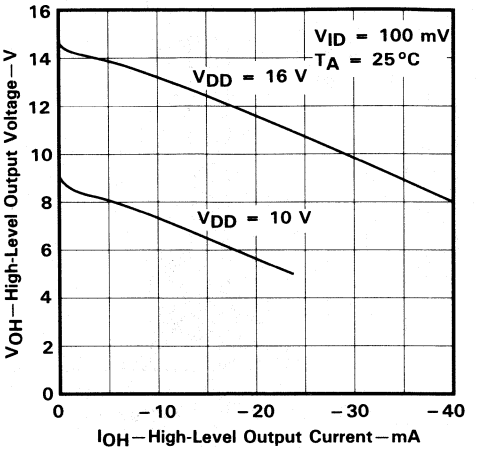


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

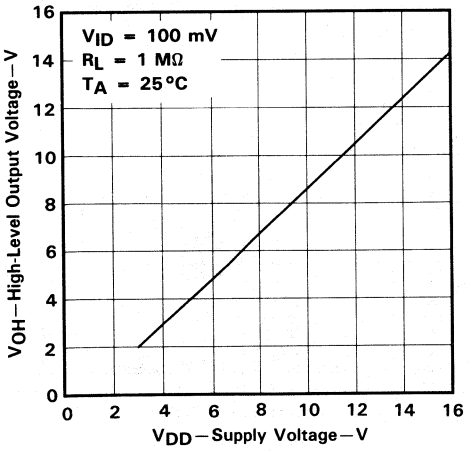


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

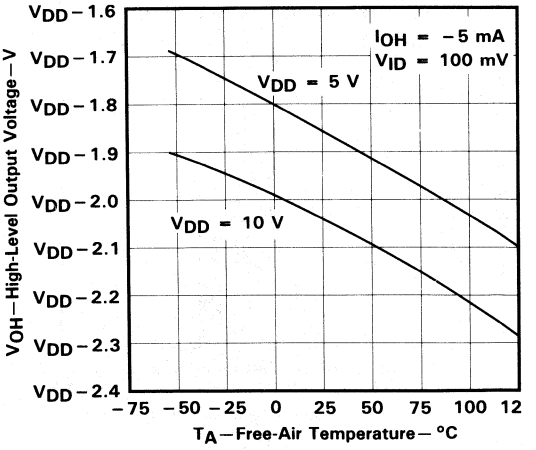


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

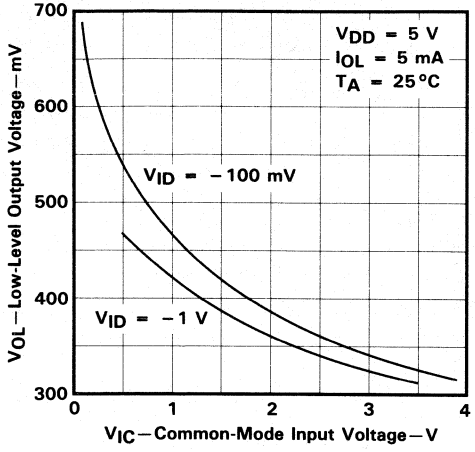


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

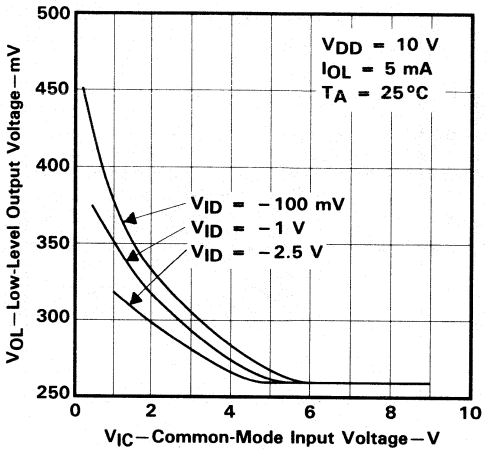


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

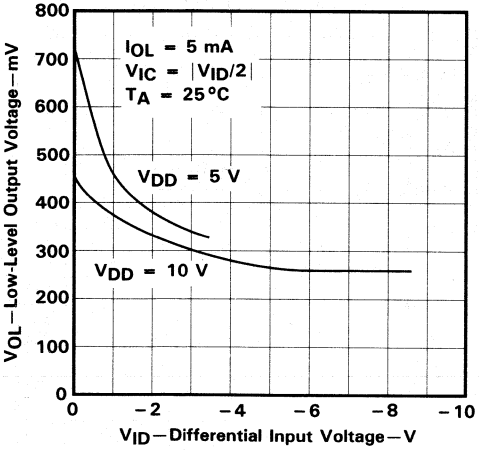


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

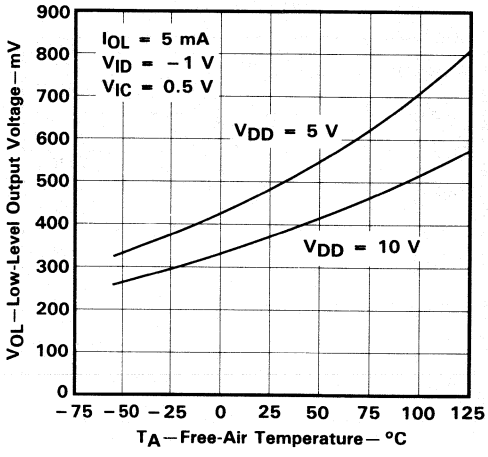


FIGURE 17

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

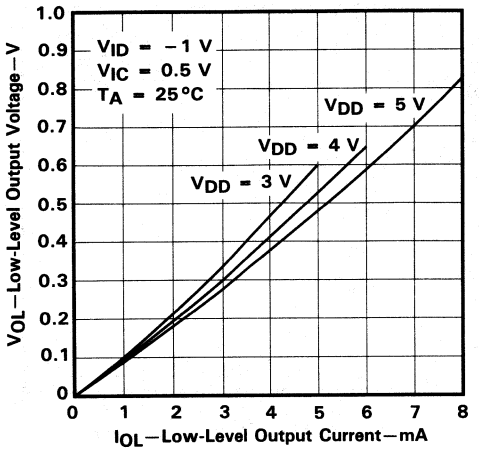


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

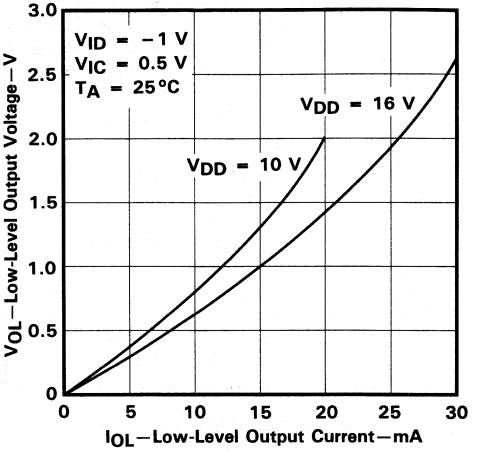


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

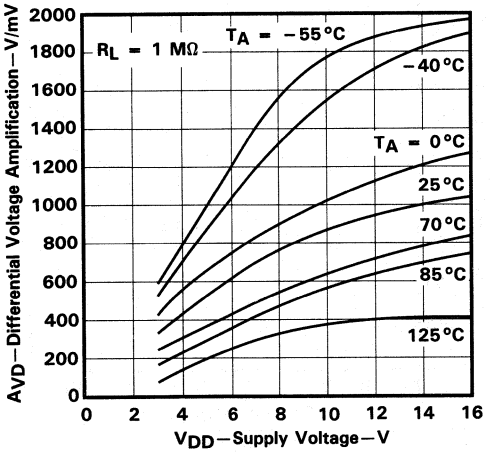


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

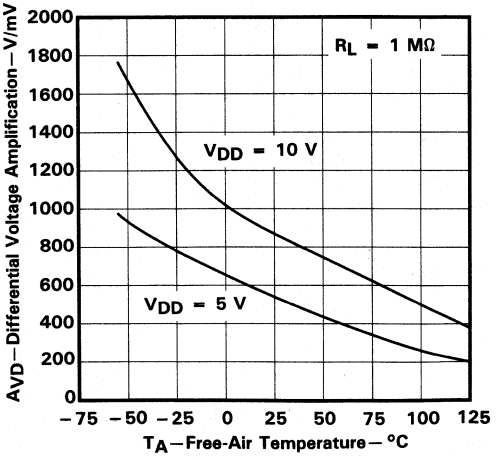


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

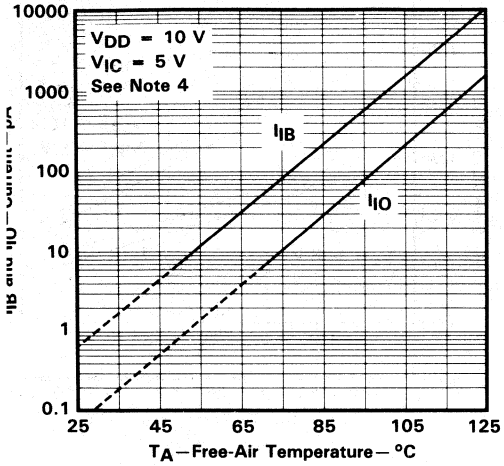


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

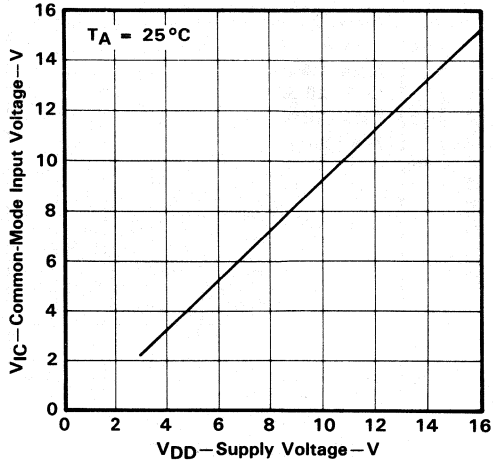


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

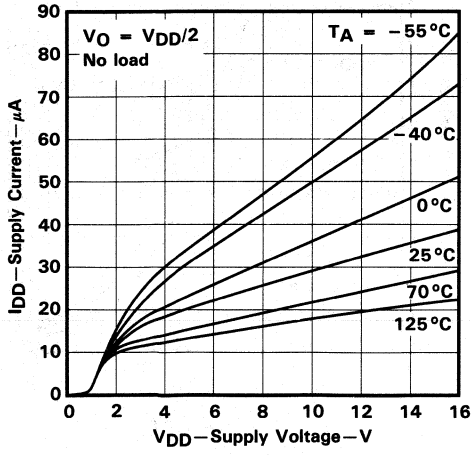


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

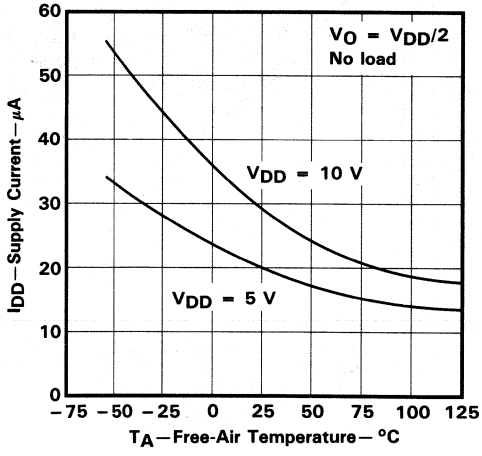


FIGURE 25

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

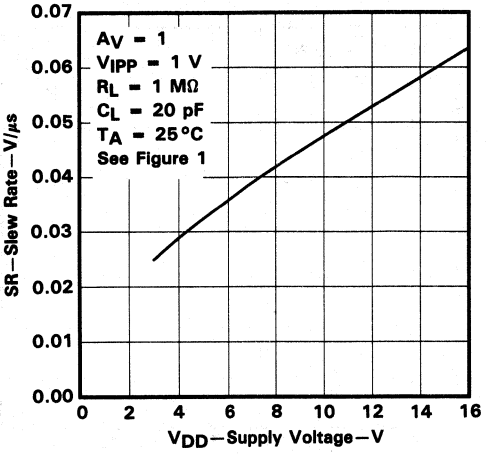


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

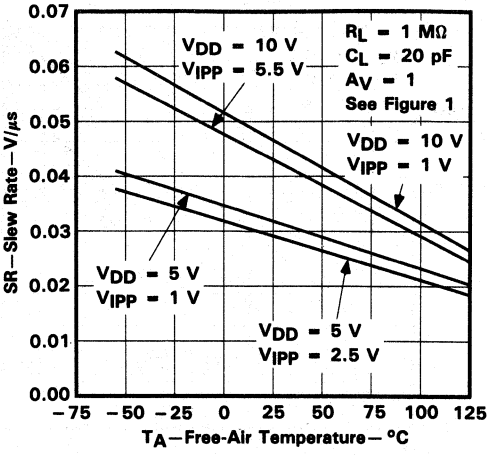


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

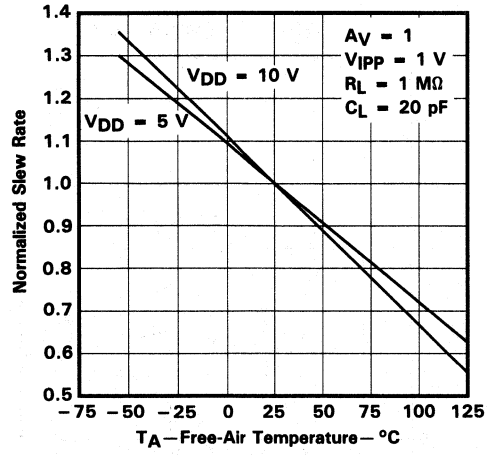


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAG
vs
FREQUENCY

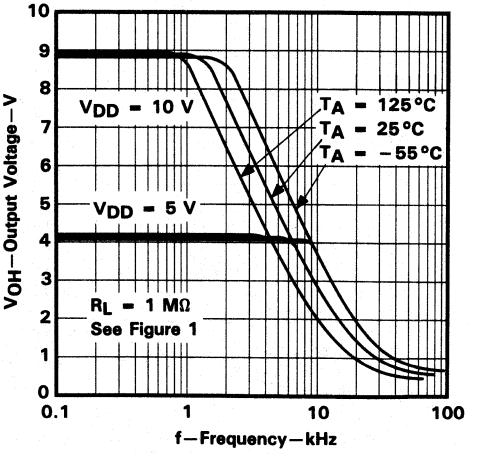


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

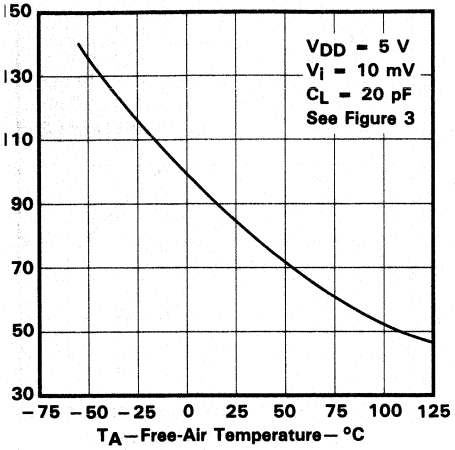


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

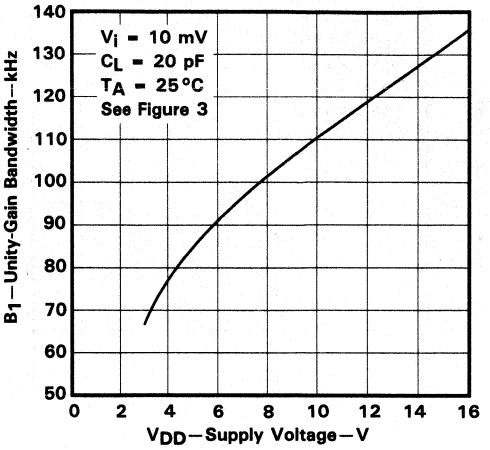


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

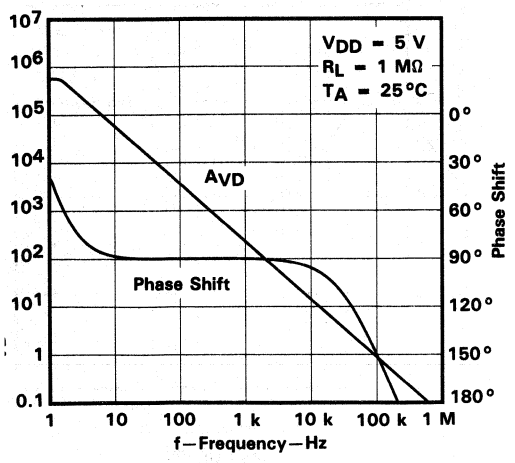


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

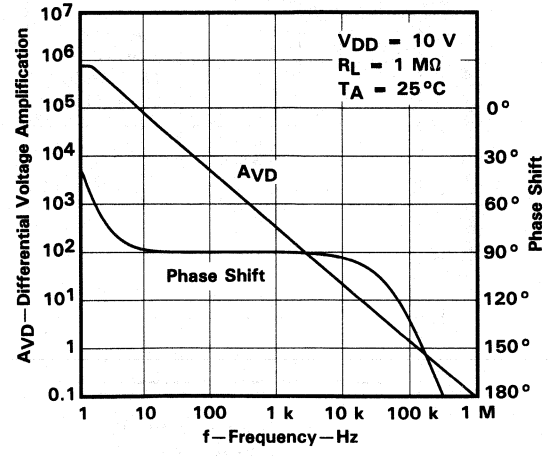


FIGURE 33

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

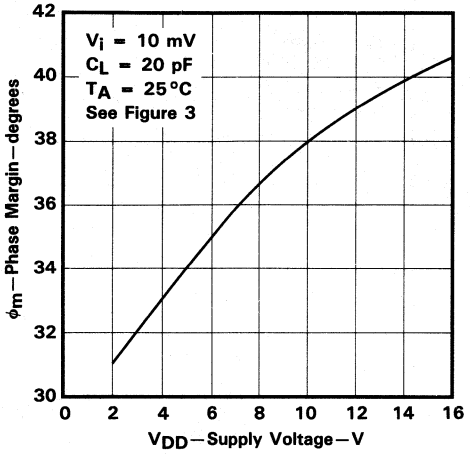


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

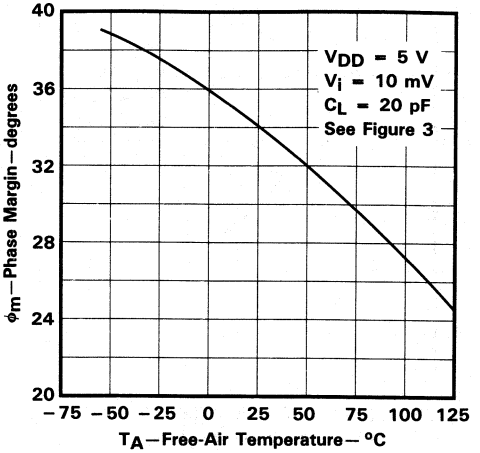


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

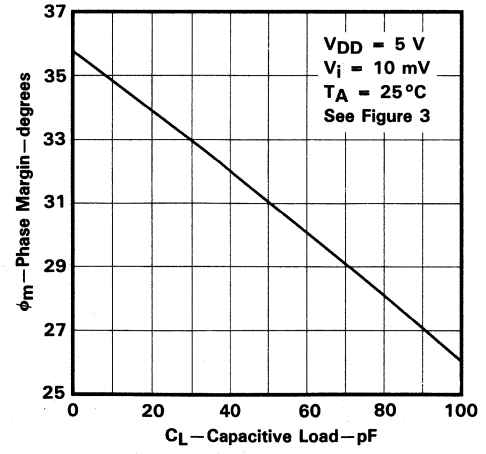


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

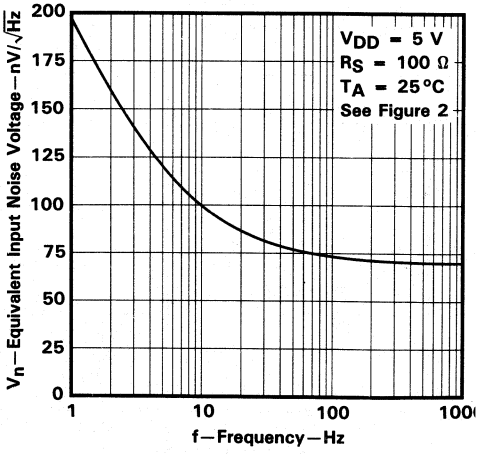


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

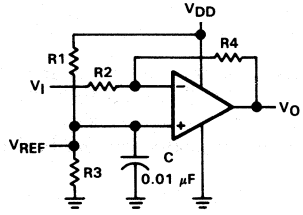
ingle-supply operation

While the TLC27L2 and TLC27L7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L2 and TLC27L7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L2 and TLC27L7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

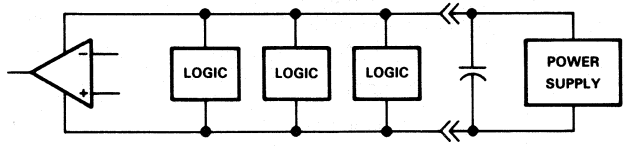
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



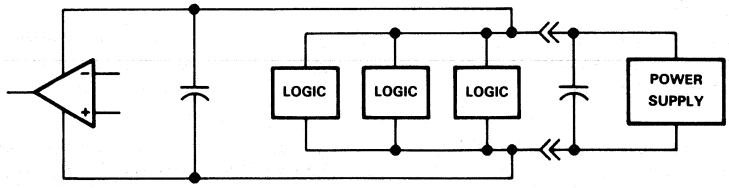
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L2 and TLC27L7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A = 25°C$ and at $V_{DD}-1.5$ V at all other temperatures.

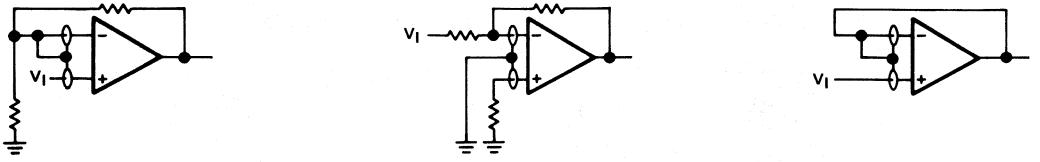
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L2 and TLC27L7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L2 and TLC27L7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L2 and TLC27L7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

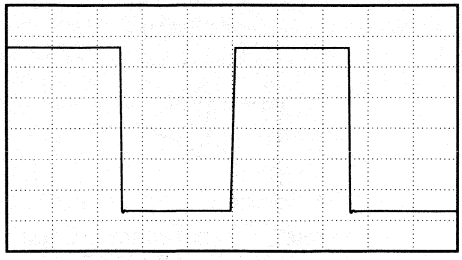
FIGURE 40. GUARD-RING SCHEMES

output characteristics

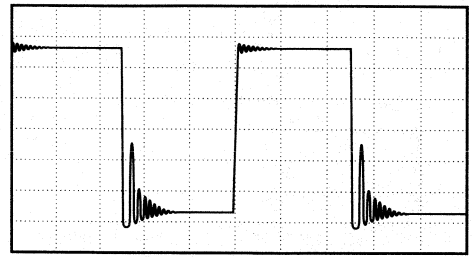
The output stage of the TLC27L2 and TLC27L7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L2 and TLC27L7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

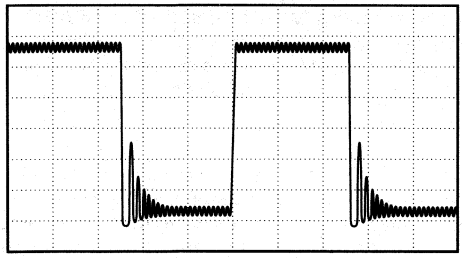
TYPICAL APPLICATION DATA



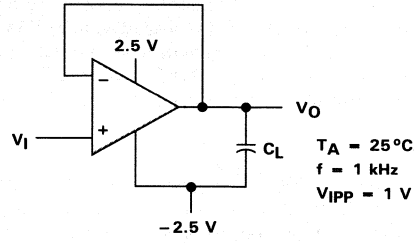
(a) C_L = 20 pF, R_L = No load



(b) C_L = 260 pF, R_L = No load



(c) C_L = 310 pF, R_L = No load



(d) Test Circuit

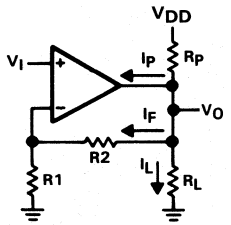
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L2 and TLC27L7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

eedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

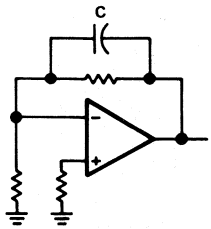


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L2 and TLC27L7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L2 and TLC27L7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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TYPICAL APPLICATION DATA

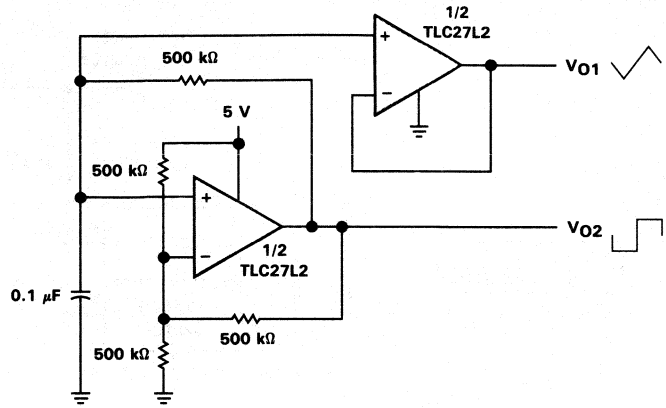
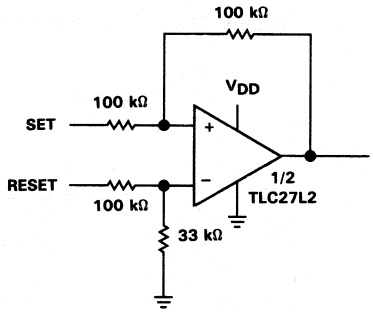


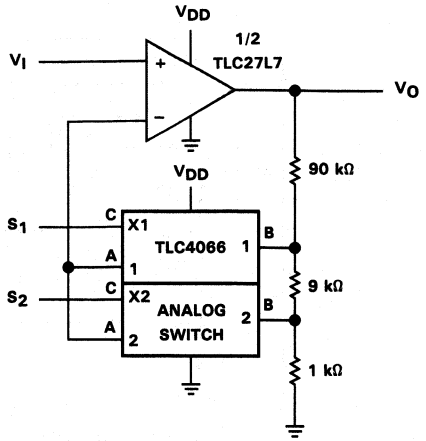
FIGURE 44. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

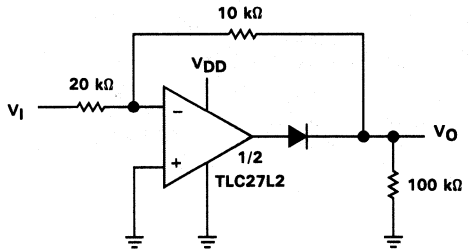
TYPICAL APPLICATION DATA



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

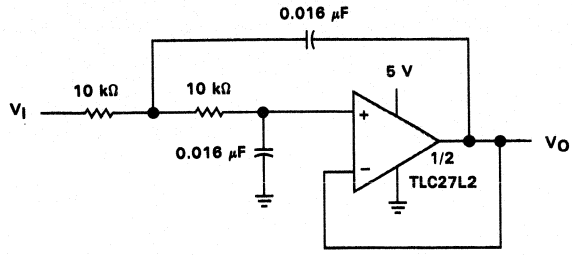
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

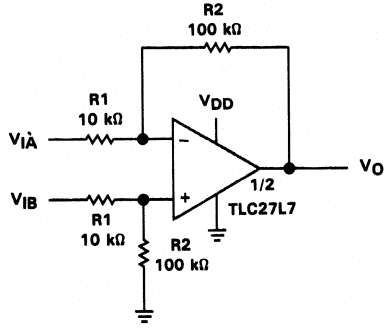
FIGURE 47. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

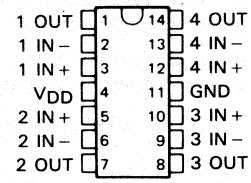
$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

FIGURE 49. DIFFERENCE AMPLIFIER

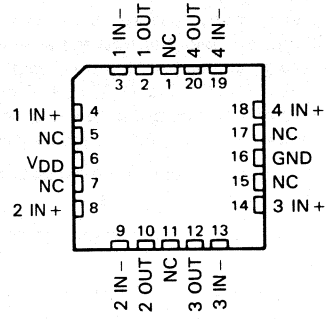
D3142, OCTOBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage:**
  TLC27L9 . . . 900 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Ultra-Low Power . . . Typically 195 μW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



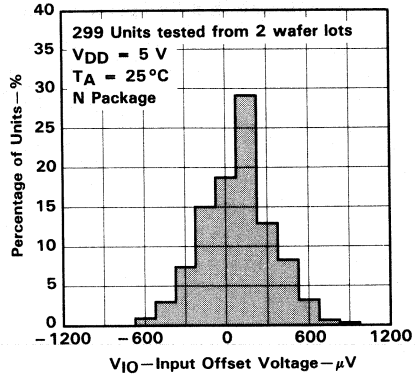
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC27L9CD	—	TLC27L9CJ	TLC27L9CN
	2 mV	TLC27L4BCD	—	TLC27L4BCJ	TLC27L4BCN
	5 mV	TLC27L4ACD	—	TLC27L4ACJ	TLC27L4ACN
	10 mV	TLC27L4CD	—	TLC27L4CJ	TLC27L4CN
−40°C to 85°C	900 μV	TLC27L9ID	—	TLC27L9IJ	TLC27L9IN
	2 mV	TLC27L4BID	—	TLC27L4BIJ	TLC27L4BIN
	5 mV	TLC27L4AID	—	TLC27L4AIJ	TLC27L4AIN
	10 mV	TLC27L4ID	—	TLC27L4IJ	TLC27L4IN
−55°C to 125°C	900 μV	—	TLC27L9MFK	TLC27L9MJ	—
	10 mV	—	TLC27L4MFK	TLC27L4MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27L9CDR).

DISTRIBUTION OF TLC27L9
INPUT OFFSET VOLTAGE



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description

The TLC27L4 and TLC27L9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, extremely low power, and high gain.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and low power consumption make these cost-effective devices ideal for high gain, low frequency, low power applications. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L4 (10 mV) to the high-precision TLC27L9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading exisitng designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27L4 and TLC27L9. The devices also exhibit low voltage single-supply operation and ultra-low power comsumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27L4 and TLC27L9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

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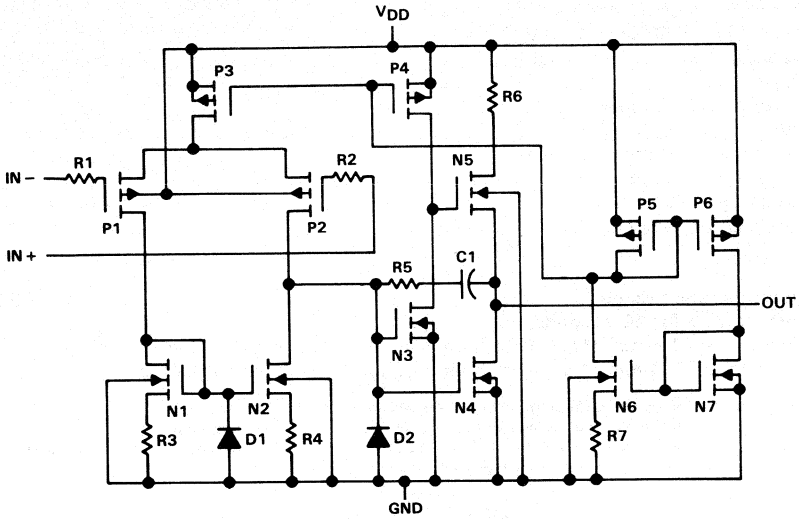
equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . ±V_{DD}
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		200	900	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−55°C	3	4.1		
					125°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−55°C	25	950		
					125°C	25	200		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	95		
					125°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		39	68	μA
					−55°C		69	120	
					125°C		27	48	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		210	1200	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.4		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−55°C	7.8	8.8		
					125°C	7.8	9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−55°C	25	1750		
					125°C	25	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−55°C	60	97		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−55°C	60	97		
					125°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					−55°C		111	192	
					125°C		35	60	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

Electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		240	2000	μV
					Full range			3500	
		TLC27L9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		200	900	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					−40°C	3	4.1		
					85°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	480		V/mV
					−40°C	50	900		
					85°C	50	330		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	95		
					85°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		39	68	μA
					−40°C		62	108	
					85°C		29	52	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27L4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			7	
		TLC27L4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		260	2000	μV
					Full range			3500	
		TLC27L9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		210	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					−40°C	7.8	8.9		
					85°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	800		V/mV
					−40°C	50	1550		
					85°C	50	585		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					−40°C	60	97		
					85°C	60	98		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					−40°C	60	97		
					85°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					−40°C		98	172	
					85°C		40	72	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

Electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		240	2000	μV
					Full range			3000	
		TLC27L9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		200	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	3.2	4.1		V
					0°C	3	4.1		
					70°C	3	4.2		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 1 MΩ	25°C	50	520		V/mV
					0°C	50	680		
					70°C	50	380		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	95		
					70°C	60	95		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		40	68	μA
					0°C		48	84	
					70°C		31	56	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27L4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27L4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27L4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		260	2000	μV
					Full range			3000	
		TLC27L9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 1 MΩ	25°C		210	1200	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 1 MΩ	25°C	8	8.9		V
					0°C	7.8	8.9		
					70°C	7.8	8.9		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 1 MΩ	25°C	50	870		V/mV
					0°C	50	1020		
					70°C	50	660		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	97		dB
					0°C	60	97		
					70°C	60	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	97		dB
					0°C	60	97		
					70°C	60	98		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		57	92	μA
					0°C		72	132	
					70°C		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

perating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−55°C		0.04		
				125°C		0.02		
			V_{IPP} = 2.5 V	25°C		0.03		
				−55°C		0.04		
				125°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−55°C		8		
				125°C		3		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−55°C		140		
				125°C		45		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−55°C		39°		
				125°C		25°		

perating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−55°C		0.06		
				125°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−55°C		0.06		
				125°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−55°C		1.5		
				125°C		0.7		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−55°C		165		
				125°C		70		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−55°C		43°		
				125°C		29°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				−40°C		0.04		
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				−40°C		0.04		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				−40°C		7		
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				−40°C		130		
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				−40°C		38°		
				85°C		28°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				−40°C		0.06		
				85°C		0.03		
			V_{IPP} = 5.5 V	25°C		0.04		
				−40°C		0.05		
				85°C		0.03		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				−40°C		1.4		
				85°C		0.8		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				−40°C		155		
				85°C		80		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				−40°C		42°		
				85°C		32°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.03		V/μs
				0°C		0.04		
				70°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				0°C		0.03		
				70°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		5		kHz
				0°C		6		
				70°C		4.5		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		85		kHz
				0°C		100		
				70°C		65		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		34°		
				0°C		36°		
				70°C		30°		

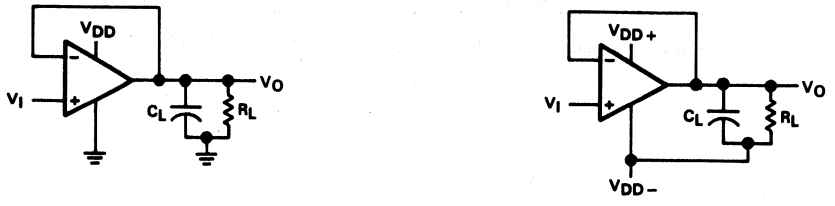
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.05		V/μs
				0°C		0.05		
				70°C		0.04		
			V_{IPP} = 5.5 V	25°C		0.04		
				0°C		0.05		
				70°C		0.04		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		70		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 1 MΩ,	C_L = 20 pF, See Figure 1	25°C		1		kHz
				0°C		1.3		
				70°C		0.9		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		110		kHz
				0°C		125		
				70°C		90		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		38°		
				0°C		40°		
				70°C		34°		

PARAMETER MEASUREMENT INFORMATION

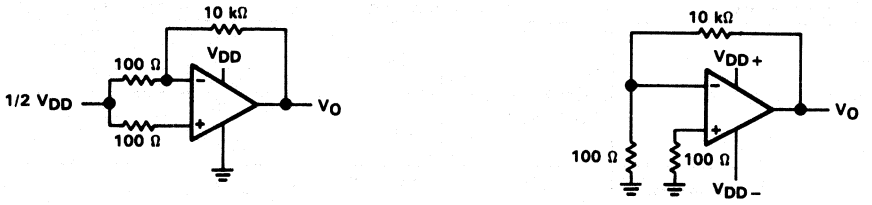
single-supply versus split-supply test circuits

Because the TLC27L4 and TLC27L9 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



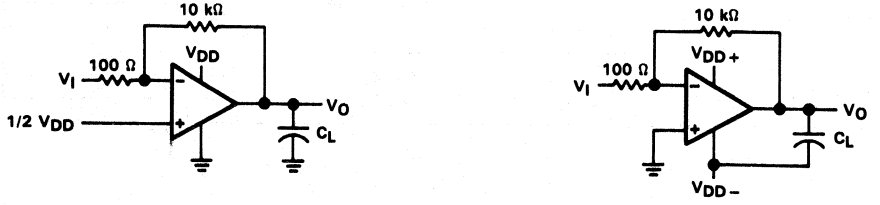
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 2. NOISE TEST CIRCUIT



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

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PARAMETER MEASUREMENT INFORMATION

ıput bias current

Because of the high input impedance of the TLC27L4 and TLC27L9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

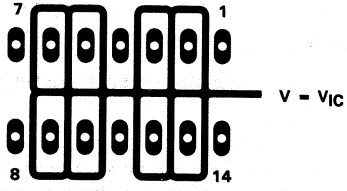

FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (J AND N DUAL-IN-LINE-PACKAGE)

ɔw-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

ıput offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

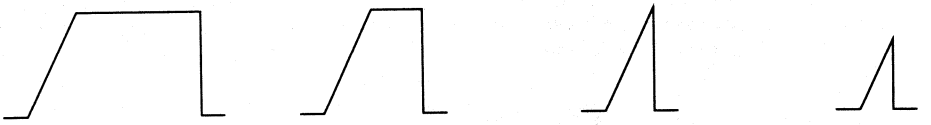

FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

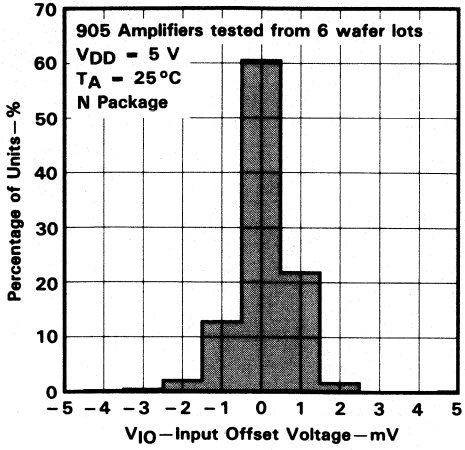

FIGURE 6

DISTRIBUTION OF TLC27L4
INPUT OFFSET VOLTAGE

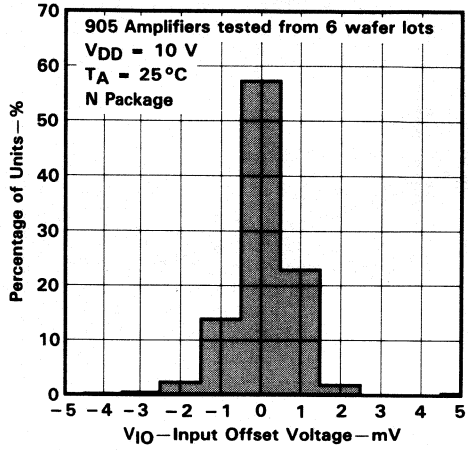

FIGURE 7

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

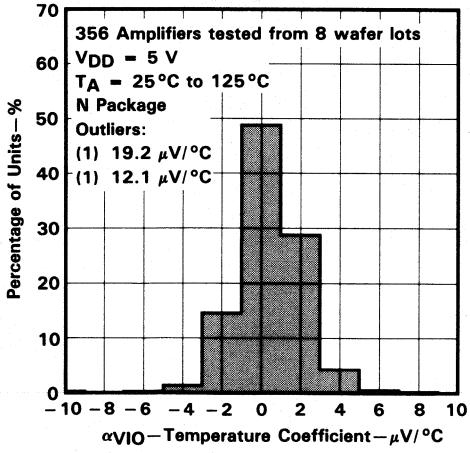

FIGURE 8

DISTRIBUTION OF TLC27L4 AND TLC27L9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

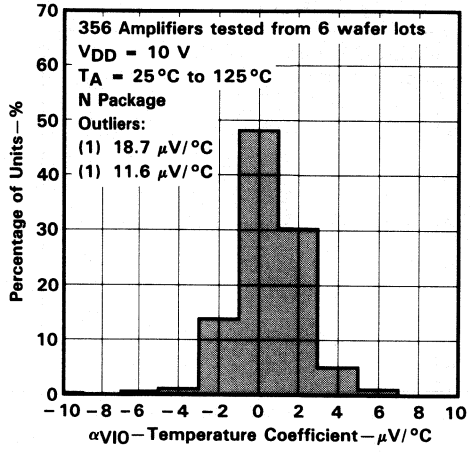

FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

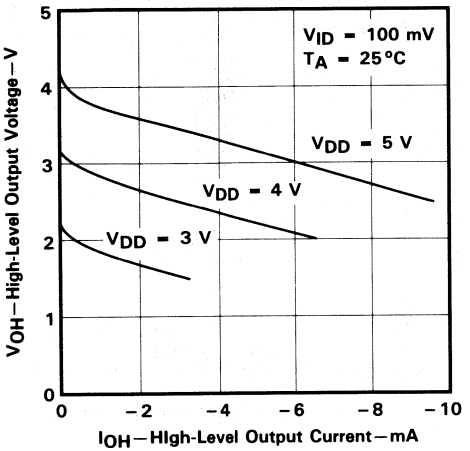

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

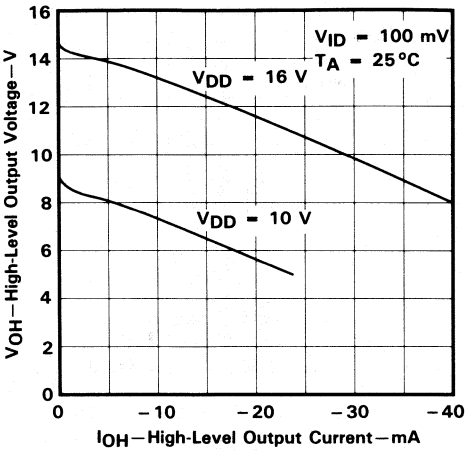

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

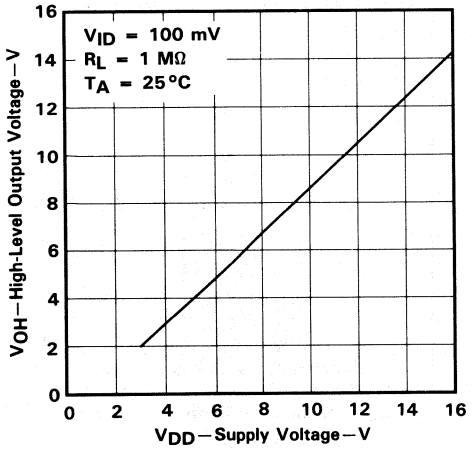

FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

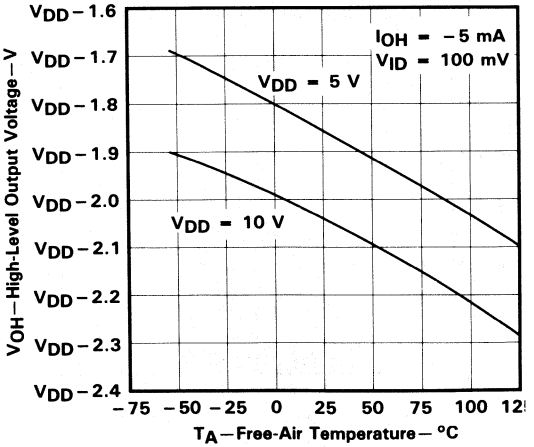

FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

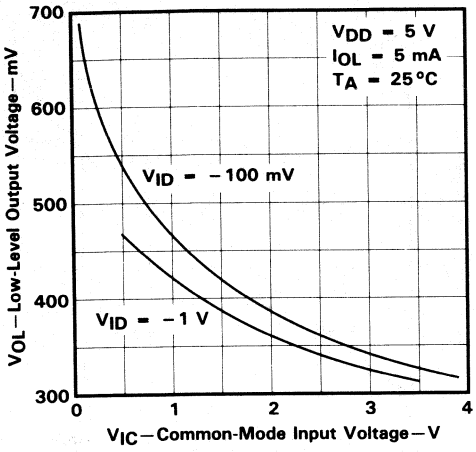

FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

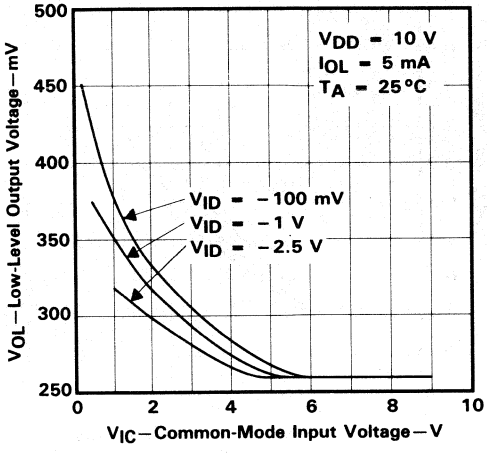

FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

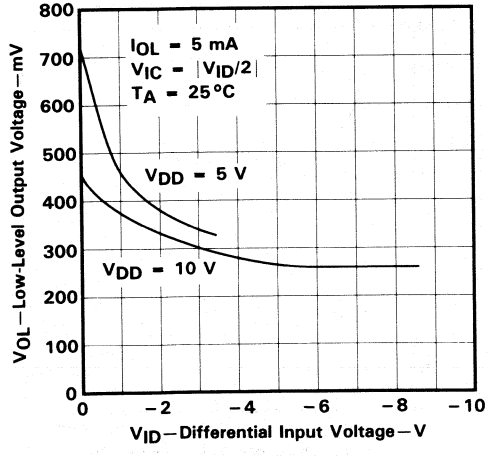

FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

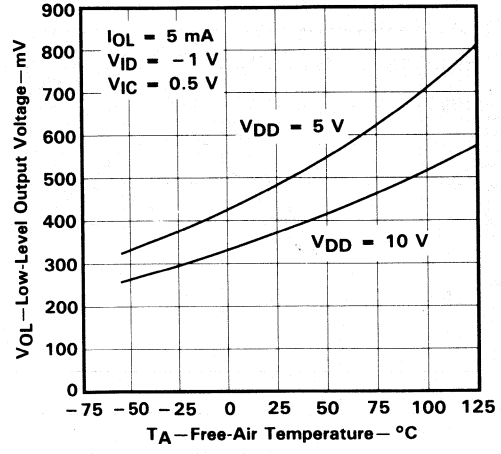

FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

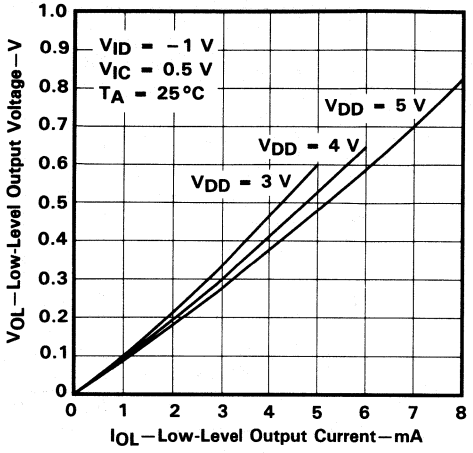

FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

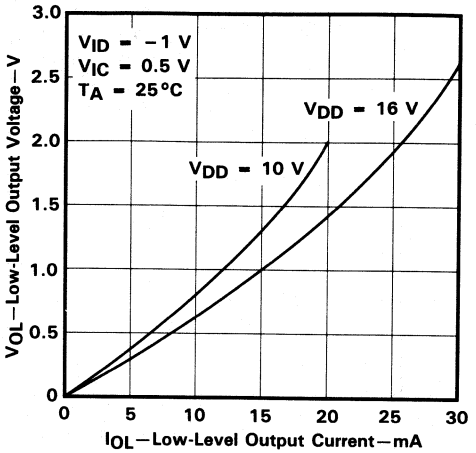

FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

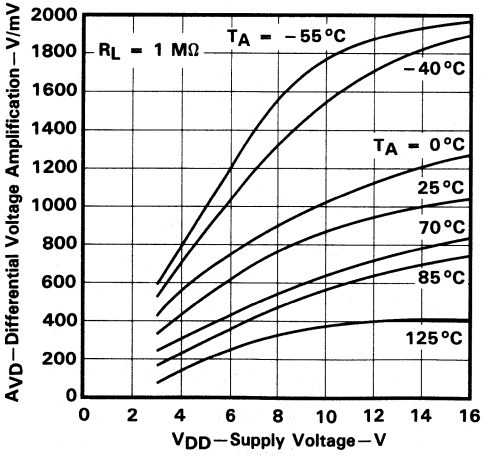

FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

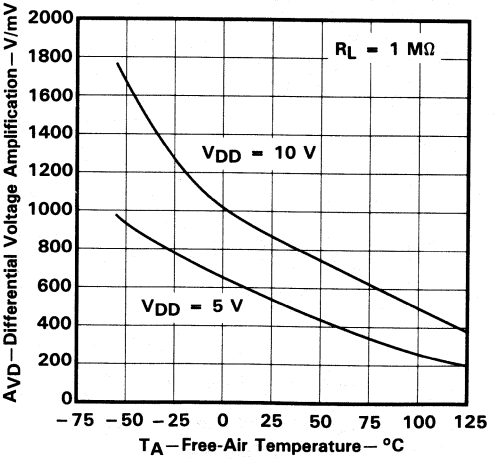

FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

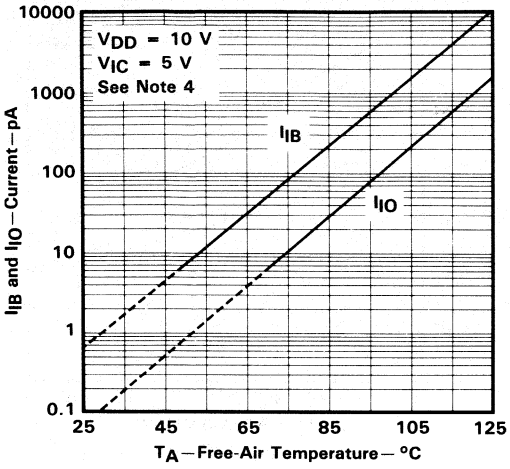


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

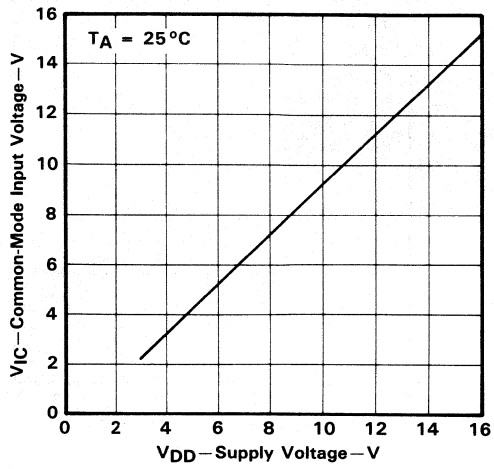


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

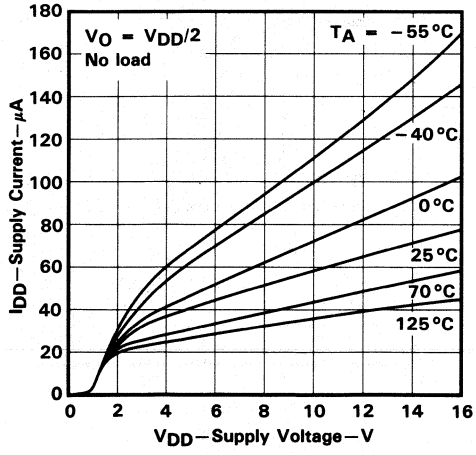


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

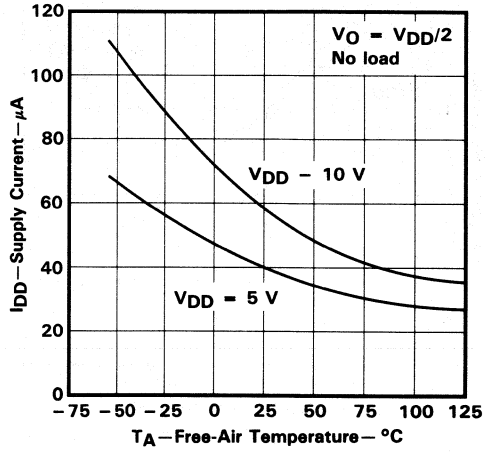


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

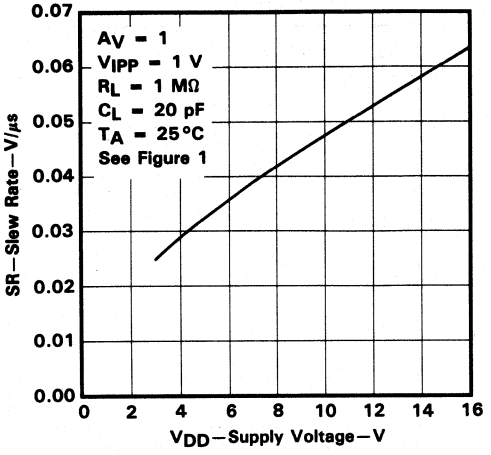


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

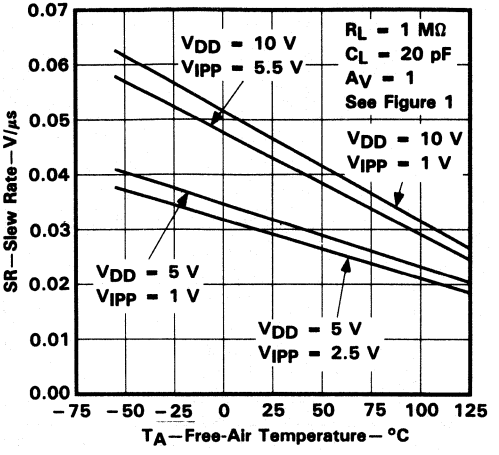


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

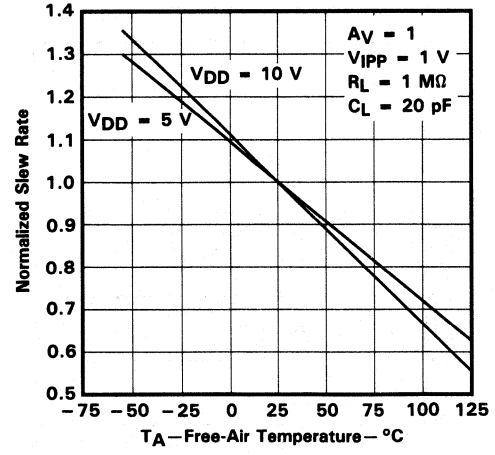


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

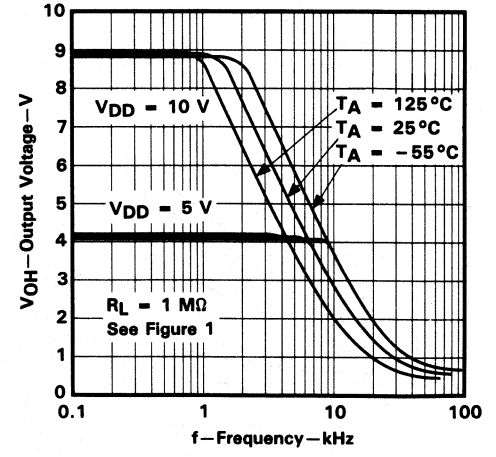


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

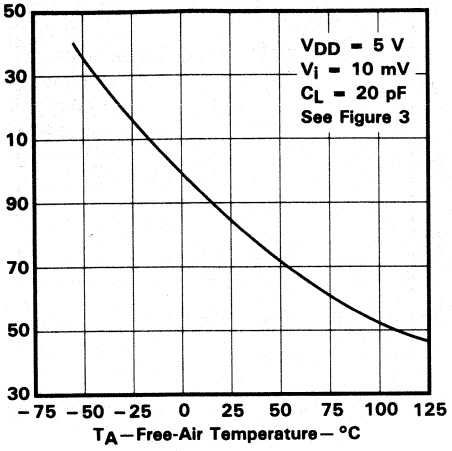


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

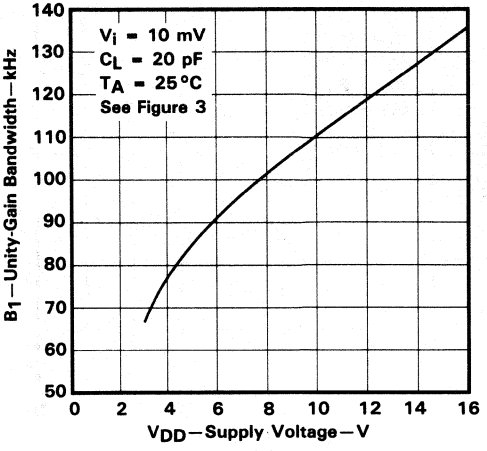


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

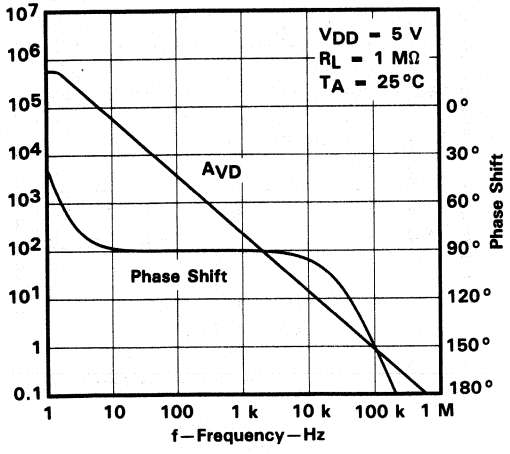


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

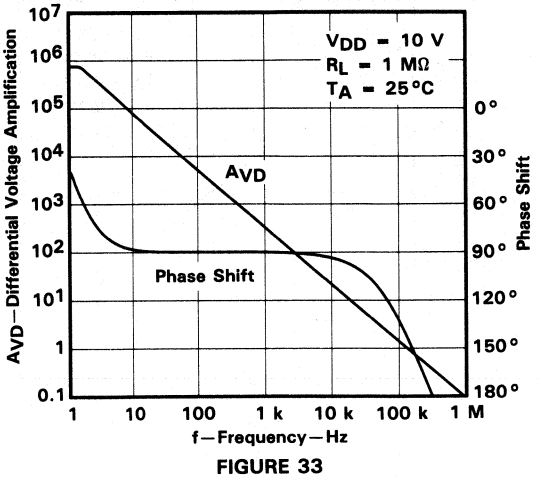


FIGURE 33

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

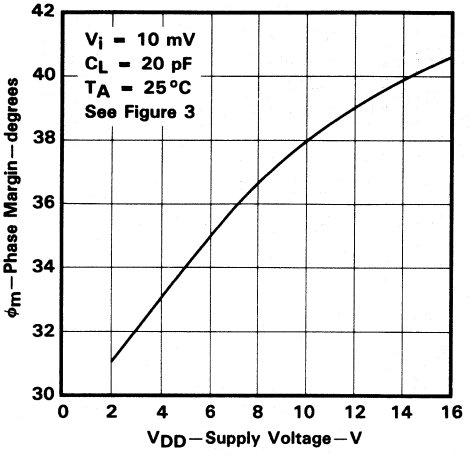


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

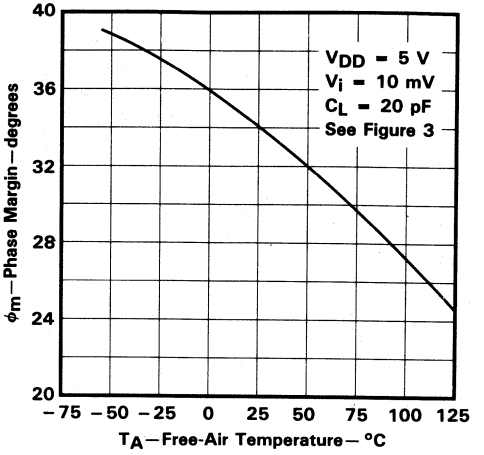


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

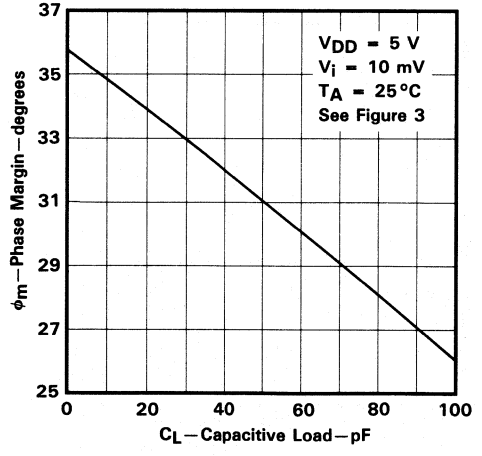


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

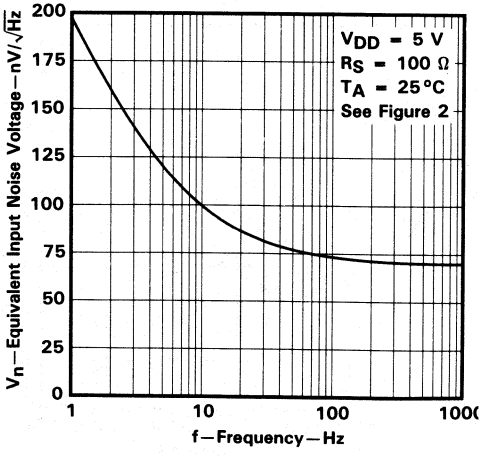


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

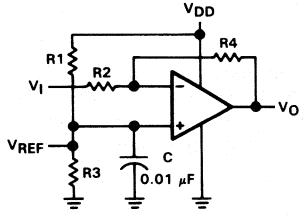
ingle-supply operation

While the TLC27L4 and TLC27L9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27L4 and TLC27L9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L4 and TLC27L9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

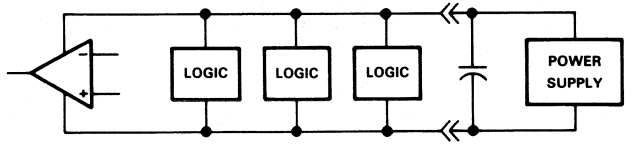
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



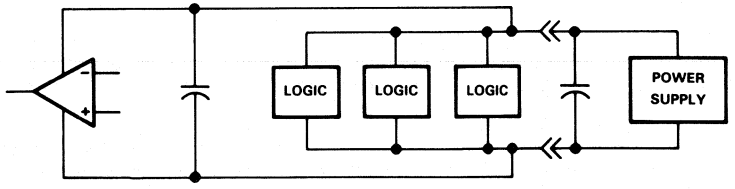
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27L4 and TLC27L9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

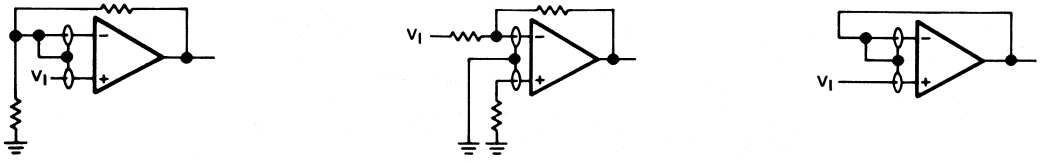
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27L4 and TLC27L9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27L4 and TLC27L9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27L4 and TLC27L9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27L4 and TLC27L9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27L4 and TLC27L9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

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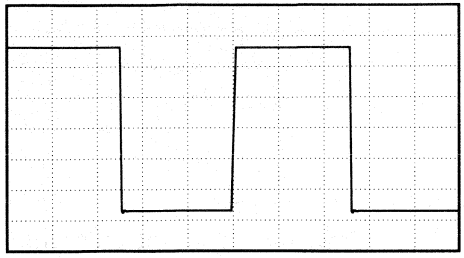
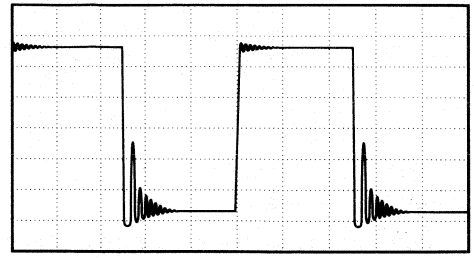
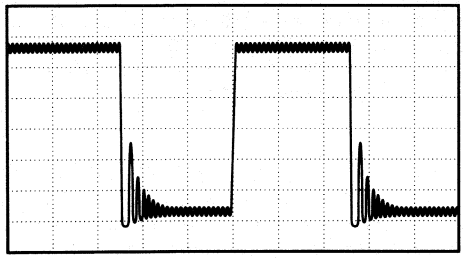
TYPICAL APPLICATION DATA



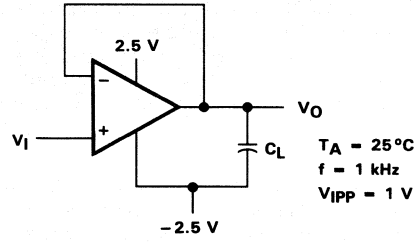
(a) C_L = 20 pF, R_L = NO LOAD



(b) C_L = 260 pF, R_L = NO LOAD



(c) C_L = 310 pF, R_L = NO LOAD



(d) TEST CIRCUIT

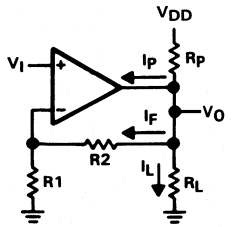
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27L4 and TLC27L9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

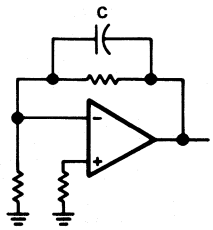


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27L4 and TLC27L9 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27L4 and TLC27L9 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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TYPICAL APPLICATION DATA

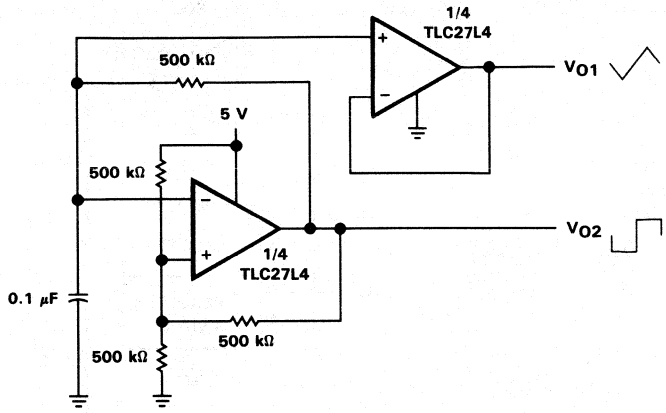
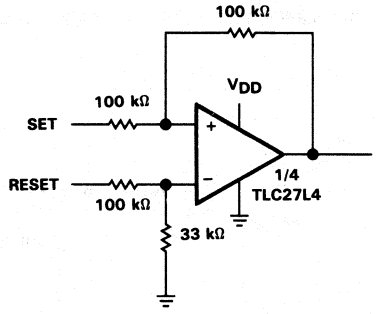


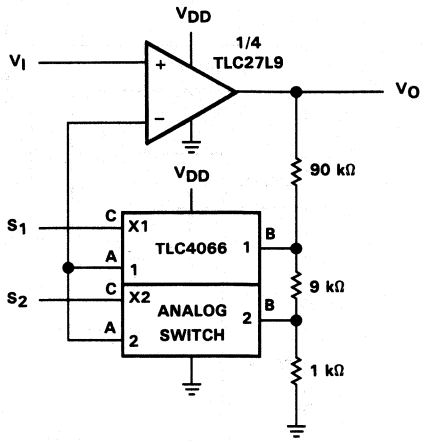
FIGURE 44. MULTIVIBRATOR



NOTE: V_{DD} = 5 V to 16 V

FIGURE 45. SET/RESET FLIP-FLOP

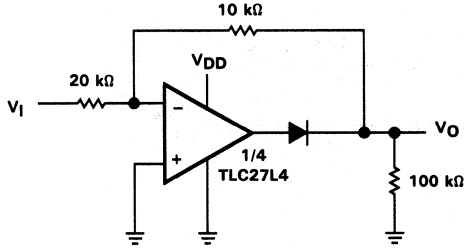
TYPICAL APPLICATION DATA



SELECT:	S_1	S_2
A_V	10	100

NOTE: V_{DD} = 5 V to 12 V

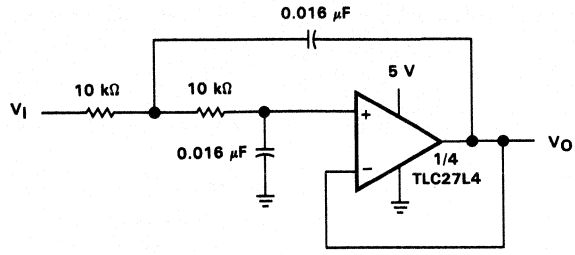
FIGURE 46. AMPLIFIER WITH DIGITAL GAIN SELECTION



NOTE: V_{DD} = 5 V to 16 V

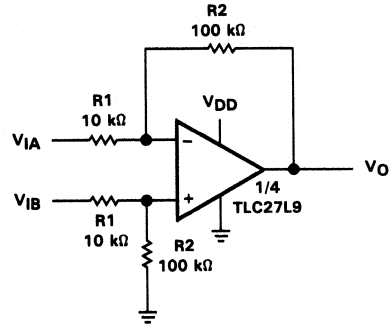
FIGURE 47. FULL-WAVE RECTIFIER

TYPICAL APPLICATION DATA



NOTE: Normalized to F_C = 1 kHz and R_L = 10 kΩ

FIGURE 48. TWO-POLE LOW-PASS BUTTERWORTH FILTER



NOTES: V_{DD} = 5 V to 16 V

$$V_O = \frac{R2}{R1}(V_{IB} - V_{IA})$$

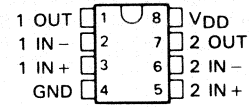
FIGURE 49. DIFFERENCE AMPLIFIER

2 Operational Amplifiers

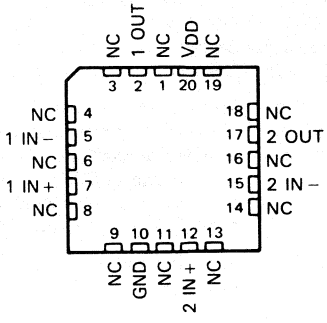
D3140, OCTOBER 1987—REVISED FEBRUARY 1989

- **Trimmed Offset Voltage:**
  TLC27M7 . . . 500 μV Max at 25 °C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55 °C to 125 °C . . . 4 V to 16 V
  −40 °C to 85 °C . . . 4 V to 16 V
  0 °C to 70 °C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 32 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25 °C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



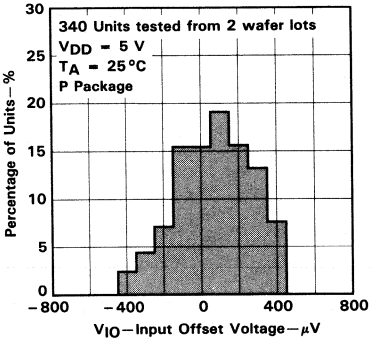
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25 °C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0 °C to 70 °C	500 μV	TLC27M7CD	—	TLC27M7CJG	TLC27M7CP
	2 mV	TLC27M2BCD	—	TLC27M2BCJG	TLC27M2BCP
	5 mV	TLC27M2ACD	—	TLC27M2ACJG	TLC27M2ACP
	10 mV	TLC27M2CD	—	TLC27M2CJG	TLC27M2CP
−40 °C to 85 °C	500 μV	TLC27M7ID	—	TLC27M7IJG	TLC27M7IP
	2 mV	TLC27M2BID	—	TLC27M2BIJG	TLC27M2BIP
	5 mV	TLC27M2AID	—	TLC27M2AIJG	TLC27M2AIP
	10 mV	TLC27M2ID	—	TLC27M2IJG	TLC27M2IP
−55 °C to 125 °C	500 μV	—	TLC27M7MFK	TLC27M7MJG	—
	10 mV	—	TLC27M2MFK	TLC27M2MJG	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27M7CDR).

DISTRIBUTION OF TLC27M7
INPUT OFFSET VOLTAGE



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description

The TLC27M2 and TLC27M7 dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications which have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M2 (10 mV) to the high-precision TLC27M7 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M2 and TLC27M7. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27M2 and TLC27M7 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. I-suffix devices are characterized for operation from −40°C to 85°C, and C-suffix devices are characterized for operation from 0°C to 70°C.

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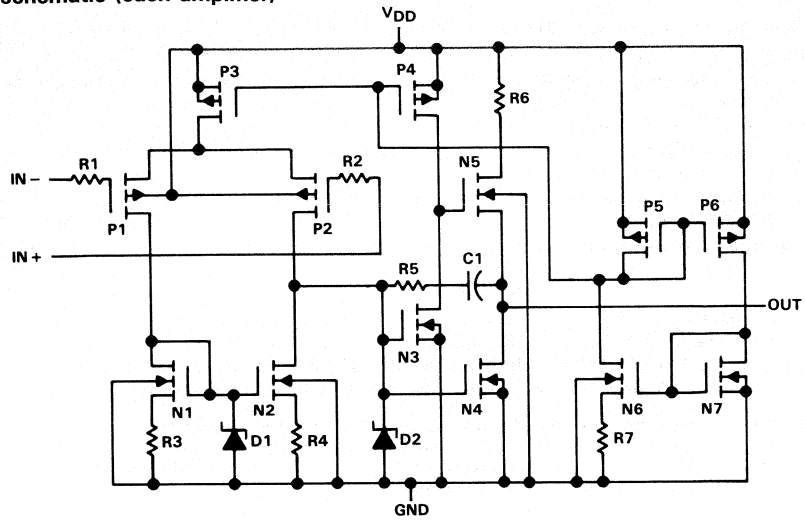
equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (C-, I-suffix)	825 mW	6.6 mW/°C	528 mW	429 mW	
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		185	500	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−55°C	3	3.9		
					125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−55°C	15	290		
					125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					−55°C	60	89		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		210	560	μA
					−55°C		340	880	
					125°C		140	360	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M7M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		190	800	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−55°C	7.8	8.6		
					125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−55°C	15	420		
					125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	93		
					125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	μA
					−55°C		490	1000	
					125°C		180	480	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M2AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M2BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		220	2000	μV
					Full range			3500	
		TLC27M7I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		185	500	
					Full range			2000	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					85°C		24	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					85°C		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−40°C	3	3.9		
					85°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−40°C	15	270		
					85°C	15	130		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					−40°C	60	90		
					85°C	60	90		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		210	560	μA
					−40°C		315	800	
					85°C		160	400	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2I	V_O = 1.4 V,	V_{IC} = 0 V,	25°C		1.1	10	mV
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			13	
		TLC27M2AI	V_O = 1.4 V,	V_{IC} = 0 V,	25°C		0.9	5	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			7	
		TLC27M2BI	V_O = 1.4 V,	V_{IC} = 0 V,	25°C		224	2000	μV
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			3500	
		TLC27M7I	V_O = 1.4 V,	V_{IC} = 0 V,	25°C		190	800	
			R_S = 50 Ω,	R_L = 100 kΩ	Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−40°C	7.8	8.7		
					85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−40°C	15	390		
					85°C	15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	93		
					85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	μA
					−40°C		450	900	
					85°C		205	520	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		220	2000	μV
					Full range			3000	
		TLC27M7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		185	500	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		210	560	μA
					0°C		250	640	
					70°C		170	440	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M2C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M2AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M2BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		224	2000	μV
					Full range			3000	
		TLC27M7C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0 V, R_L = 100 kΩ	25°C		190	800	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					0°C	15	320		
					70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (two amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		285	600	μA
					0°C		345	800	
					70°C		220	560	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

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perating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.49		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

perating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		600		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

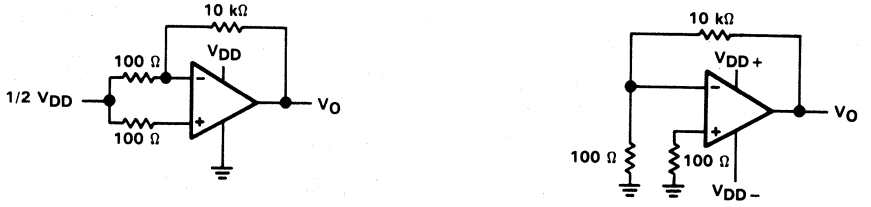
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC27M2 and TLC27M7 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

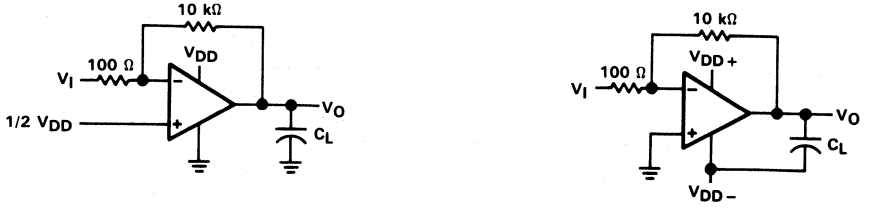
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

nput bias current

Because of the high input impedance of the TLC27M2 and TLC27M7 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

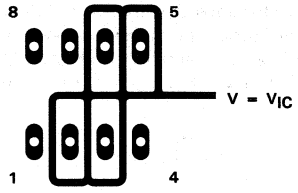


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (JG AND P DUAL-IN-LINE-PACKAGE)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing, is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

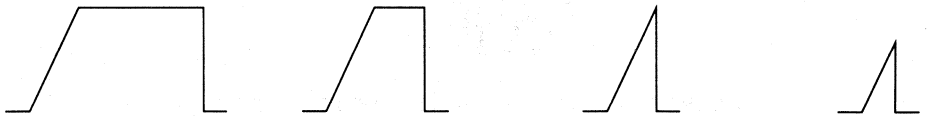


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

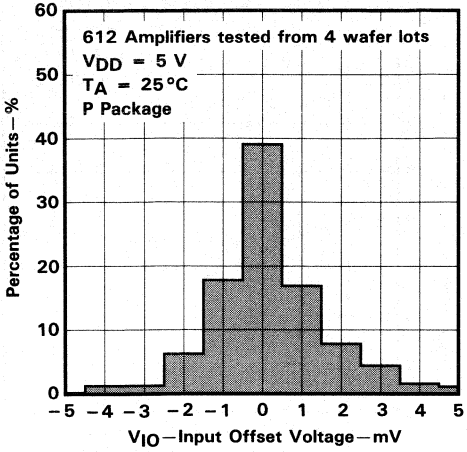


FIGURE 6

DISTRIBUTION OF TLC27M2
INPUT OFFSET VOLTAGE

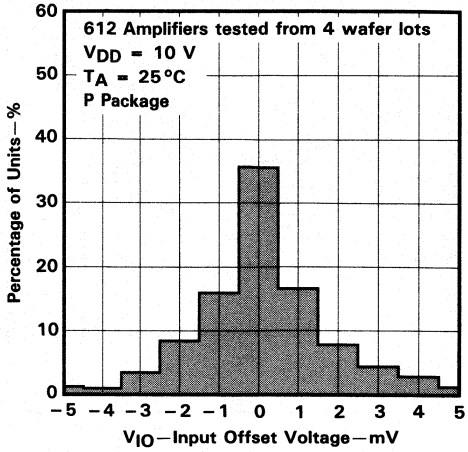


FIGURE 7

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

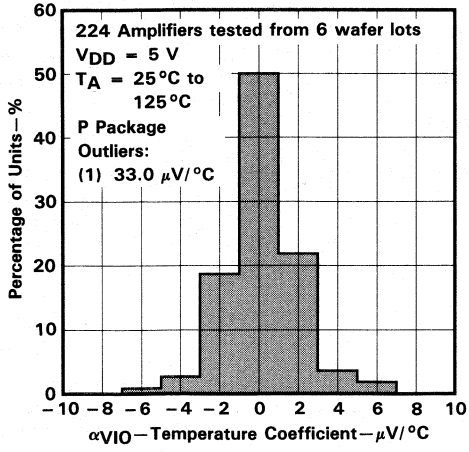


FIGURE 8

DISTRIBUTION OF TLC27M2 AND TLC27M7
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

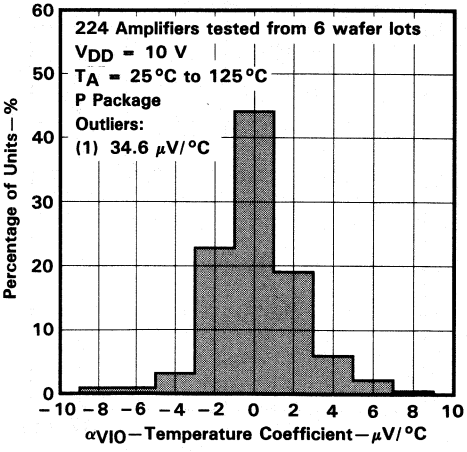


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

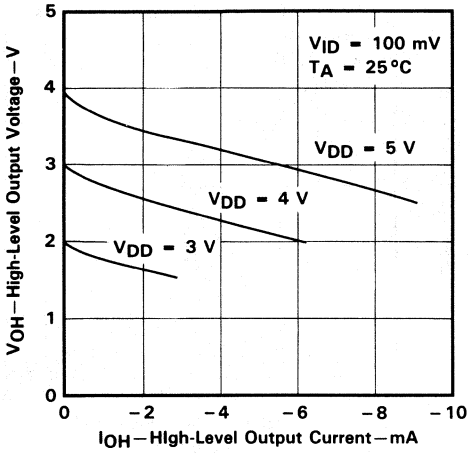


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

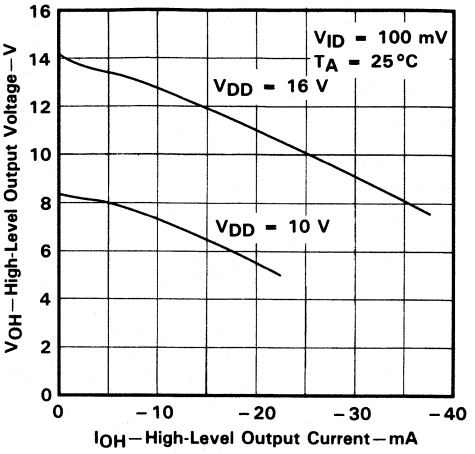


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

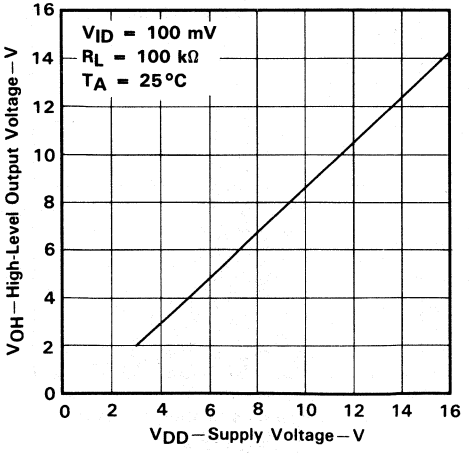


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

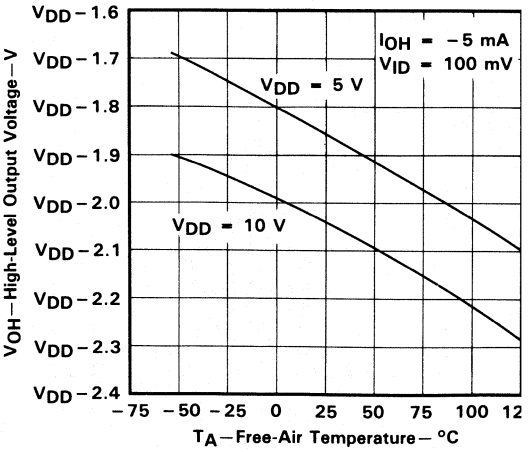


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

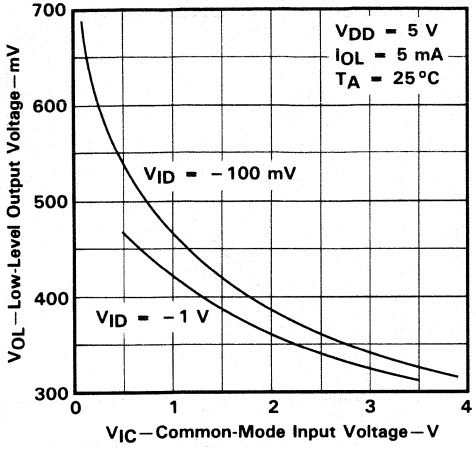


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

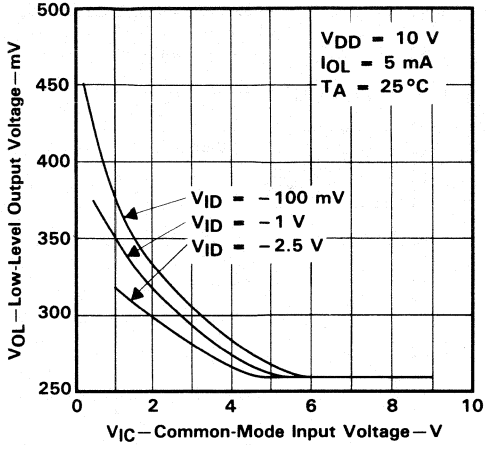


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

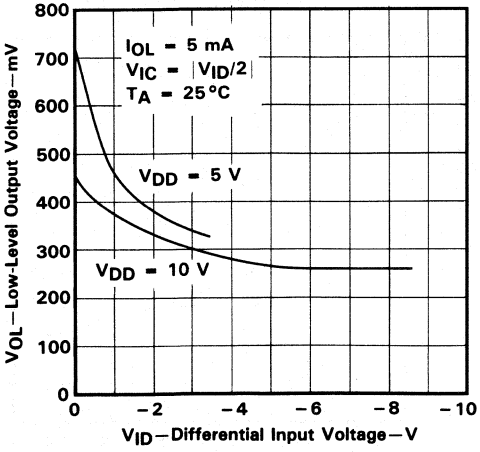


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

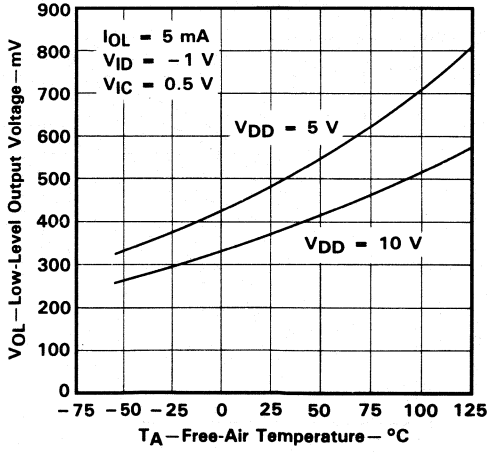


FIGURE 17

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

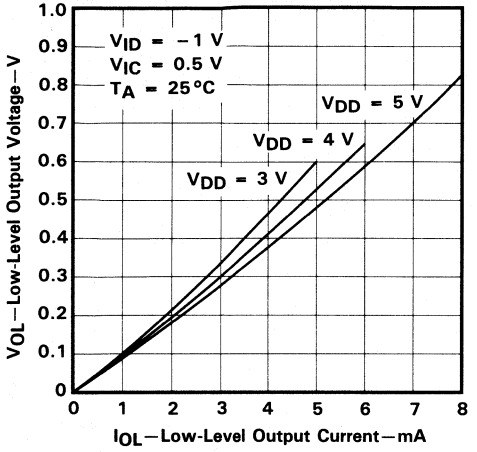


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

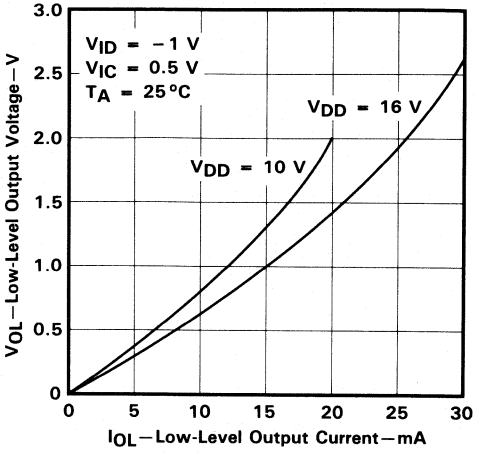


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

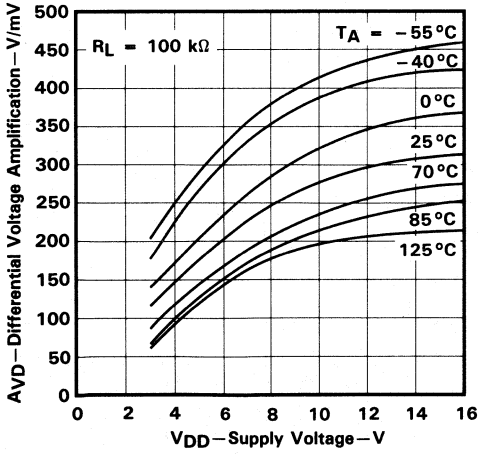


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

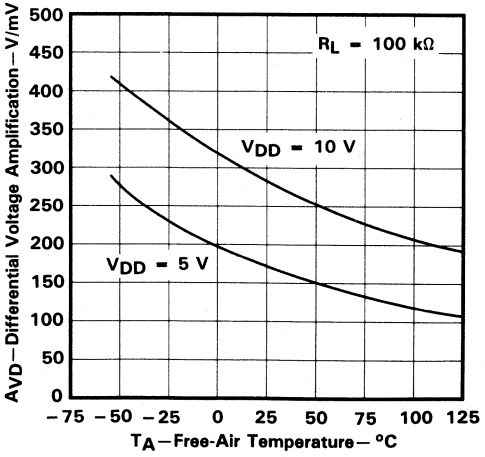


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

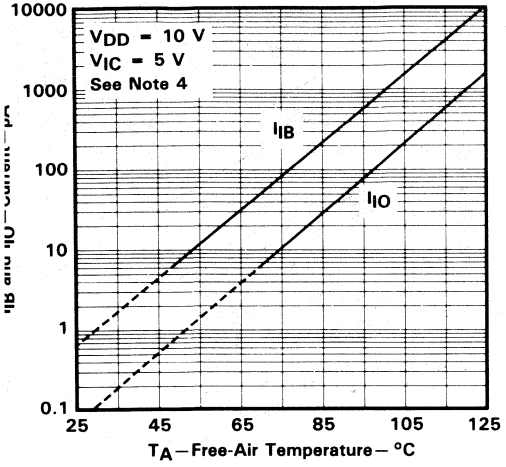


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

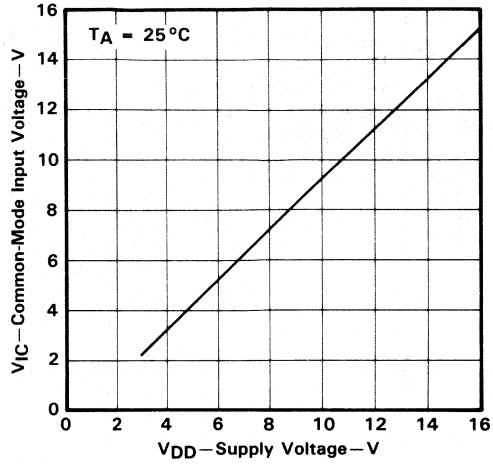


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

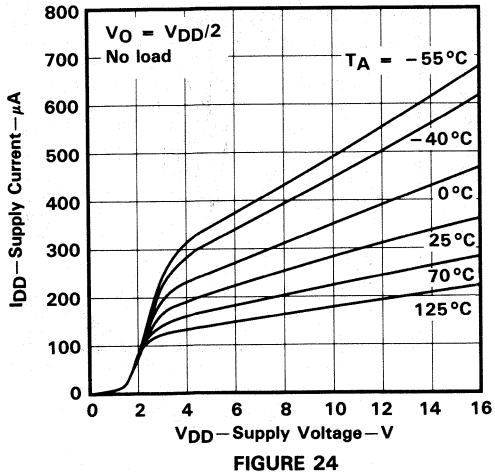


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

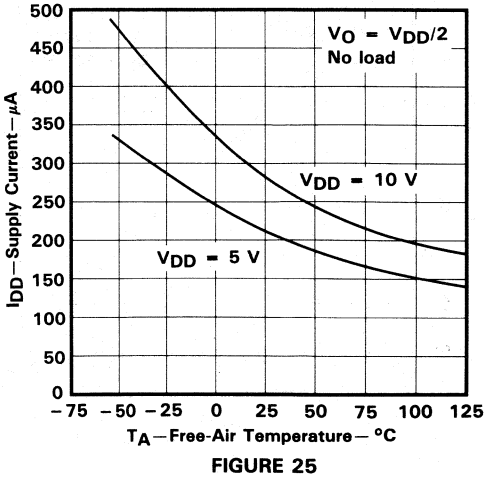


FIGURE 25

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
OTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

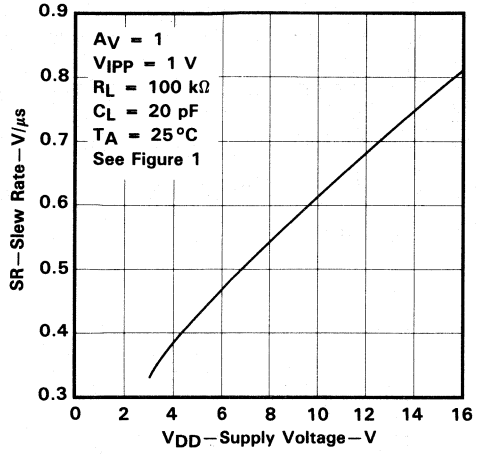


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

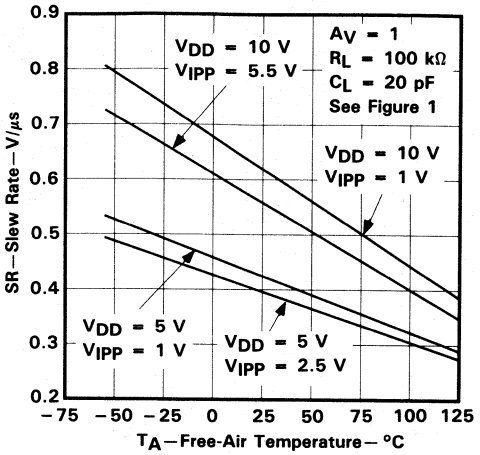


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

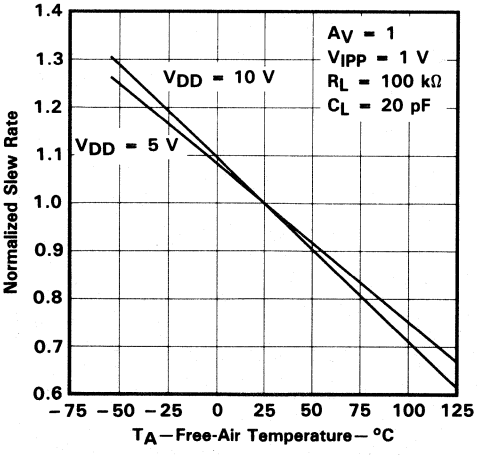


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

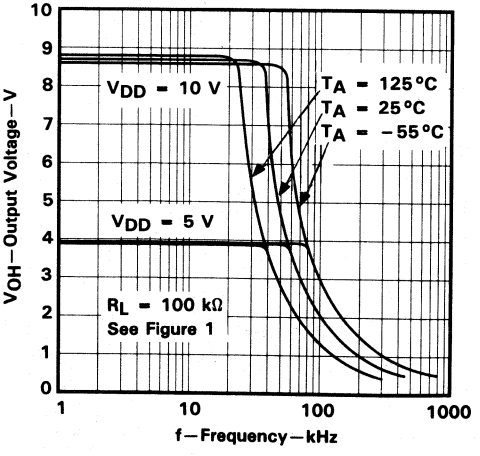


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

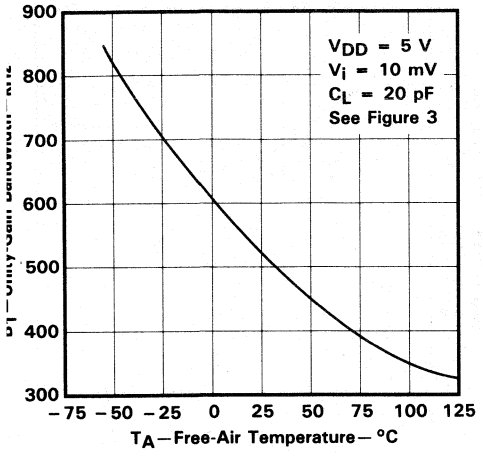


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

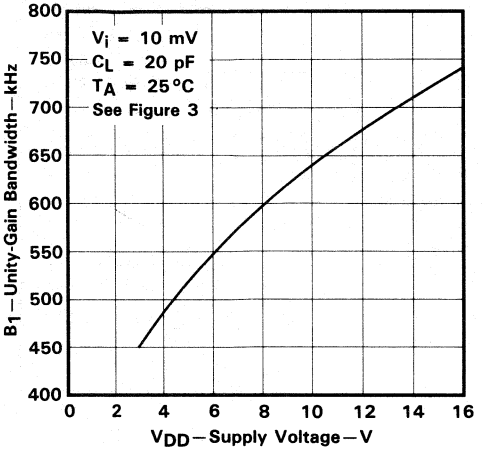


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

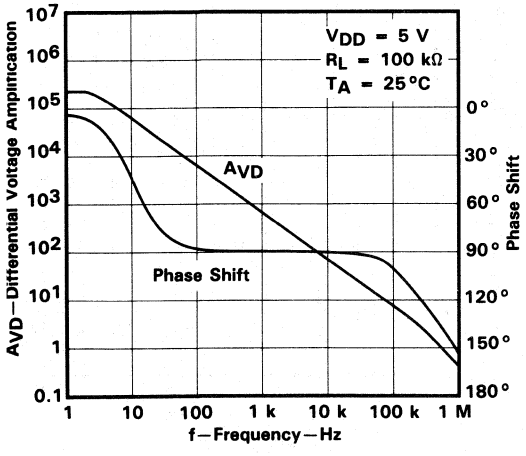


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

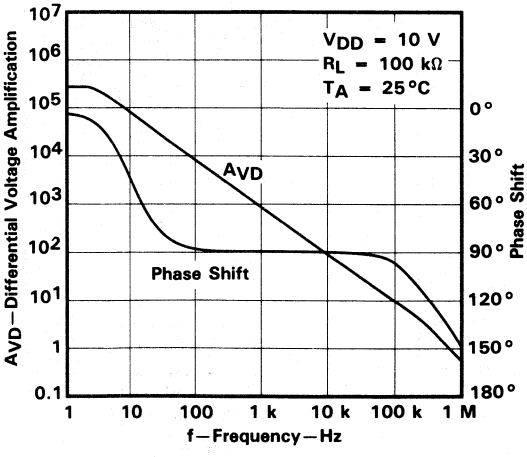


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

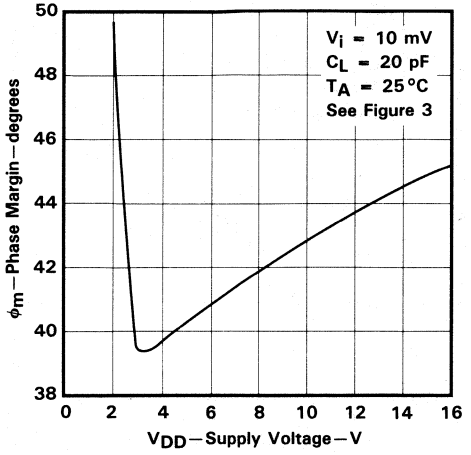


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

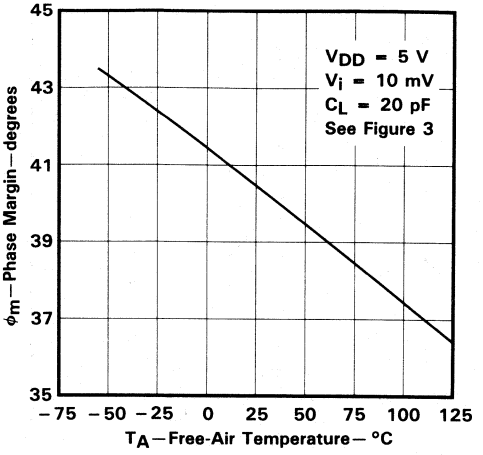


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

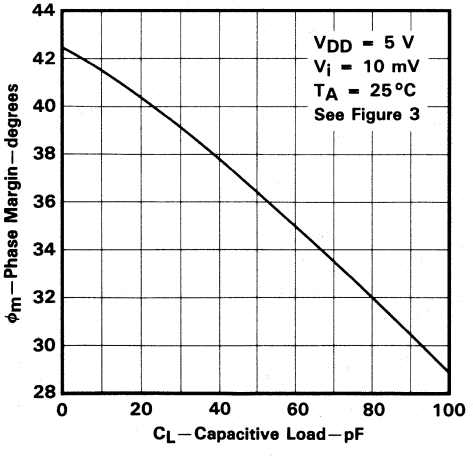


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

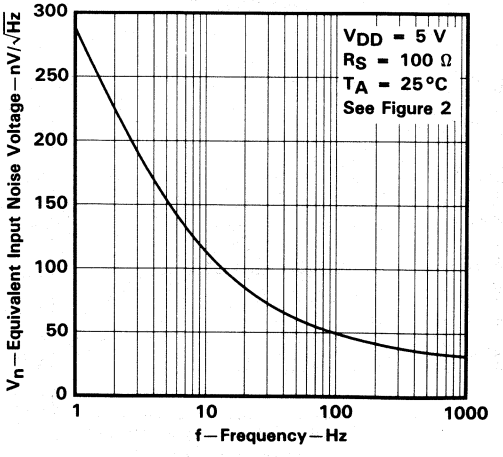


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

single-supply operation

While the TLC27M2 and TLC27M7 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M2 and TLC27M7 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M2 and TLC27M7 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

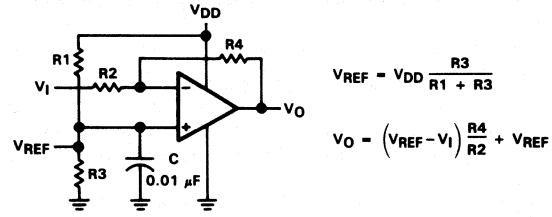
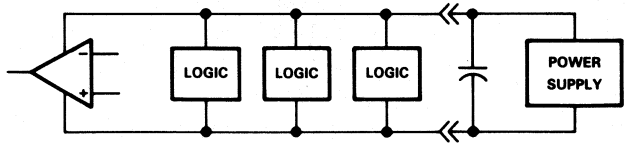
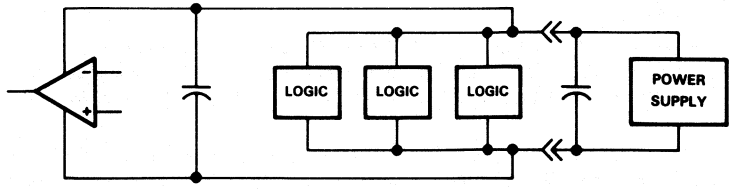


FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M2 and TLC27M7 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at T_A = 25°C and at $V_{DD}-1.5$ V at all other temperatures.

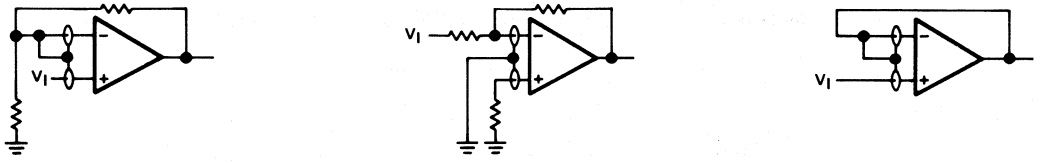
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M2 and TLC27M7 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M2 and TLC27M7 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M2 and TLC27M7 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27M2 and TLC27M7 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M2 and TLC27M7 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

TYPICAL APPLICATION DATA

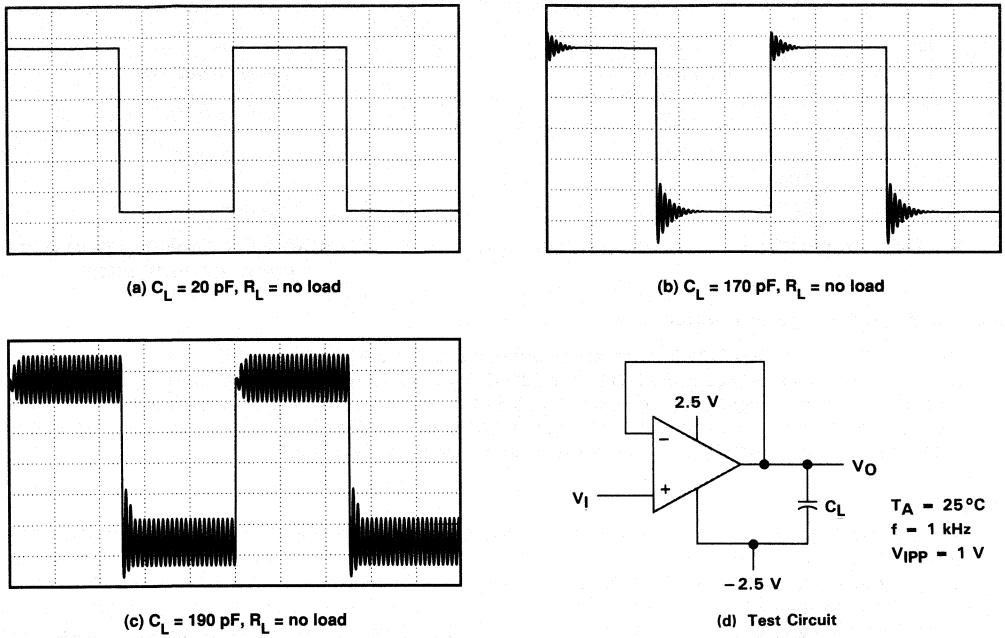


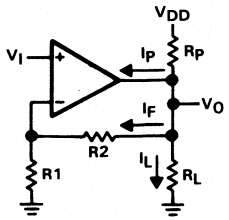
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M2 and TLC27M7 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

feedback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

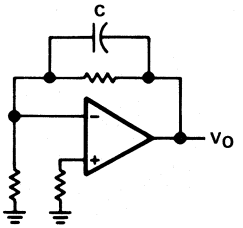


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27M2 and TLC27M7 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices, as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M2 and TLC27M7 inputs and outputs were designed to withstand −100-mA surge currents without sustaining latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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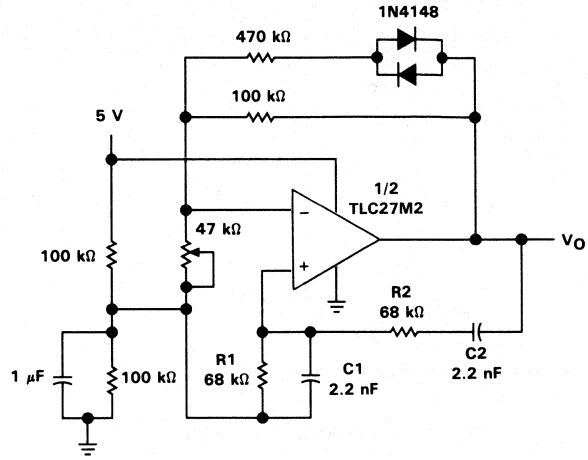
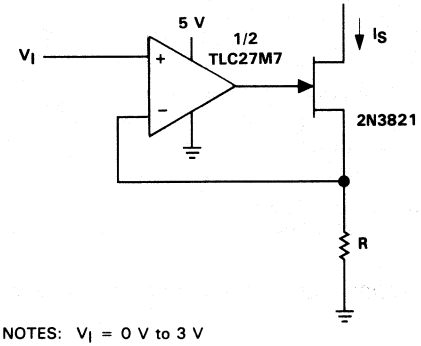
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

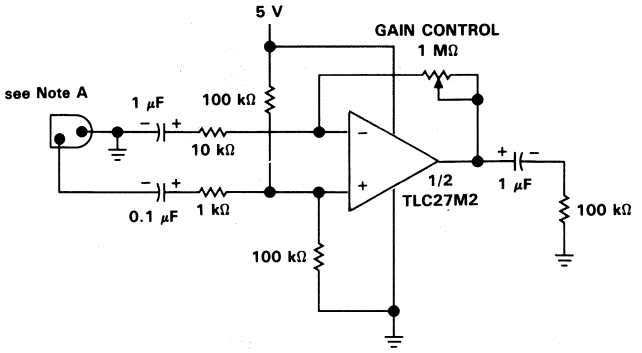


NOTES: $V_I = 0$ V to 3 V

$$I_S = \frac{V_I}{R}$$

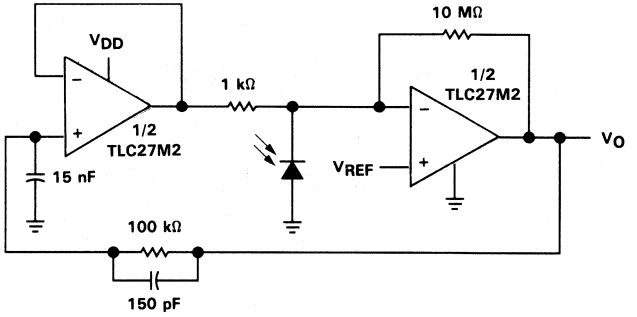
FIGURE 45. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A.: Low to medium impedance dynamic mike

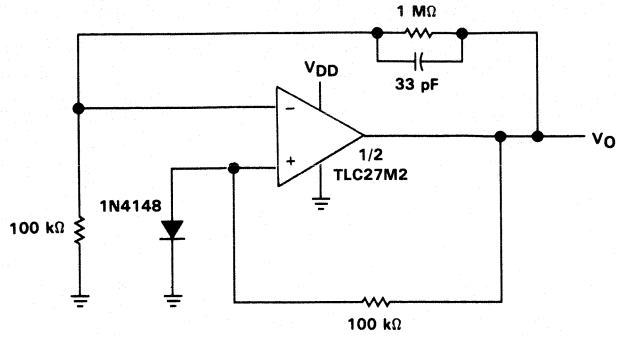
FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

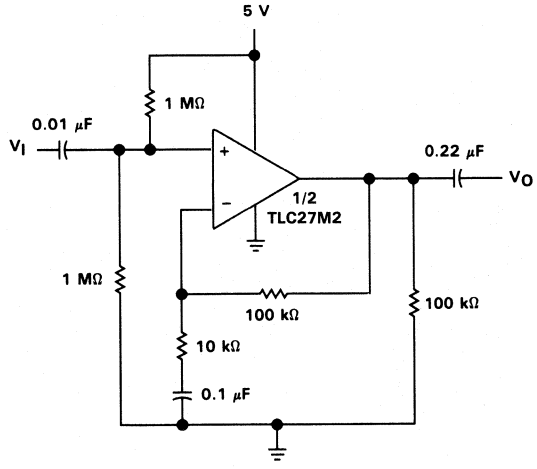
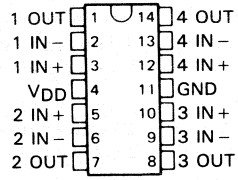


FIGURE 49. SINGLE-RAIL AC AMPLIFIER

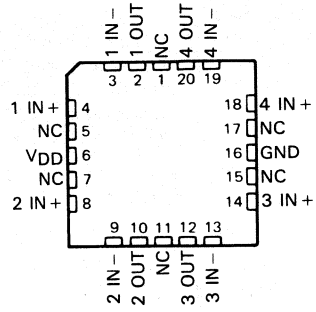
D3143, OCTOBER 1987—REVISED AUGUST 1988

- **Trimmed Offset Voltage:**
  TLC27M9 . . . 900 μV Max at 25 °C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages over Specified Temperature Range:**
  −55°C to 125°C . . . 4 V to 16 V
  −40°C to 85°C . . . 4 V to 16 V
  0°C to 70°C . . . 3 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix Types)**
- **Low Noise . . . Typically 32 nV/$\sqrt{Hz}$ at f = 1 kHz**
- **Low Power . . . Typically 2.1 mW at 25°C, V_{DD} = 5 V**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latchup Immunity**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



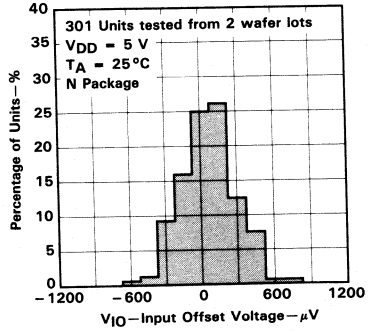
NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	900 μV	TLC27M9CD	—	TLC27M9CJ	TLC27M9CN
	2 mV	TLC27M4BCD	—	TLC27M4BCJ	TLC27M4BCN
	5 mV	TLC27M4ACD	—	TLC27M4ACJ	TLC27M4ACN
	10 mV	TLC27M4CD	—	TLC27M4CJ	TLC27M4CN
−40°C to 85°C	900 μV	TLC27M9ID	—	TLC27M9IJ	TLC27M9IN
	2 mV	TLC27M4BID	—	TLC27M4BIJ	TLC27M4BIN
	5 mV	TLC27M4AID	—	TLC27M4AIJ	TLC27M4AIN
	10 mV	TLC27M4ID	—	TLC27M4IJ	TLC27M4IN
−55°C to 125°C	900 μV	—	TLC27M9MFK	TLC27M9MJ	—
	10 mV	—	TLC27M4MFK	TLC27M4MJ	—

The D package is available in tape and reel. Add R suffix to the device type (e.g., TLC27M9CDR).

DISTRIBUTION OF TLC27M9
INPUT OFFSET VOLTAGE



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description

The TLC27M4 and TLC27M9 quad operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds comparable to that of general-purpose bipolar devices. These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance and low bias currents make these cost-effective devices ideal for applications that have previously been reserved for general-purpose bipolar products, but with only a fraction of the power consumption. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27M4 (10 mV) to the high-precision TLC27M9 (900 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC27M4 and TLC27M9. The devices also exhibit low voltage single-supply operation and low power consumption, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand −100-mA surge currents without sustaining latchup.

The TLC27M4 and TLC27M9 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

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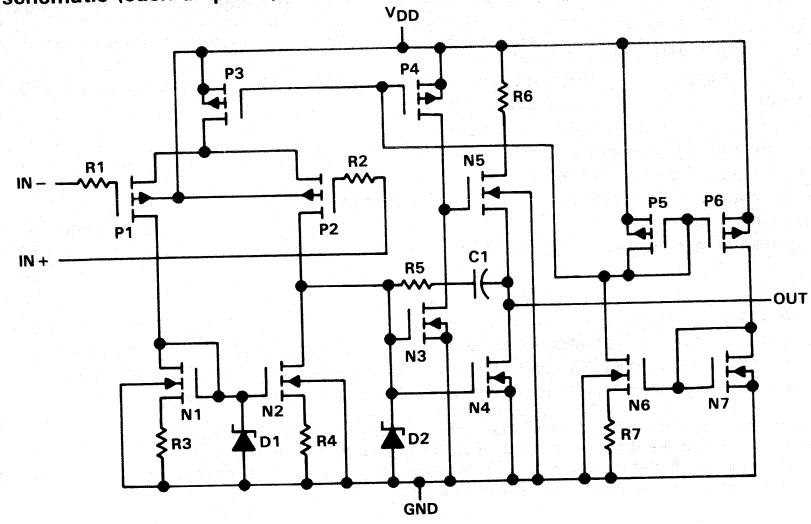
quivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal . . . . . 45 mA
Total current out of ground terminal . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D and N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (M-suffix)	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J (C-, I-suffix)	1025 mW	8.2 mW/°C	656 mW	533 mW	
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	4		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	−0.2		3.5	−0.2		3.5	V
	V_{DD} = 10 V	0		8.5	−0.2		8.5	−0.2		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	μV
					Full range			3750	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					125°C		1.4	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					125°C		9	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 4	−0.3 to 4.2		V
					Full range	0 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					−55°C	3	3.9		
					125°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					−55°C	15	290		
					125°C	15	120		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					−55°C	60	89		
					125°C	60	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	μA
					−55°C		680	1760	
					125°C		280	720	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M9M	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	μV
					Full range			4300	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 125°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					125°C		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					125°C		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	0 to 9	−0.3 to 9.2		V
					Full range	0 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−55°C	7.8	8.6		
					125°C	7.8	8.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−55°C		0	50	
					125°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−55°C	15	420		
					125°C	15	190		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−55°C	60	93		
					125°C	60	93		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−55°C	60	91		
					125°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	μA
					−55°C		980	2000	
					125°C		360	960	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
				Full range			13	
	TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
				Full range			7	
	TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	μV
				Full range			3500	
	TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
				Full range			2000	
α_{VIO} Average temperature coefficient of input offset voltage				25°C to 85°C		1.7		μV/°C
I_{IO} Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
				85°C		24	1000	
I_{IB} Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
				85°C		200	2000	
V_{ICR} Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
				Full range	−0.2 to 3.5			V
V_{OH} High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
				−40°C	3	3.9		
				85°C	3	4		
V_{OL} Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
				−40°C		0	50	
				85°C		0	50	
A_{VD} Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
				−40°C	15	270		
				85°C	15	130		
CMRR Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
				−40°C	60	90		
				85°C	60	90		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
				−40°C	60	91		
				85°C	60	94		
I_{DD} Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	μA
				−40°C		630	1600	
				85°C		320	800	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			13	
		TLC27M4AI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			7	
		TLC27M4BI	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	μV
					Full range			3500	
		TLC27M9I	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	
					Full range			2900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 85°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					85°C		26	1000	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					85°C		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					−40°C	7.8	8.7		
					85°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					−40°C		0	50	
					85°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					−40°C	15	390		
					85°C	15	220		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					−40°C	60	93		
					85°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					−40°C	60	91		
					85°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	μA
					−40°C		900	1800	
					85°C		410	1040	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		250	2000	μV
					Full range			3000	
		TLC27M9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		210	900	
					Full range			1500	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		1.7		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.6		pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	3.2	3.9		V
					0°C	3	3.9		
					70°C	3	4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 100 kΩ	25°C	25	170		V/mV
					0°C	15	200		
					70°C	15	140		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	91		dB
					0°C	60	91		
					70°C	60	92		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 2.5 V, No load	V_{IC} = 2.5 V,	25°C		420	1120	μA
					0°C		500	1280	
					70°C		340	880	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLC27M4C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC27M4AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC27M4BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		260	2000	μV
					Full range			3000	
		TLC27M9C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 100 kΩ	25°C		220	1200	
					Full range			1900	
α_{VIO}	Average temperature coefficient of input offset voltage				25°C to 70°C		2.1		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1		pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.7		pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 100 kΩ	25°C	8	8.7		V
					0°C	7.8	8.7		
					70°C	7.8	8.7		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 100 kΩ	25°C	25	275		V/mV
					0°C	15	320		
					70°C	15	230		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR} min		25°C	65	94		dB
					0°C	60	94		
					70°C	60	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	70	93		dB
					0°C	60	92		
					70°C	60	94		
I_{DD}	Supply current (four amplifiers)		V_O = 5 V, No load	V_{IC} = 5 V,	25°C		570	1200	μA
					0°C		690	1600	
					70°C		440	1120	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−55°C		0.54		
				125°C		0.29		
			V_{IPP} = 2.5 V	25°C		0.40		
				−55°C		0.50		
				125°C		0.28		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−55°C		80		
				125°C		40		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−55°C		850		
				125°C		330		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−55°C		44°		
				125°C		36°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−55°C		0.81		
				125°C		0.38		
			V_{IPP} = 5.5 V	25°C		0.56		
				−55°C		0.73		
				125°C		0.35		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−55°C		50		
				125°C		20		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−55°C		960		
				125°C		440		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−55°C		47°		
				125°C		39°		

operating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				−40°C		0.51		
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				−40°C		0.48		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				−40°C		75		
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				−40°C		770		
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				−40°C		43°		
				85°C		38°		

operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				−40°C		0.77		
				85°C		0.47		
			V_{IPP} = 5.5 V	25°C		0.56		
				−40°C		0.70		
				85°C		0.44		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				−40°C		45		
				85°C		25		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				−40°C		880		
				85°C		480		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				−40°C		46°		
				85°C		41°		

perating characteristics, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.43		V/μs
				0°C		0.46		
				70°C		0.36		
			V_{IPP} = 2.5 V	25°C		0.40		
				0°C		0.43		
				70°C		0.34		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		55		kHz
				0°C		60		
				70°C		50		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		525		kHz
				0°C		610		
				70°C		400		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		40°		
				0°C		41°		
				70°C		39°		

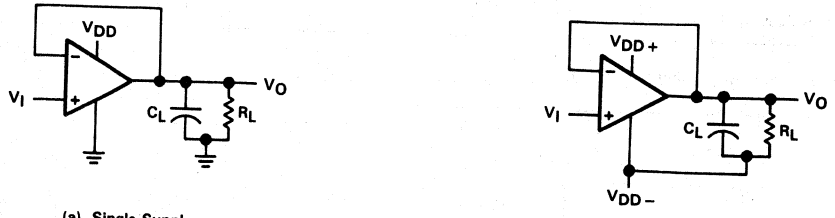
operating characteristics, V_{DD} = 10 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 100 kΩ, C_L = 20 pF, See Figure 1	V_{IPP} = 1 V	25°C		0.62		V/μs
				0°C		0.67		
				70°C		0.51		
			V_{IPP} = 5.5 V	25°C		0.56		
				0°C		0.61		
				70°C		0.46		
V_n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	R_S = 100 Ω,	25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, R_L = 100 kΩ,	C_L = 20 pF, See Figure 1	25°C		35		kHz
				0°C		40		
				70°C		30		
B_1	Unity-gain bandwidth	V_i = 10 mV, See Figure 3	C_L = 20 pF,	25°C		635		kHz
				0°C		710		
				70°C		510		
ϕ_m	Phase margin	V_i = 10 mV, C_L = 20 pF,	f = B_1, See Figure 3	25°C		43°		
				0°C		44°		
				70°C		42°		

PARAMETER MEASUREMENT INFORMATION

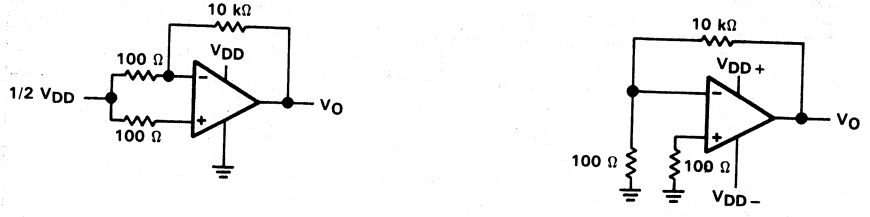
single-supply versus split-supply test circuits

Because the TLC27M4 and TLC27M9 are optimized for single-supply operation, circuit configurations use for the various tests often present some inconvenience since the input signal, in many cases, must b offset from ground. This inconvenience can be avoided by testing the device with split supplies and th output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is show below. The use of either circuit will give the same result.



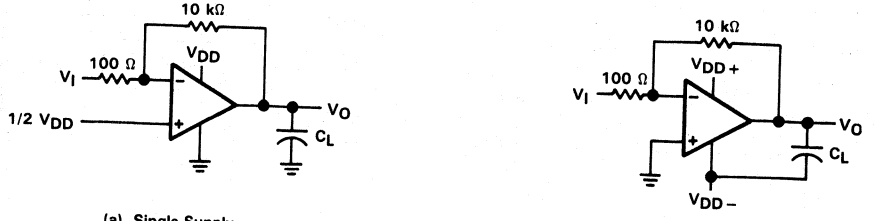
(a) Single-Supply (b) Split-Supply

FIGURE 1. UNITY-GAIN AMPLIFIER



(a) Single-Supply (b) Split-Supply

FIGURE 2. NOISE TEST CIRCUIT



(a) Single-Supply (b) Split-Supply

FIGURE 3. GAIN-OF-100 INVERTING AMPLIFIER

PARAMETER MEASUREMENT INFORMATION

ıput bias current

Because of the high input impedance of the TLC27M4 and TLC27M9 op amps, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the "open-socket" leakage readings from the readings obtained with a device in the test socket.

   One word of caution . . . many automatic testers as well as some bench-top op amp testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an "open-socket" reading is not feasible using this method.

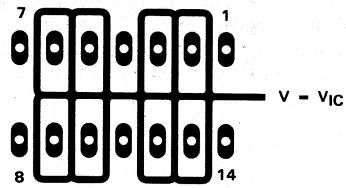


FIGURE 4. ISOLATION METAL AROUND DEVICE INPUTS (J AND N DUAL-IN-LINE-PACKAGE)

ɔw-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

PARAMETER MEASUREMENT INFORMATION

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage This parameter is actually a calculation using input offset voltage measurements obtained at two differen temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect or the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full-power response

Full-power response, the frequency above which the op amp slew rate limits the output voltage swing is often specified two ways . . . full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significan distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for "significant" distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude o the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak outpu can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determinatior of the point at which the maximum peak-to-peak output is reached.

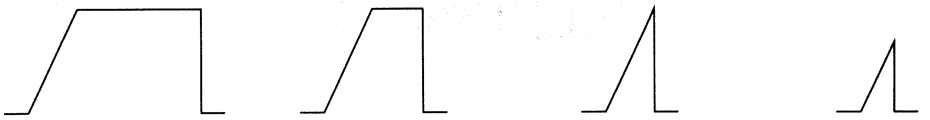


FIGURE 5. FULL-POWER-RESPONSE OUTPUT SIGNAL

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

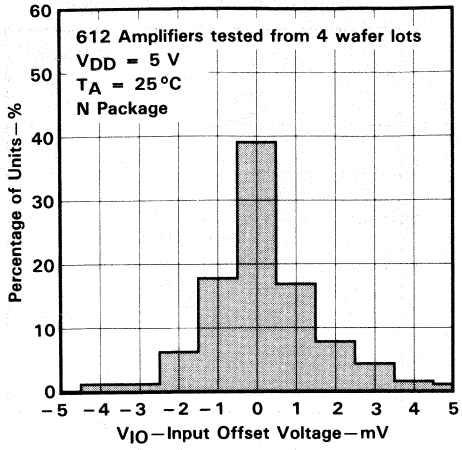


FIGURE 6

DISTRIBUTION OF TLC27M4
INPUT OFFSET VOLTAGE

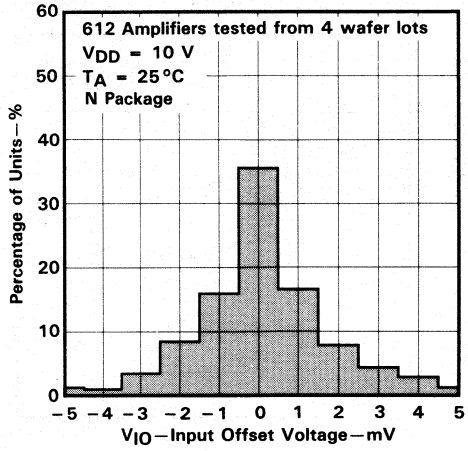


FIGURE 7

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

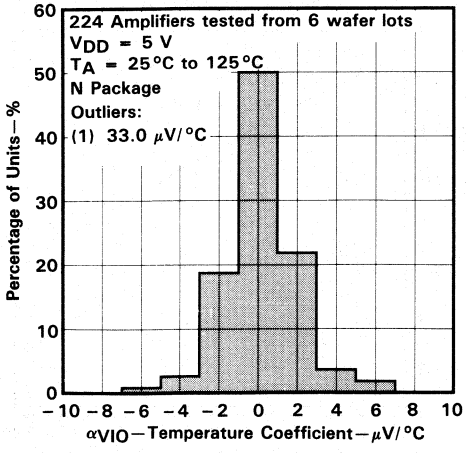


FIGURE 8

DISTRIBUTION OF TLC27M4 AND TLC27M9
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

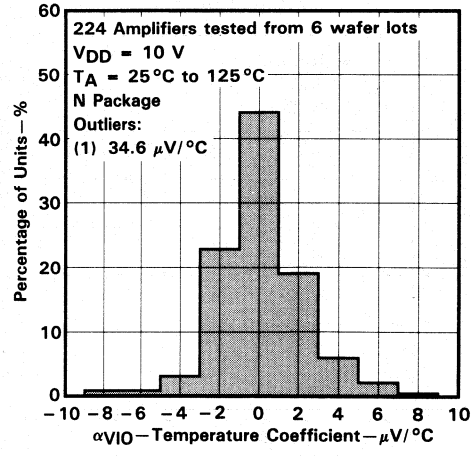


FIGURE 9

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

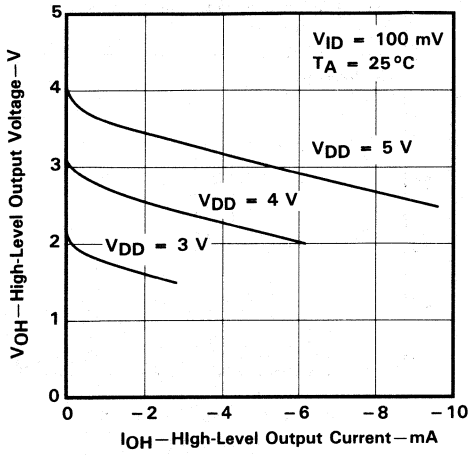


FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

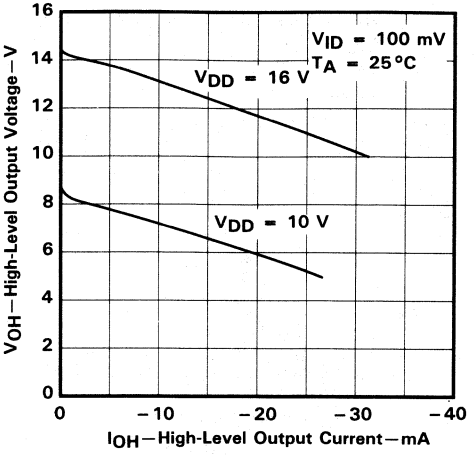


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

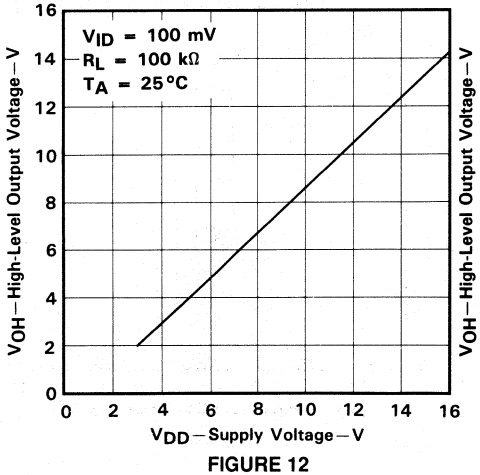


FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

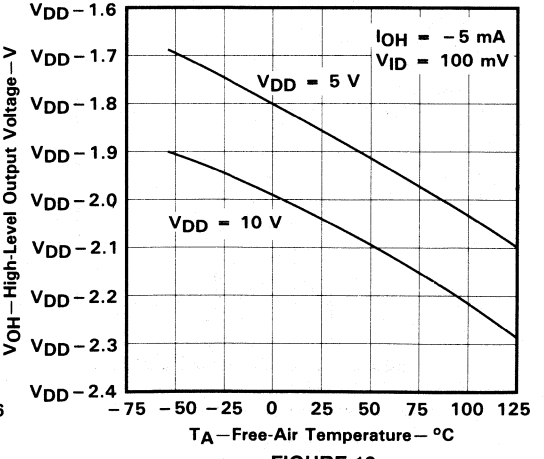


FIGURE 13

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

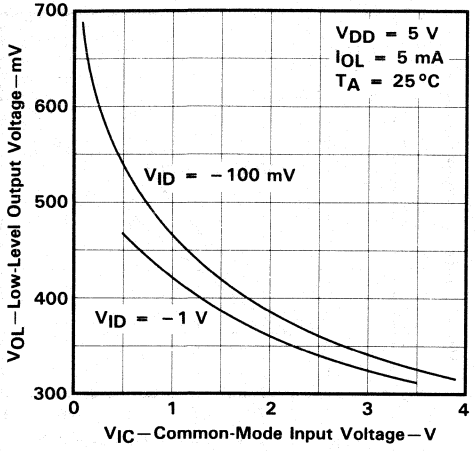


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

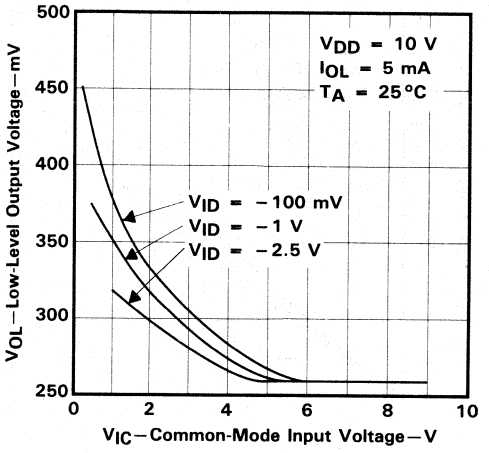


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

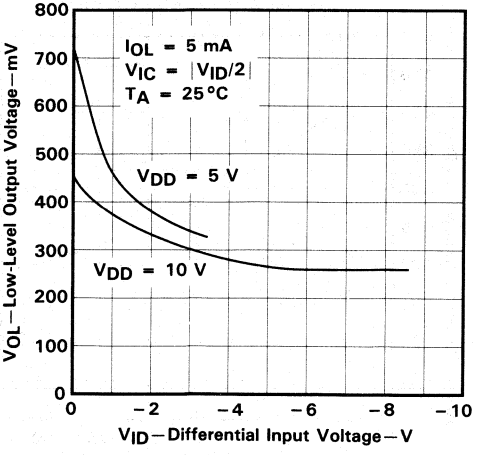


FIGURE 16

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

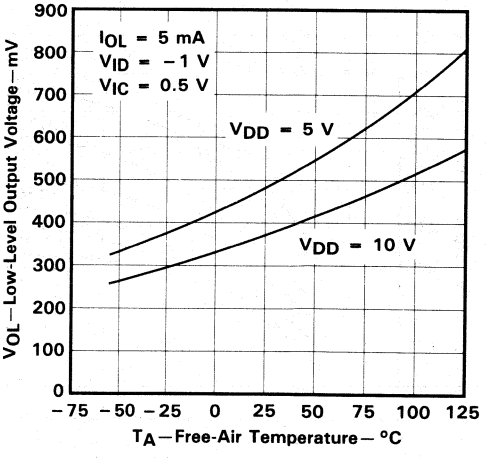


FIGURE 17

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

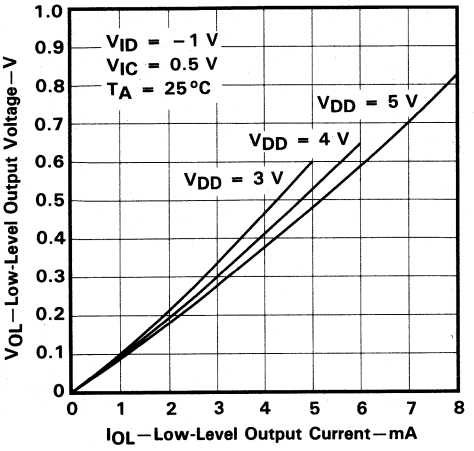


FIGURE 18

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

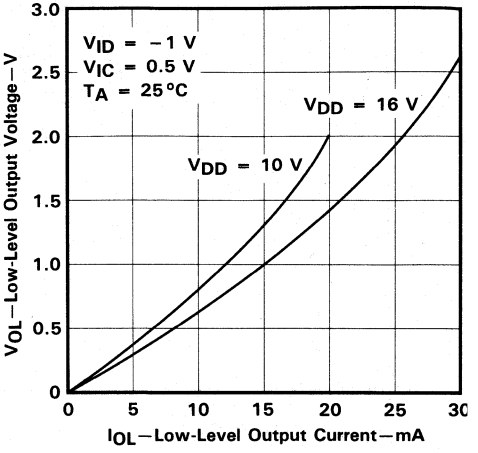


FIGURE 19

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

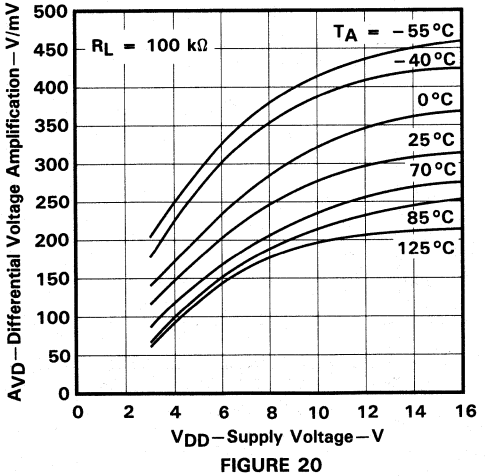


FIGURE 20

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

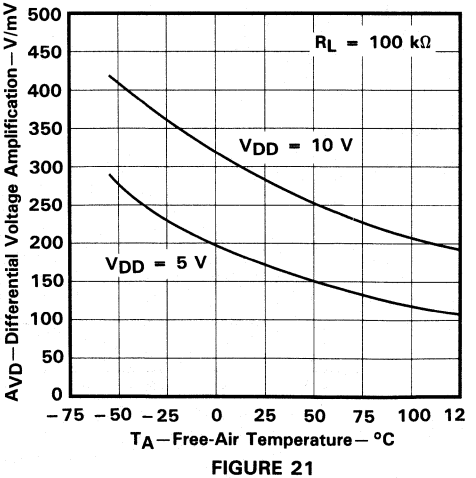


FIGURE 21

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

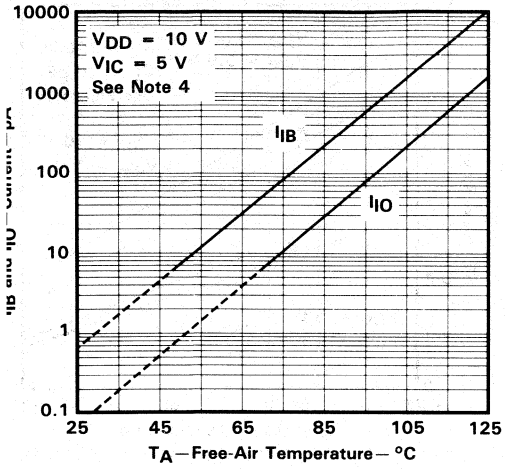


FIGURE 22

COMMON-MODE
INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

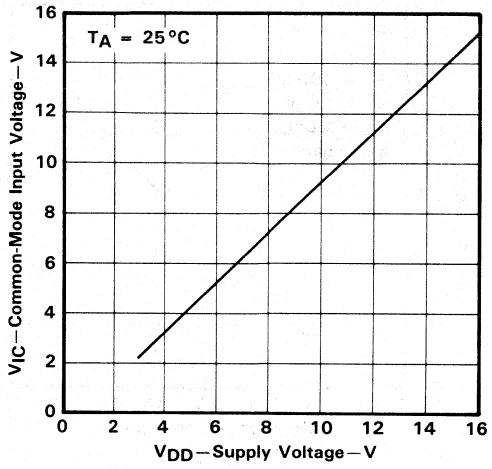


FIGURE 23

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

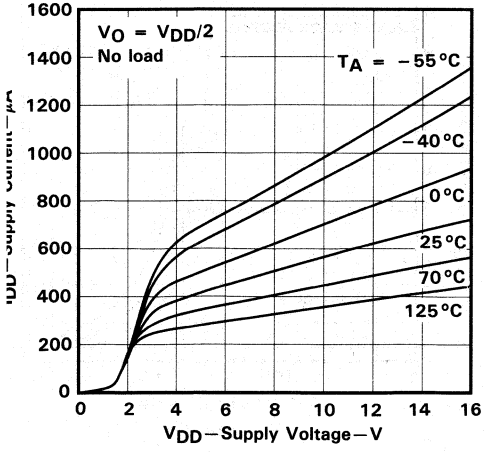


FIGURE 24

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

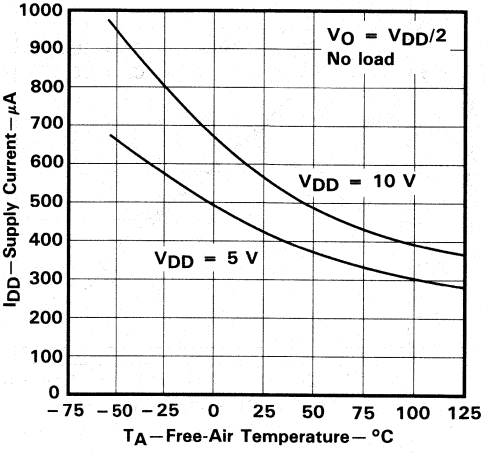


FIGURE 25

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

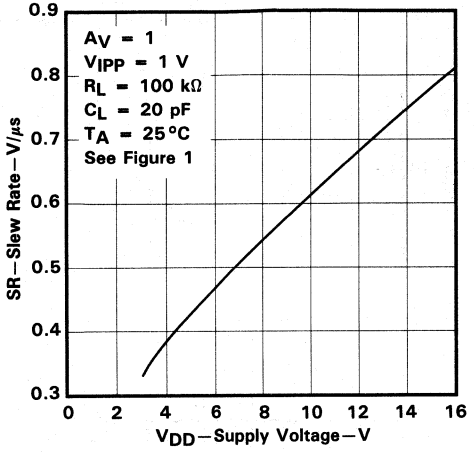


FIGURE 26

SLEW RATE
vs
FREE-AIR TEMPERATURE

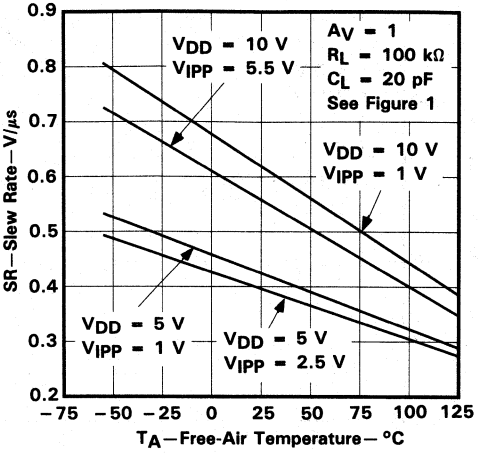


FIGURE 27

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

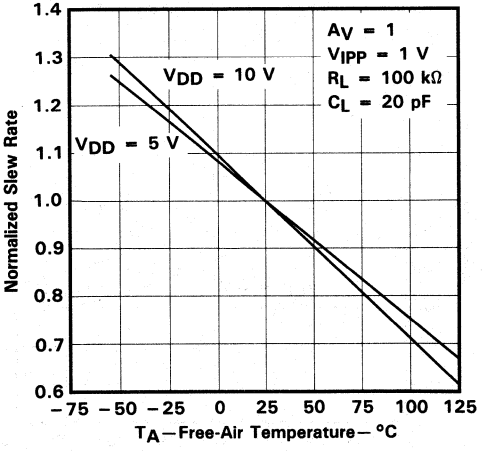


FIGURE 28

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

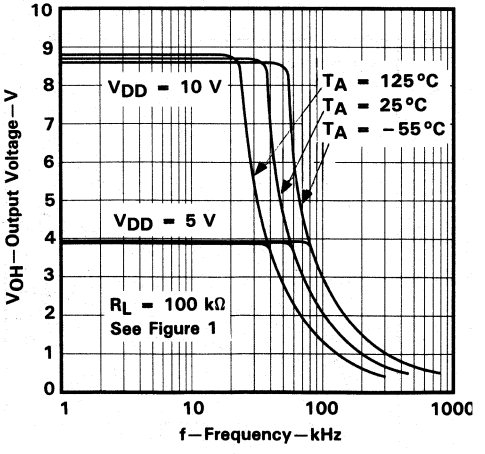


FIGURE 29

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

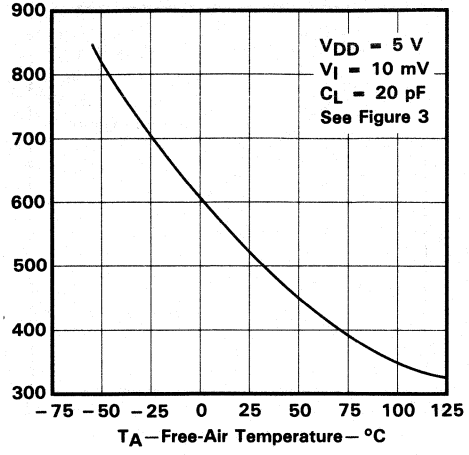


FIGURE 30

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

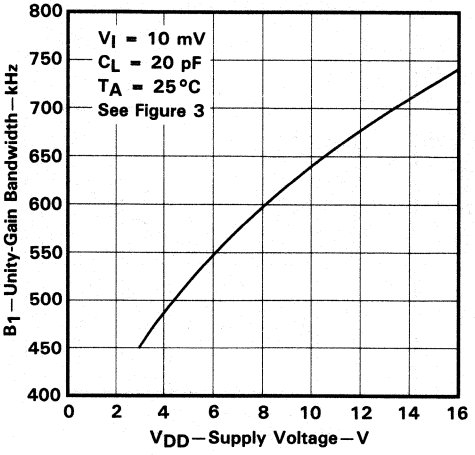


FIGURE 31

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

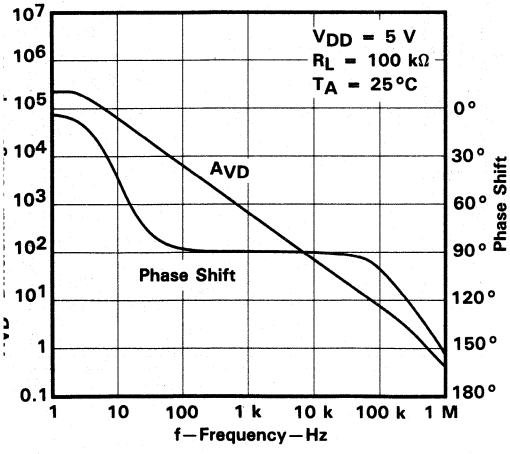


FIGURE 32

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

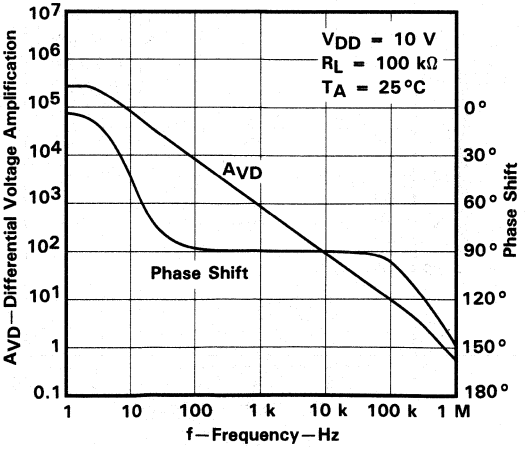


FIGURE 33

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

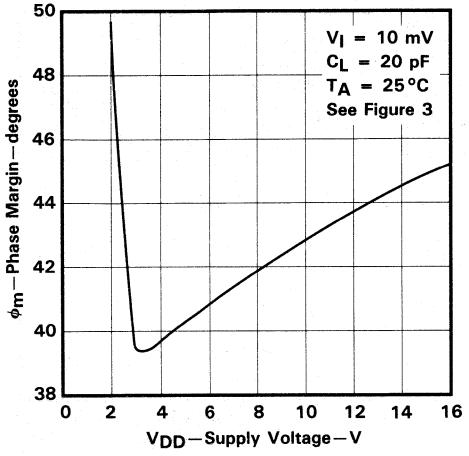


FIGURE 34

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

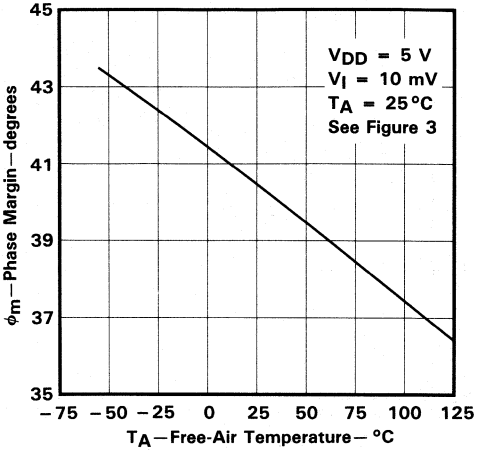


FIGURE 35

PHASE MARGIN
vs
CAPACITIVE LOAD

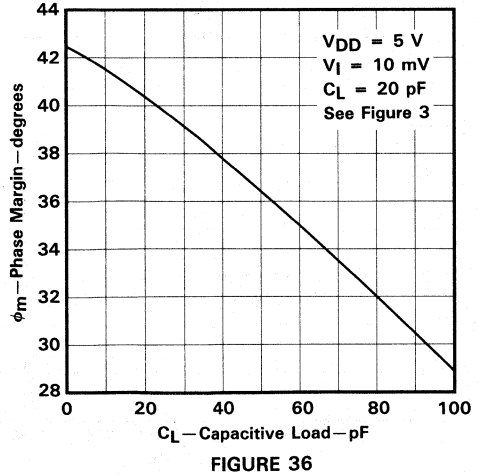


FIGURE 36

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

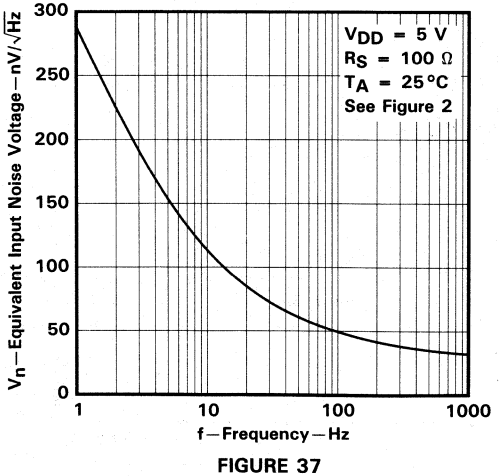


FIGURE 37

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

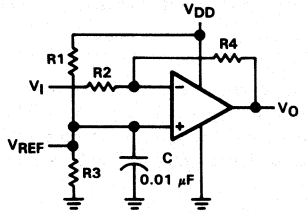
single-supply operation

While the TLC27M4 and TLC27M9 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC27M4 and TLC27M9 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27M4 and TLC27M9 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

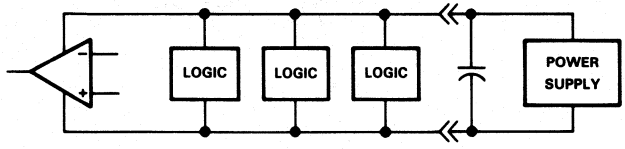
1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.



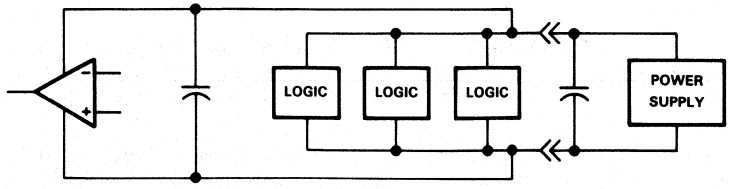
$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

$$V_O = \left(V_{REF} - V_I\right)\frac{R4}{R2} + V_{REF}$$

FIGURE 38. INVERTING AMPLIFIER WITH VOLTAGE REFERENCE



(a) Common Supply Rails



(b) Separate Bypassed Supply Rails (preferred)

FIGURE 39. COMMON VS SEPARATE SUPPLY RAILS

TYPICAL APPLICATION DATA

input characteristics

The TLC27M4 and TLC27M9 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.5$ V at all other temperatures.

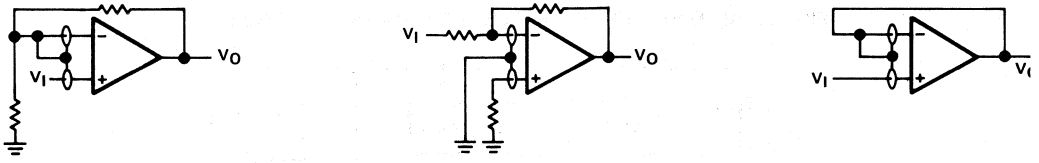
The use of the polysilicon-gate process and the careful input circuit design gives the TLC27M4 and TLC27M9 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC27M4 and TLC27M9 are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

noise performance

The noise specifications in op amp circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC27M4 and TLC27M9 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.



(a) Noninverting Amplifier (b) Inverting Amplifier (c) Unity-Gain Amplifier

FIGURE 40. GUARD-RING SCHEMES

output characteristics

The output stage of the TLC27M4 and TLC27M9 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC27M4 and TLC27M9 were measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance will alleviate the problem.

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TYPICAL APPLICATION DATA

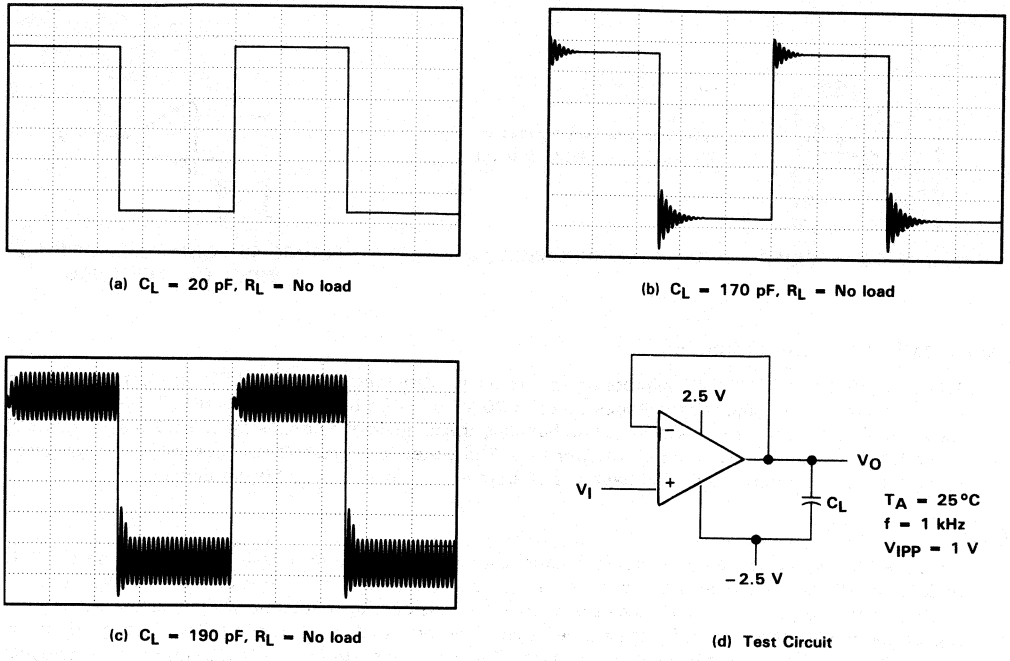


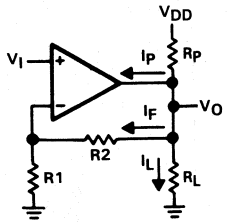
FIGURE 41. EFFECT OF CAPACITIVE LOADS AND TEST CIRCUIT

Although the TLC27M4 and TLC27M9 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pull-down transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the op amp input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Second, pullup resistor R_P acts as a drain load to N4 and the gain of the op amp is reduced at output voltage levels where N5 is not supplying the output current.

edback

Op amp circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

TYPICAL APPLICATION DATA



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the op amp (typically 500 μA)

FIGURE 42. RESISTIVE PULLUP TO INCREASE V_{OH}

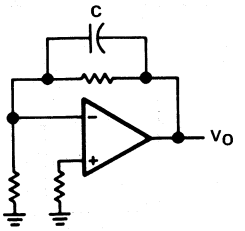


FIGURE 43. COMPENSATION FOR INPUT CAPACITANCE

electrostatic discharge protection

The TLC27M4 and TLC27M9 incorporate an internal electrostatic discharge (ESD) protection circuit tha prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2 Care should be exercised, however, when handling these devices as exposure to ESD may result in th degradation of the device parametric performance. The protection circuit also causes the input bias current to be temperature dependent and have the characteristics of a reverse-biased diode.

latchup

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC27M and TLC27M9 inputs and outputs were designed to withstand −100-mA surge currents without sustainin latchup; however, techniques should be used to reduce the chance of latchup whenever possible. Intern protection diodes should not, by design, be forward biased. Applied input and output voltage should nc exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive couplir on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typica located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the positive supply rail and ground ar can be triggered by surges on the supply lines and/or voltages on either the output or inputs that excee the supply voltage. Once latchup occurs, the current flow is limited only by the impedance of the pow supply and the forward resistance of the parasitic thyristor and usually results in the destruction of th device. The chance of latchup occurring increases with increasing temperature and supply voltages.

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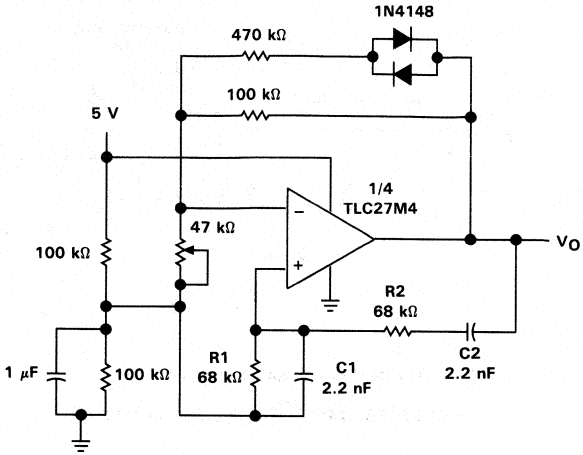
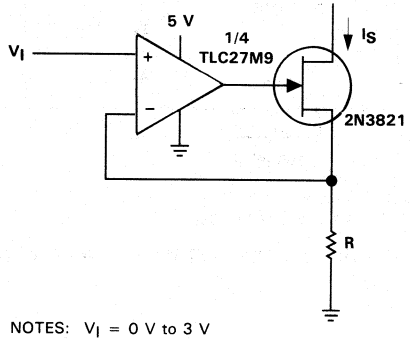
TYPICAL APPLICATION DATA



NOTES: $V_{OPP} \approx 2$ V

$$f_O = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

FIGURE 44. WIEN OSCILLATOR

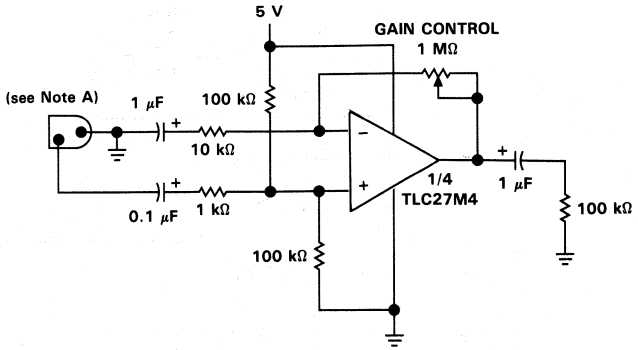


NOTES: $V_I = 0$ V to 3 V

$$I_S = \frac{V_I}{R}$$

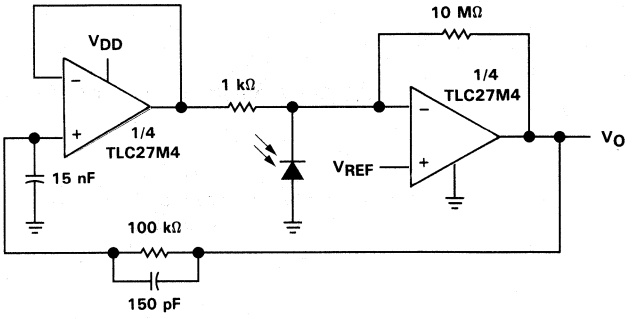
FIGURE 45. PRECISION LOW-CURRENT SINK

TYPICAL APPLICATION DATA



NOTE A: Low to medium impedance dynamic mike.

FIGURE 46. MICROPHONE PREAMPLIFIER



NOTES: V_{DD} = 4 V to 15 V
V_{REF} = 0 V to V_{DD} − 2 V

FIGURE 47. PHOTO DIODE AMPLIFIER WITH AMBIENT LIGHT REJECTION

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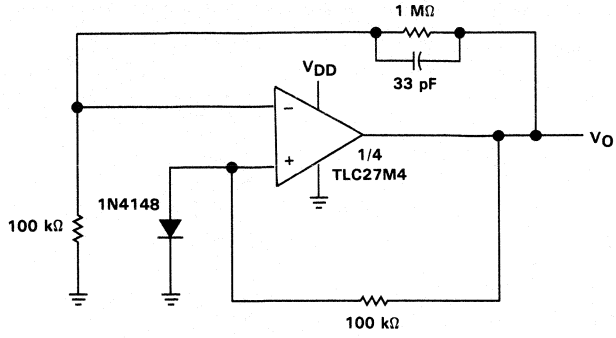
TYPICAL APPLICATION DATA



NOTES: V_{DD} = 8 V to 16 V
V_O = 5 V, 10 mA

FIGURE 48. 5-V LOW-POWER VOLTAGE REGULATOR

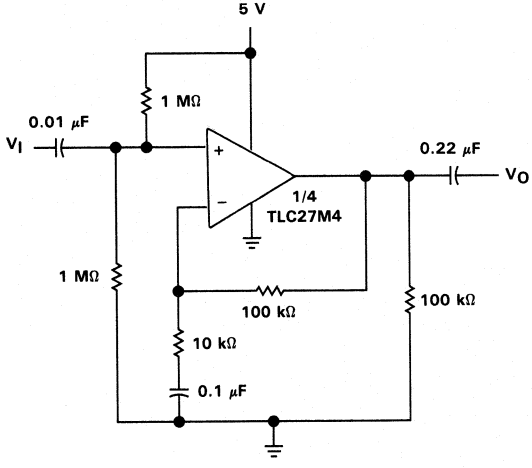


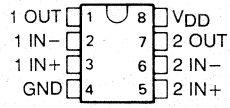
FIGURE 49. SINGLE-RAIL AC AMPLIFIER

2 Operational Amplifiers

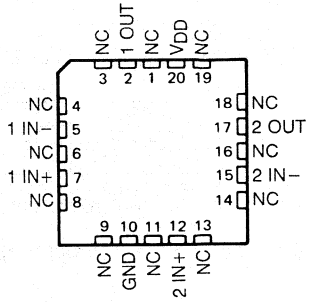
D3146, AUGUST 1988 – REVISED OCTOBER 1988

- **Power Dissipation as Low as 10 µW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 450 µV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 µV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**

D, JG, OR P PACKAGE
(TOP VIEW)

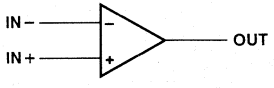


FK PACKAGE
(TOP VIEW)

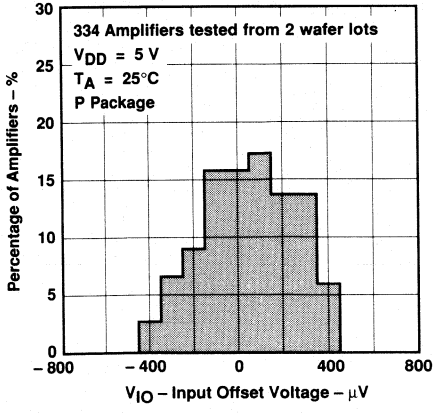


NC – No internal connection

symbol (each amplifier)



DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE



escription

The TLC1078 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-µW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1078C is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC1078 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L2 and TLC27L7, the TLC1078 easily upgrades existing designs that can benefit from its improved performance.

The TLC1078 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

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description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the devic parametric performance. The TLC1078 design also inhibits latchup of the device inputs and outputs even wit surge currents as large as 100 mA.

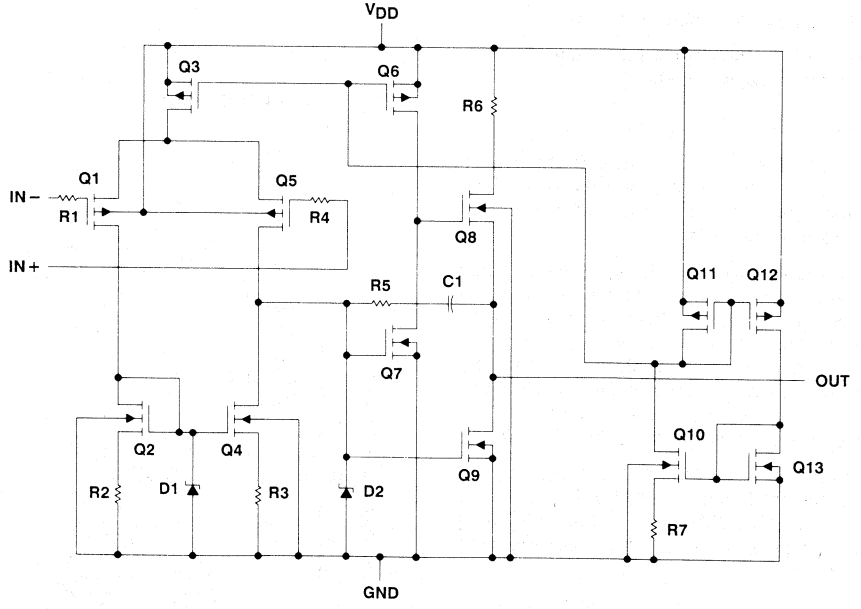
The M- suffix devices are characterized for operation over the full military temperature range of −55°C t 125°C. The I- suffix devices are characterized for operation from −40°C to 85°C. The C- suffix devices ar characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline an chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D) SEE NOTE 1	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1078CD	–	TLC1078CJG	TLC1078CP
−40°C to 85°C	TLC1078ID	–	TLC1078IJG	TLC1078IP
−55°C to 125°C	–	TLC1078MFK	TLC1078MJG	–

NOTE 1: The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Different input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal (see Note 4) . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		4	−0.2		4	−0.2		4	V
	V_{DD} = 10 V	0		9	−0.2		9	−0.2		9	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

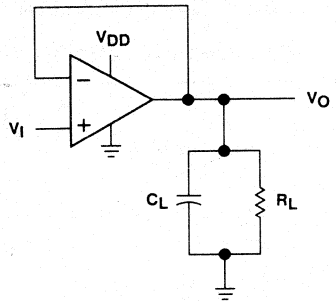
PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V,	25°C		160	450		180	600	μV
		R_S = 50 Ω, R_I = 1 MΩ	Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ See Note 7	25°C	250	525		500	850		V/mV
			0°C	250	680		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			0°C		24	42		36	66	
			70°C		16	28		22	40	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

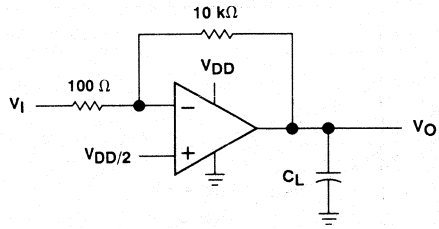
PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 10 V MIN	V_{DD} = 10 V TYP	V_{DD} = 10 V MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

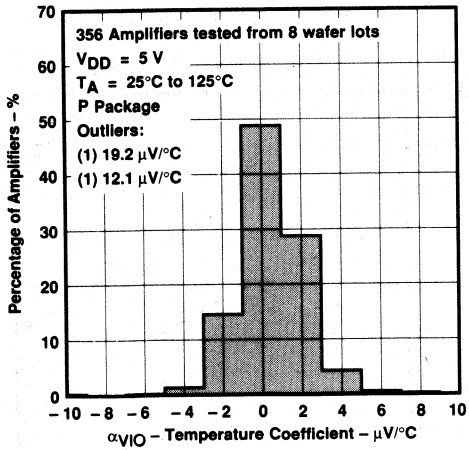


FIGURE 3

DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

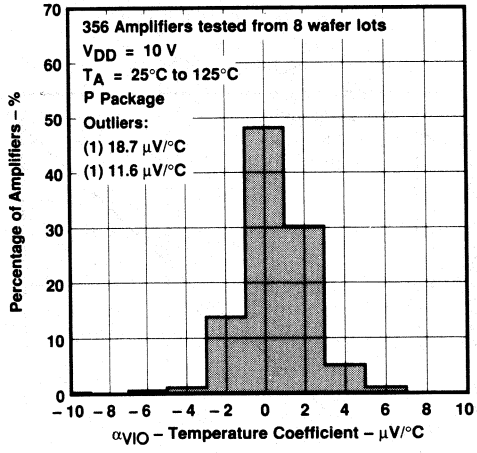


FIGURE 4

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

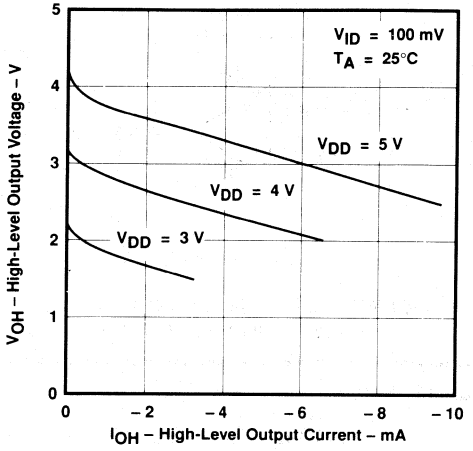


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

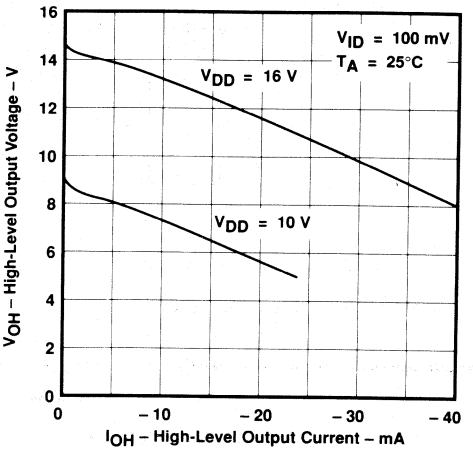


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

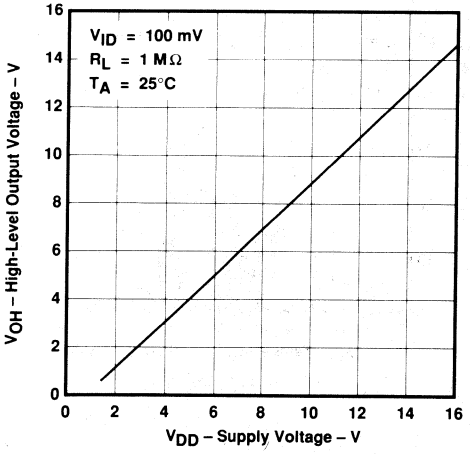


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

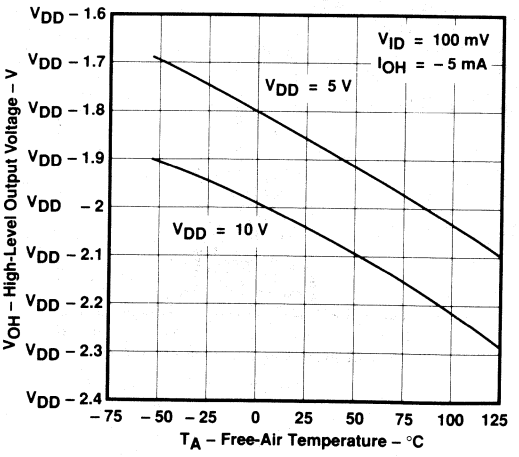


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

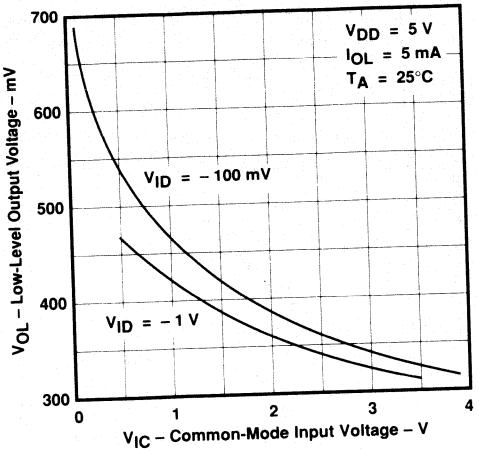


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

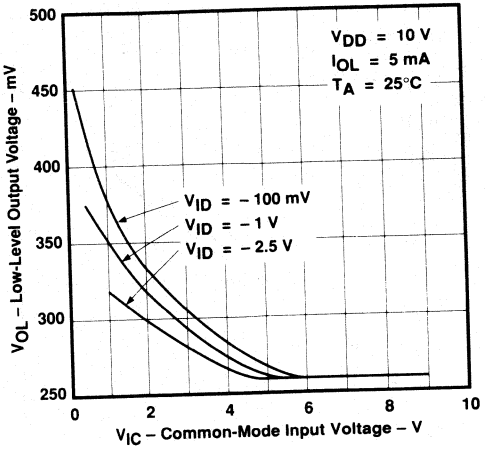


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

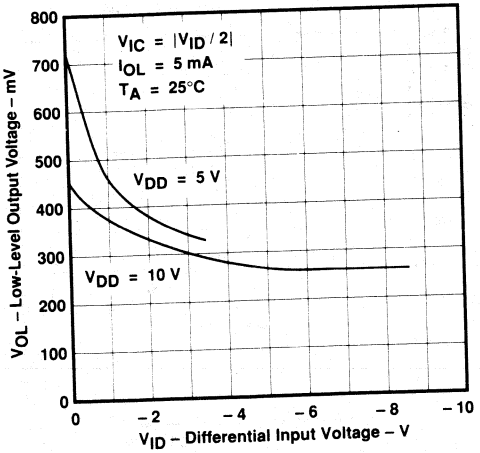


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

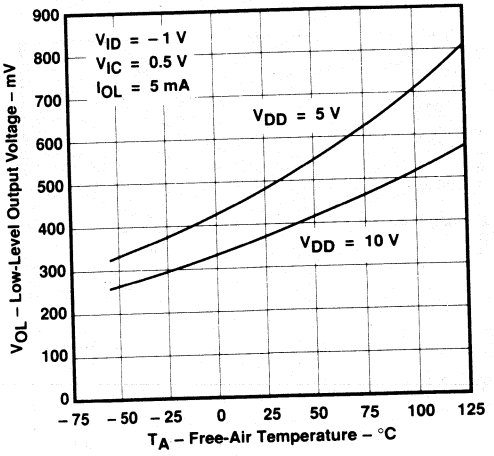


FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

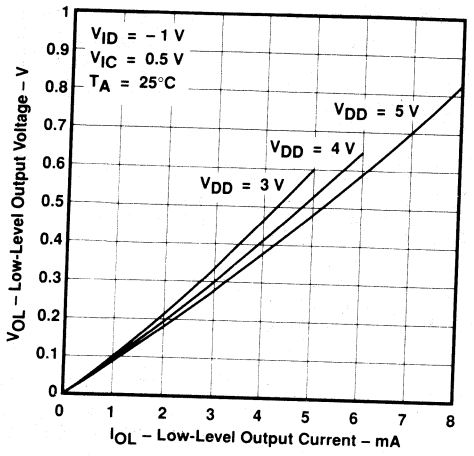


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

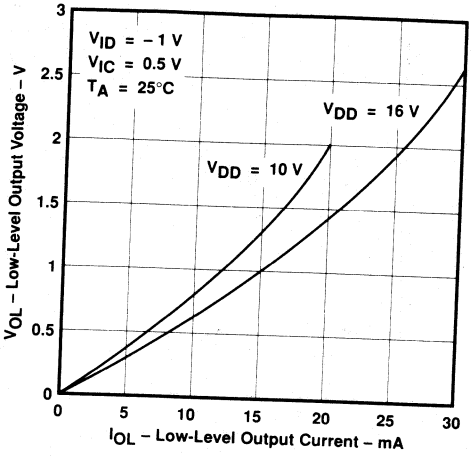


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

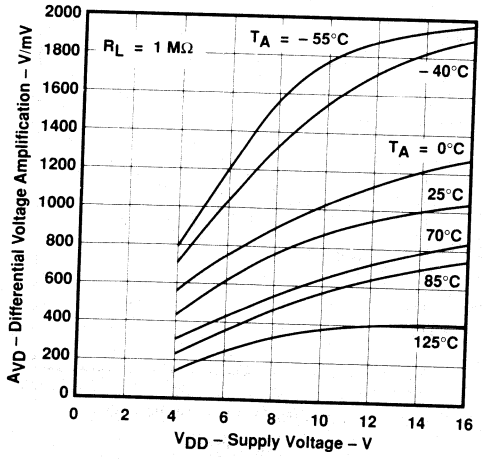


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

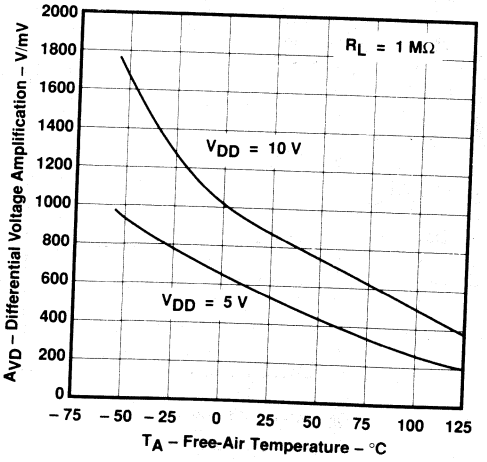


FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

NPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

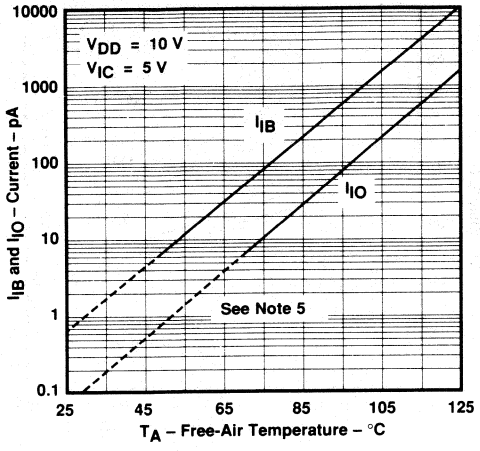


FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

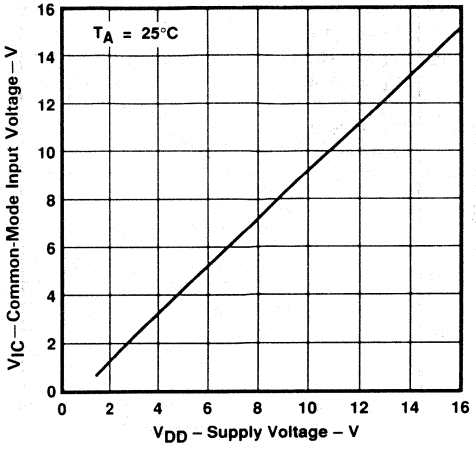


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

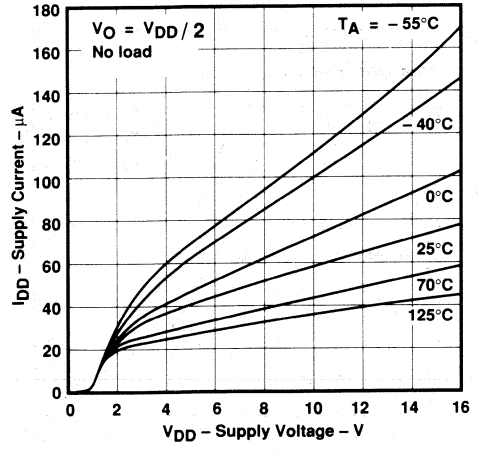


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

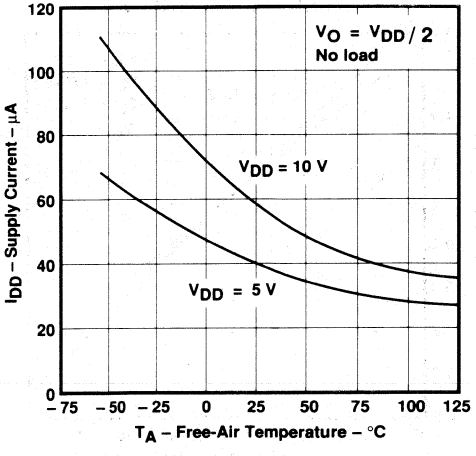


FIGURE 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathmatically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

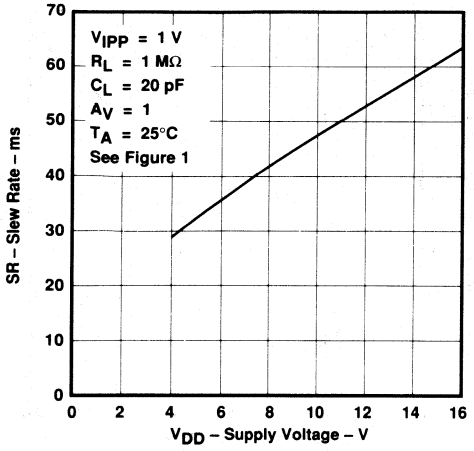


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

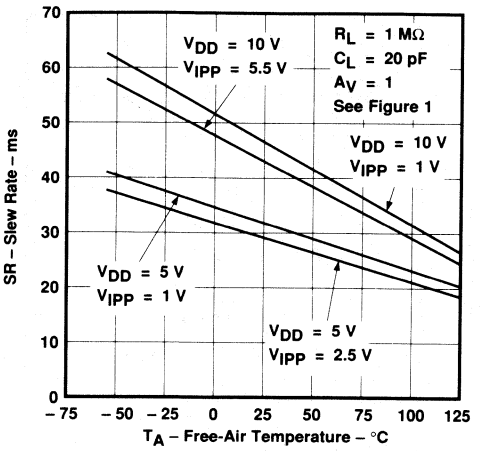


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

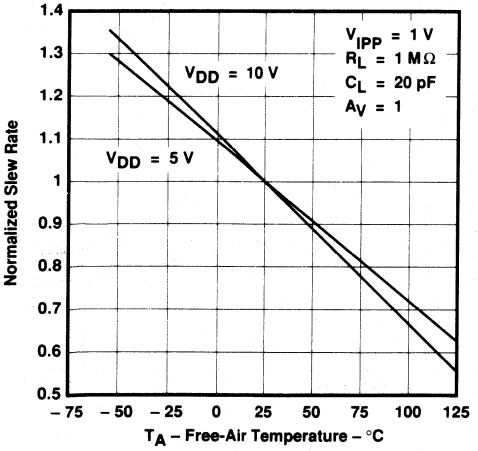


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

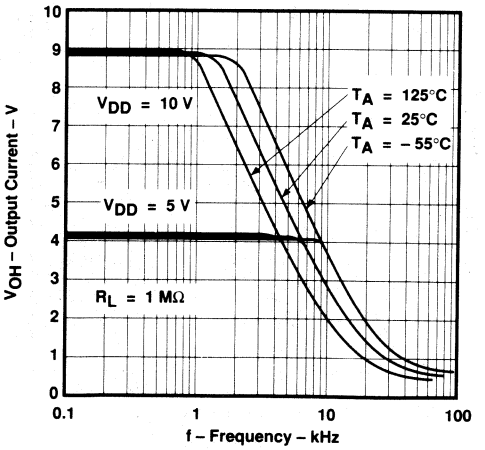


FIGURE 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

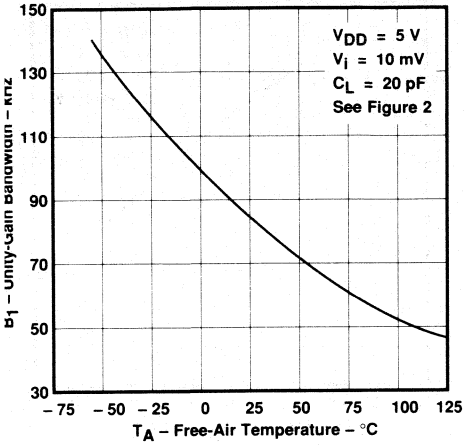


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

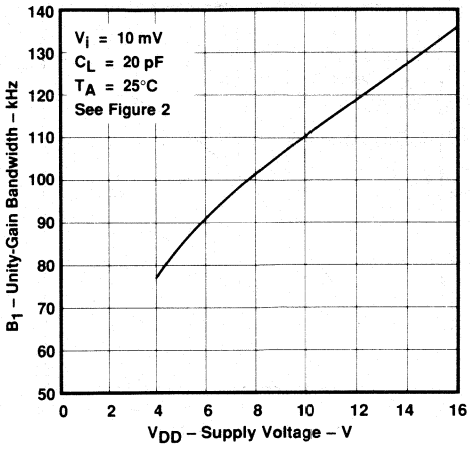


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

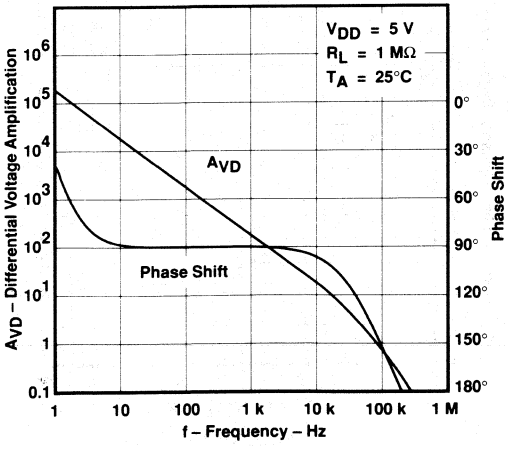


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

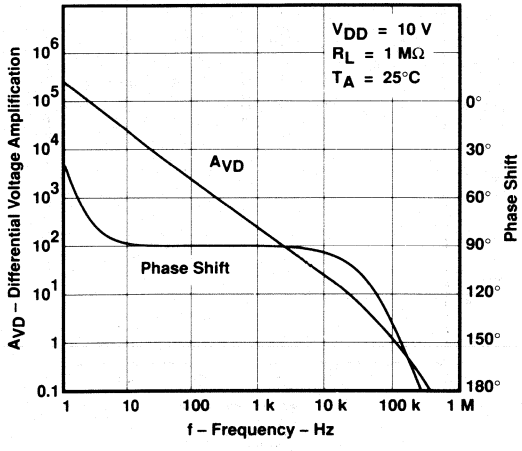


FIGURE 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

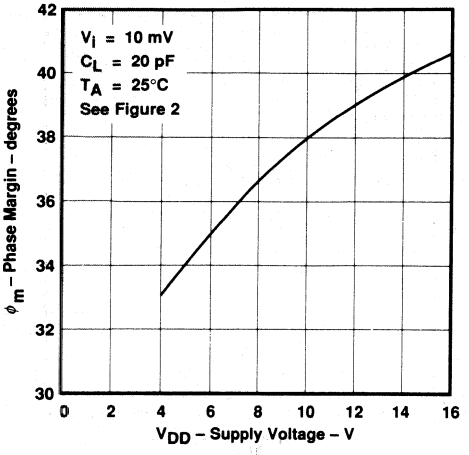


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

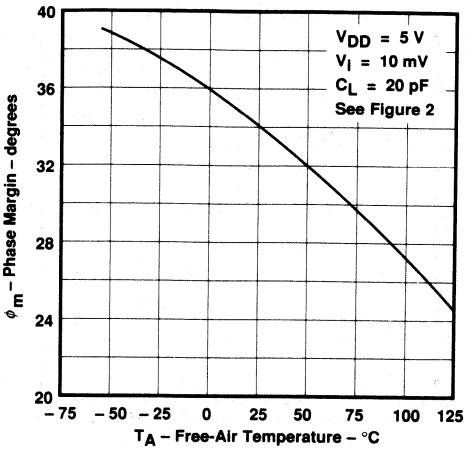


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

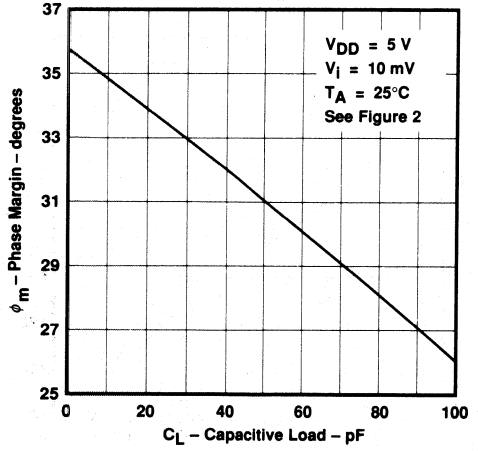


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

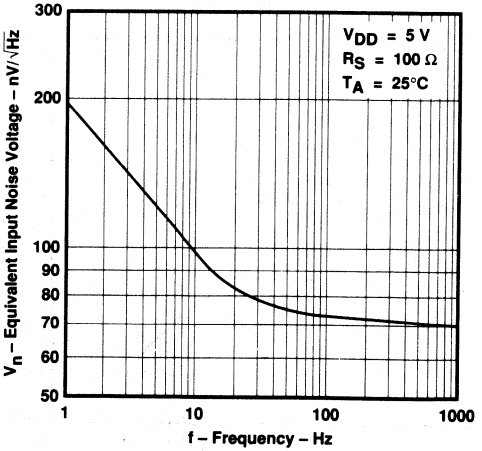


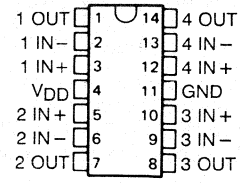
FIGURE 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

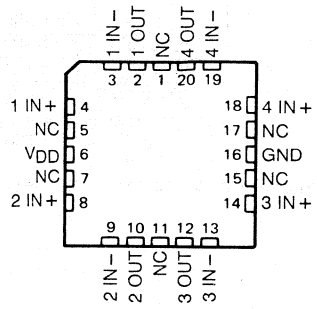
D3147, AUGUST 1988 – REVISED OCTOBER 1988

- **Power Dissipation as Low as 10 µW Typ per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 850 µV Max in DIP and Small-Outline Package**
- **Input Offset Voltage Drift . . . 0.1 µV/Month Typ, Including the First 30 Days**
- **High-Impedance LinCMOS™ Inputs I_{IB} = 0.6 pA Typ**
- **High Open-Loop Gain . . . 800,000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **14-Pin Small-Outline Package Option Also Available in Tape and Reel**

D, J, OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

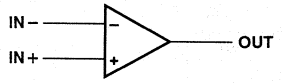
The TLC1079 operational amplifier offers ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-µW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC1079 is an ideal solution for low-voltage, battery-operated systems. The 20-mA output drive capability means that the TLC1079 can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

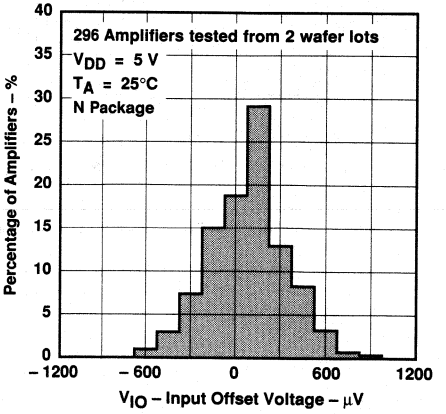
Since this device is functionally compatible as well as pin compatible with the TLC27L4 and TLC27L9, the TLC1079 easily upgrades existing designs that can benefit from its improved performance.

The TLC1079 incorporates internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care

symbol (each amplifier)



DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE



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description (continued)

should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC1079 design also inhibits latchup of the device inputs and outputs even with surge currents as large as 100 mA.

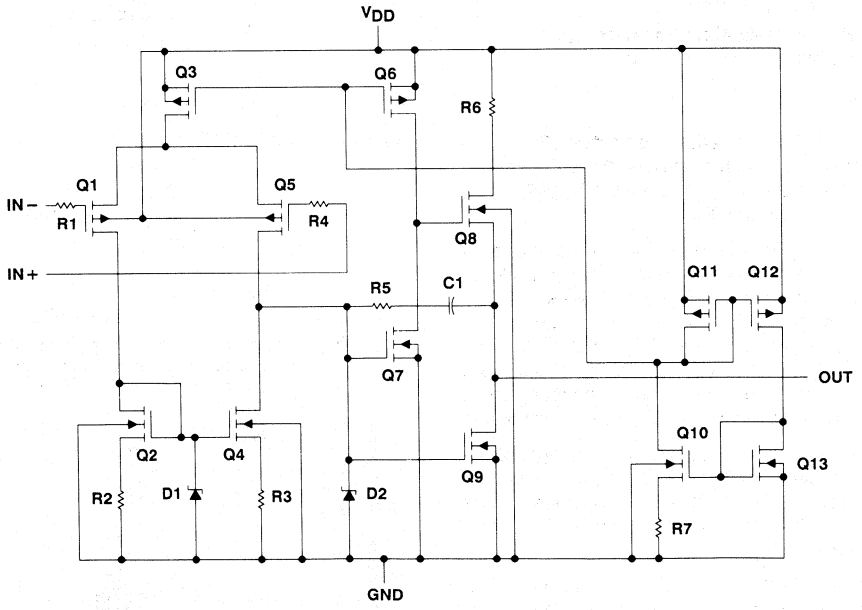
The M- suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I- suffix devices are characterized for operation from −40°C to 85°C. The C- suffix devices are characterized for operation from 0°C to 70°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D) SEE NOTE 1	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	TLC1079CD	–	TLC1079CJ	TLC1079CN
−40°C to 85°C	TLC1079ID	–	TLC1079IJ	TLC1079IN
−55°C to 125°C	–	TLC1079MFK	TLC1079MJ	–

NOTE 1: The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1079CDR).

equivalent schematic (each amplifier)



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD} (see Note 2) . . . . . 18 V
Different input voltage (see Note 3) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±30 mA
Total current into V_{DD} terminal (see Note 4) . . . . . 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 4) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 2. All voltage values, except differential voltages, are with respect to network ground.
3. Differential voltages are at the noninverting input with respect to the inverting input.
4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		4	−0.2		4	−0.2		4	V
	V_{DD} = 10 V	0		9	−0.2		9	−0.2		9	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_l = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1200			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ See Note 7	25°C	250	525		500	850		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			0°C		35			51		
			70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			0°C		100			125		
			70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			0°C		36°			40°		
			70°C		30°			34°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_l = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		µV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ See Note 7	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			−40°C		62	108		98	172	
			85°C		29	52		40	72	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

perating characteristics

PARAMETER		TEST CONDITIONS	T_A	V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−40°C		39			59		
			85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−40°C		130			155		
			85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−40°C		38°			42°		
			85°C		28°			32°		

electrical characteristics over operating free-air temperature range (unless otherwise noted)

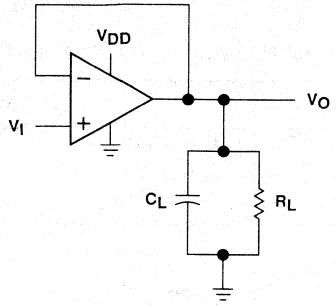
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0 V, R_S = 50 Ω, R_l = 1 MΩ	25°C		190	850		200	1150	µV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		µV/°C
I_{IO}	Input offset current (see Note 5)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1			0.1		pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 5)		25°C		0.6			0.7		pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 6)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ See Note 7	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	75	200		150	380		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		40	68		57	92	µA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

NOTES: 5. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
6. This range also applies to each input individually.
7. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics

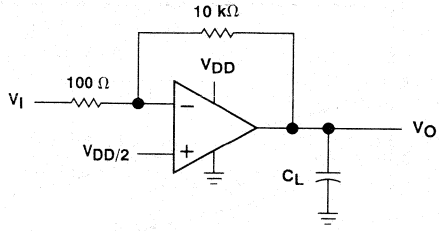
PARAMETER		TEST CONDITIONS		V_{DD} = 5 V			V_{DD} = 10 V			UNIT
			T_A	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, C_L = 20 pF, V_{IPP} = 1 V, See Figure 1	25°C		32			47		V/ms
			−55°C		41			63		
			125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω	25°C		68			68		nv/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF, See Figure 2	25°C		85			110		kHz
			−55°C		140			165		
			125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF, See Figure 2	25°C		34°			38°		
			−55°C		39°			43°		
			125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



C_L includes fixture capacitance.

FIGURE 1. SLEW RATE TEST CIRCUIT



C_L includes fixture capacitance.

FIGURE 2. UNITY-GAIN BANDWIDTH AND PHASE MARGIN TEST CIRCUIT

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

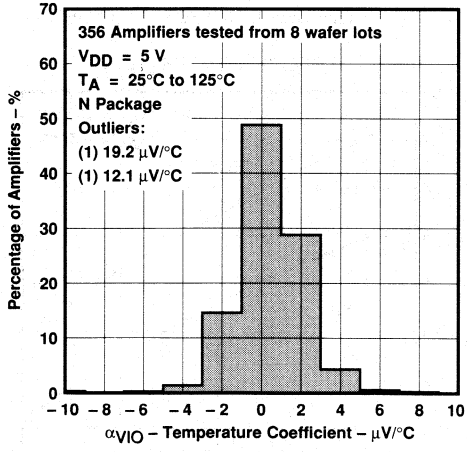


FIGURE 3

DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

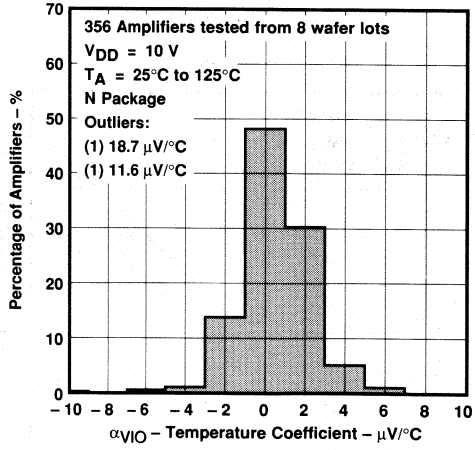


FIGURE 4

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

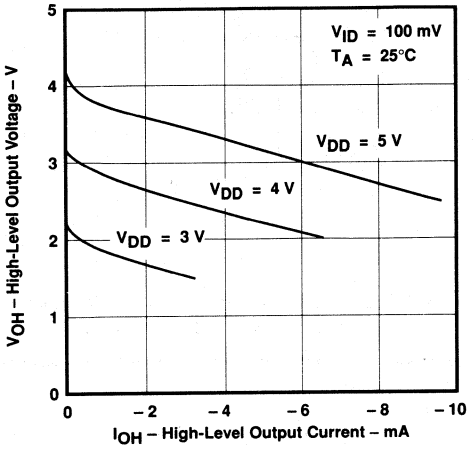


FIGURE 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

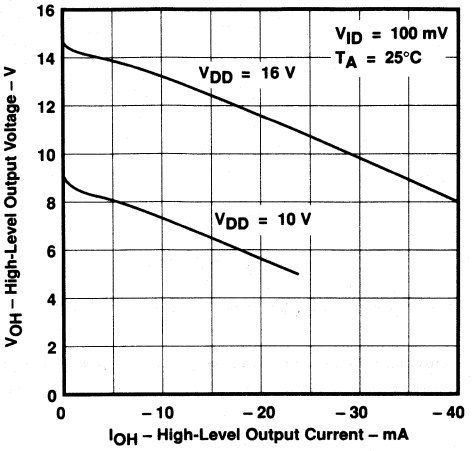


FIGURE 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

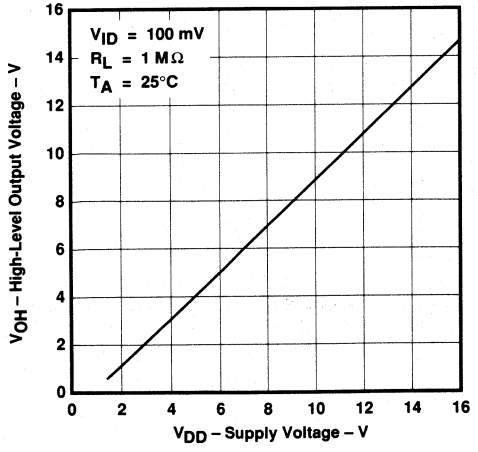


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

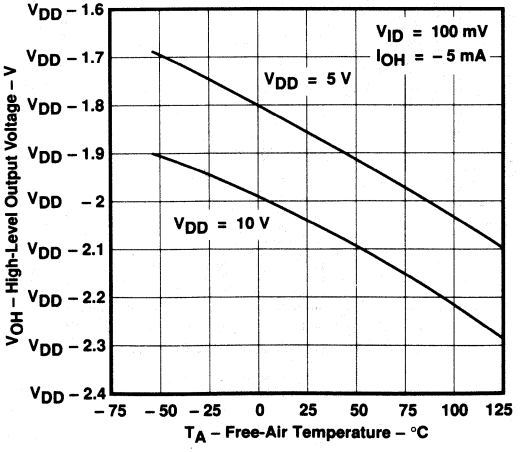


FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

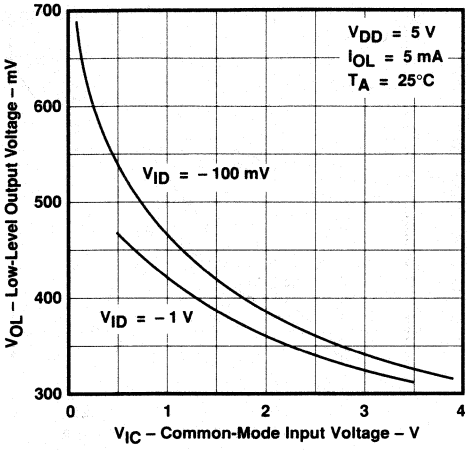


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

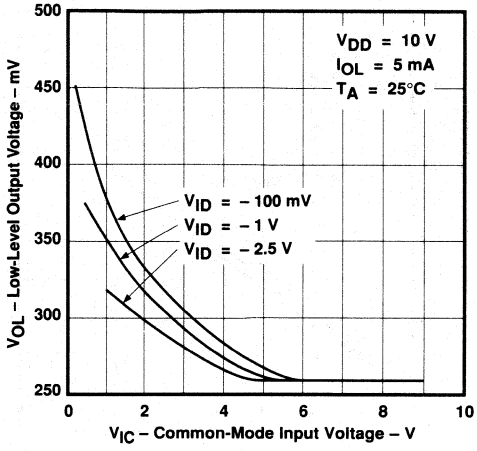


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

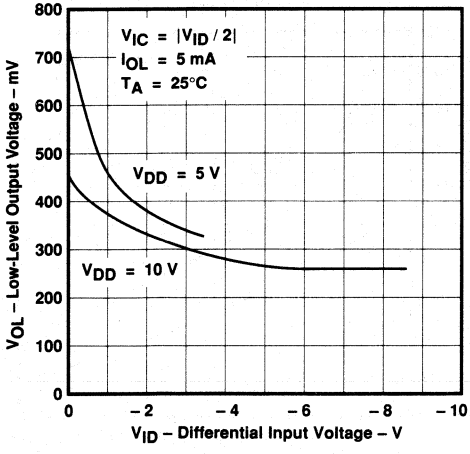


FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

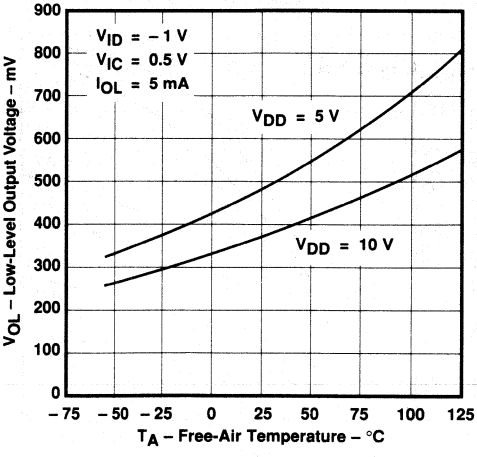


FIGURE 12

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

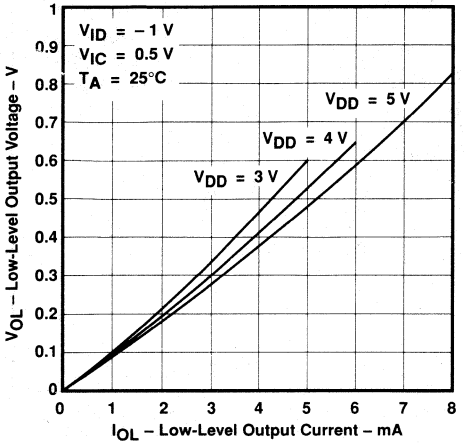


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

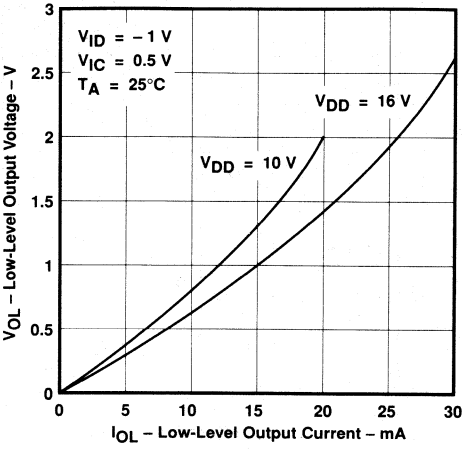


FIGURE 14

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

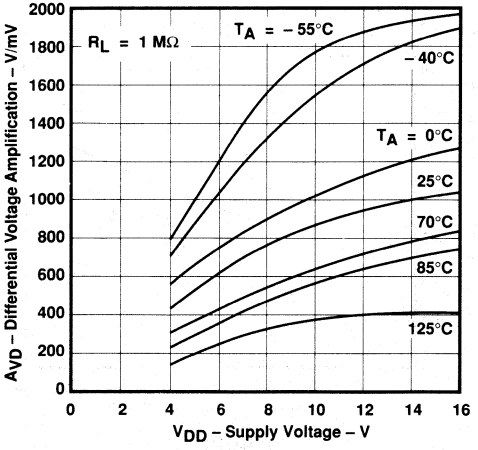


FIGURE 15

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

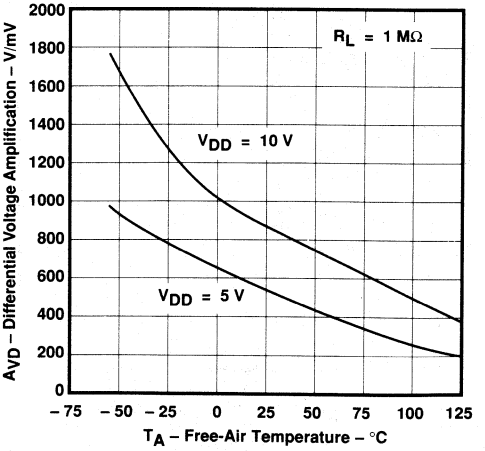


FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

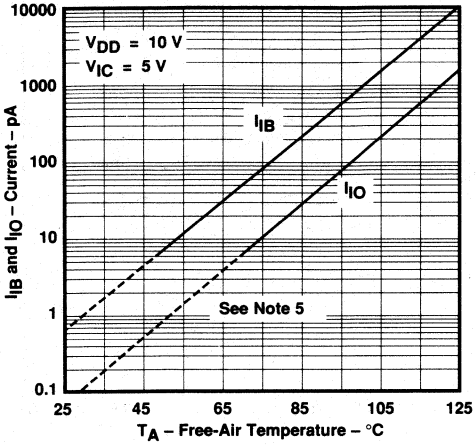


FIGURE 17

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT
vs
SUPPLY VOLTAGE

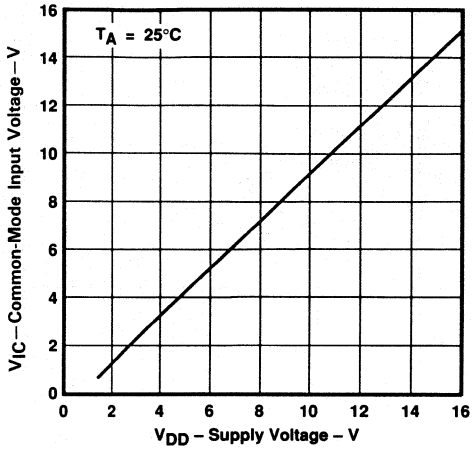


FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

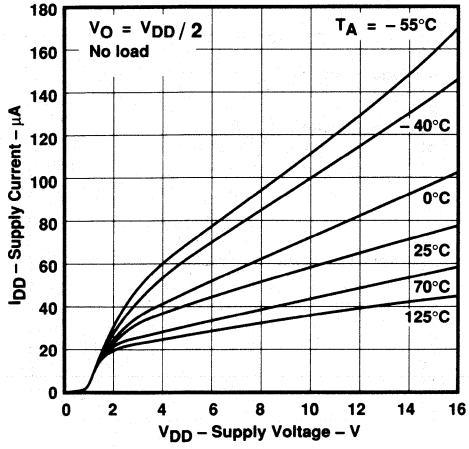


FIGURE 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

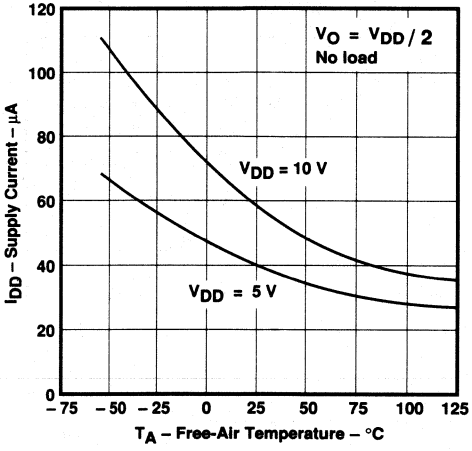


FIGURE 20

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 5: The typical values of input bias current and input offset current below 5 pA were determined mathmatically.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

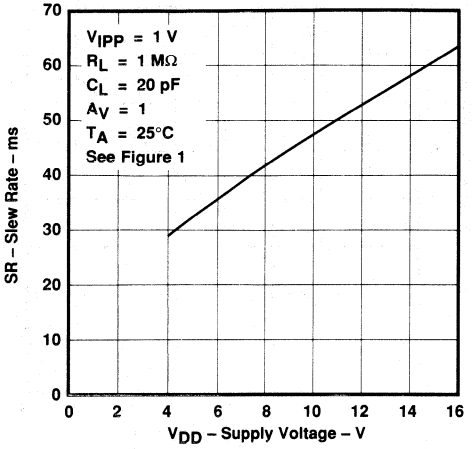


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

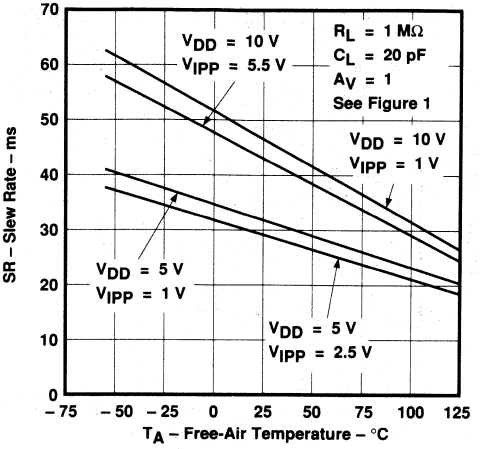


FIGURE 22

NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE

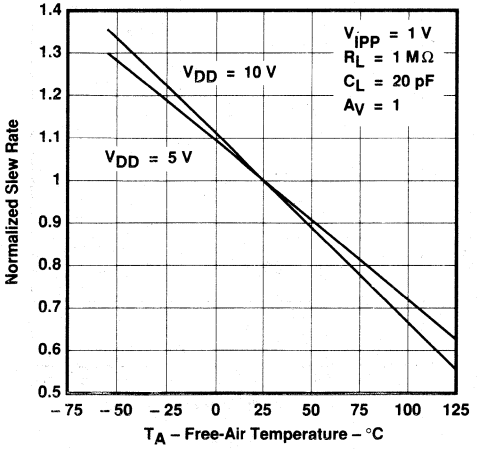


FIGURE 23

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

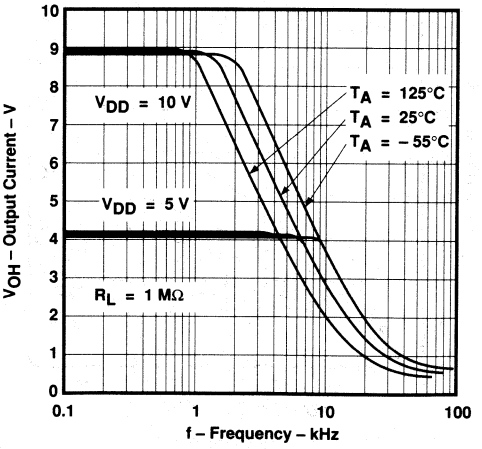


FIGURE 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

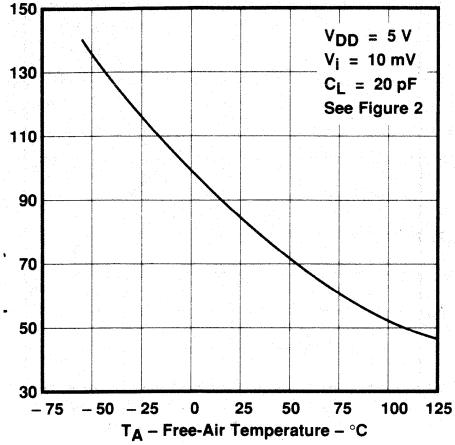


FIGURE 25

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

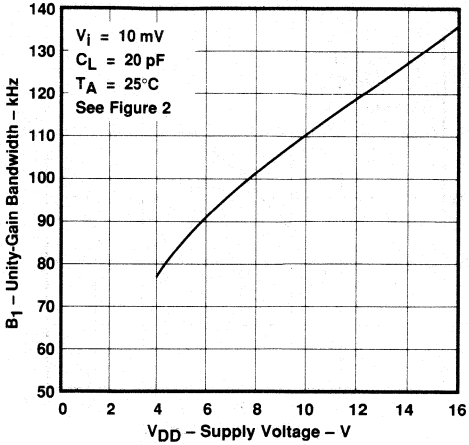


FIGURE 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

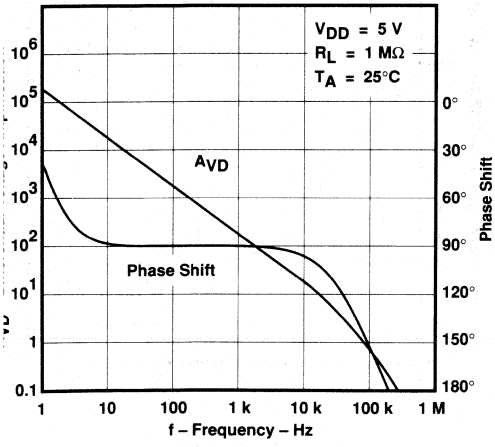


FIGURE 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

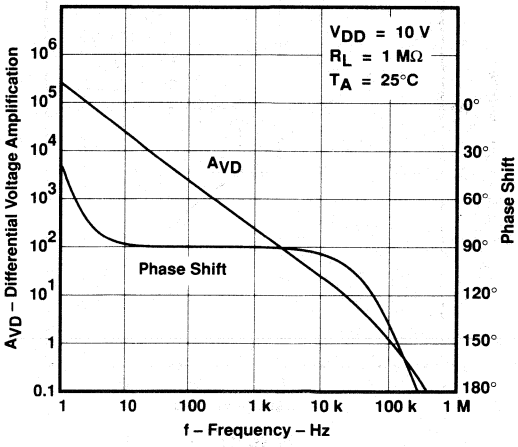


FIGURE 28

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

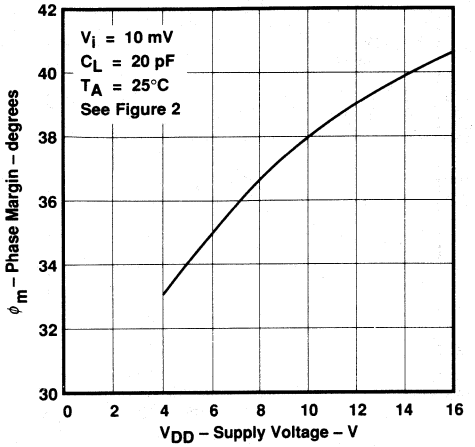


FIGURE 29

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

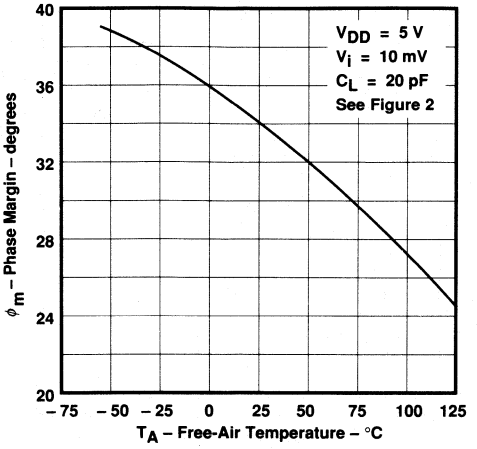


FIGURE 30

PHASE MARGIN
vs
CAPACITIVE LOAD

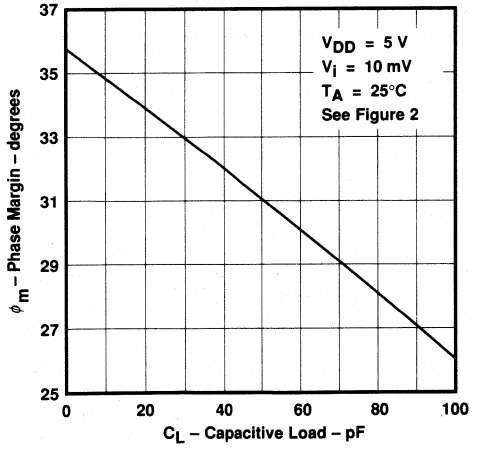


FIGURE 31

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

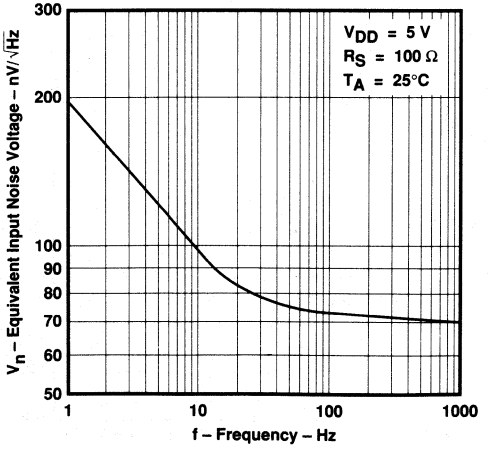


FIGURE 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

D3173, NOVEMBER 1988

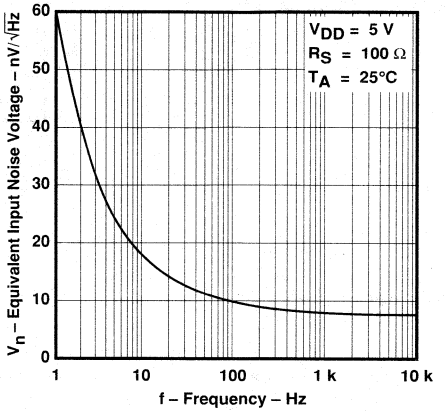
- **TLC2201B Is 100% Tested for Noise:**
  25 nV/√Hz Max at f = 10 Hz
  12 nV/√Hz Max at f = 1 kHz
- **Low Input Offset Voltage . . . 200 μV Max**
- **Excellent Offset Voltage Stability with Temperature . . . 0.5 μV/°C Typ**
- **Low Input Bias Current . . . 1 pA Typ at T_A = 25°C**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

escription

The TLC2201, TLC2201A, and TLC2201B are precision, low-noise operational amplifiers using Texas Instruments Advanced LinCMOS™ process. These devices combine the noise performance of the lowest-noise JFET amplifiers with the dc precision available previously only in bipolar amplifiers. The Advanced LinCMOS™ process uses silicon-gate technology to obtain input offset voltage stability with temperature and time that far exceeds that obtainable using metal-gate technology. In addition, this technology makes possible input impedance levels that meet or exceed levels offered by top-gate JFET and expensive dielectric-isolated devices.

The combination of excellent dc and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal conditioning applications in either single-supply or split-supply configurations.

TYPICAL EQUIVALENT
INPUT NOISE VOLTAGE
VS
FREQUENCY



The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup. In addition, internal ESD protection circuits prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	V_n max f = 10 Hz AT 25°C	V_n max f = 1 kHz AT 25°C	PACKAGE				
				SMALL-OUTLINE (D)	PLASTIC DIP (P)	CERAMIC DIP (JG)	CHIP CARRIER (FK)	METAL CAN (L)
0°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BCD	TLC2201BCP	TLC2201BCJG	—	TLC2201BCL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201ACD	TLC2201ACP	TLC2201ACJG	—	TLC2201ACL
70°C	500 μV	—	—	TLC2201CD	TLC2201CP	TLC2201CJG	—	TLC2201CL
- 40°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BID	TLC2201BIP	TLC2201BIJG	—	TLC2201BIL
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AID	TLC2201AIP	TLC2201AIJG	—	TLC2201AIL
85°C	500 μV	—	—	TLC2201ID	TLC2201IP	TLC2201IJG	—	TLC2201IL
- 55°C	200 μV	25 nV/√Hz	12 nV/√Hz	TLC2201BMD	TLC2201BMP	TLC2201BMJG	TLC2201BMFK	TLC2201BML
to	200 μV	35 nV/√Hz	15 nV/√Hz	TLC2201AMD	TLC2201AMP	TLC2201AMJG	TLC2201AMFK	TLC2201AML
125°C	500 μV	—	—	TLC2201MD	TLC2201MP	TLC2201MJG	TLC2201MFK	TLC2201ML

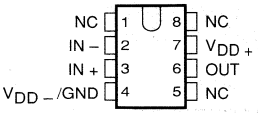
packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2201BCDR).

dvanced LinCMOS is a trademark of Texas Instruments Incorporated.

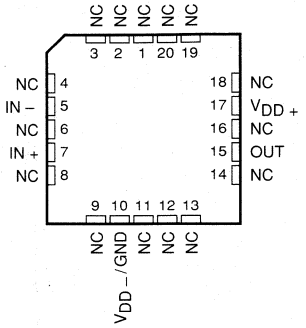
description (continued)

The M-suffix devices are characterized for operation over the full military temperature range of –55°C t 125°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The C-suffix devices ar characterized for operation from 0°C to 70°C.

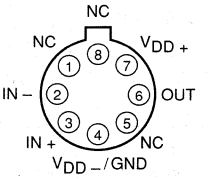
D, JG, or P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



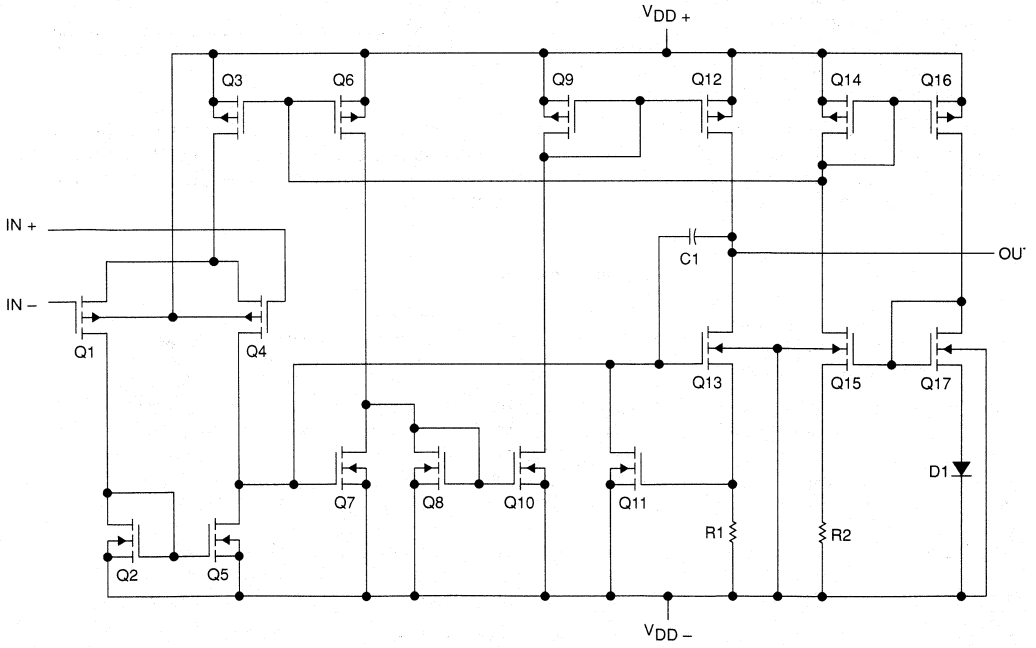
L PACKAGE
(TOP VIEW)



Pin 4 of the L package is in electrica contact with the case.

NC – No internal connection

equivalent schematic



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bsolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±8 V
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C

IOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

·ecommended operating conditions

	M-SUFFIX		I-SUFFIX		C-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-2.3$	V_{DD-}	$V_{DD+}-2.3$	V_{DD-}	$V_{DD+}-2.3$	V
Operating free-air temperature, T_A	−55	125	−40	85	0	70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TLC2201M TYP	TLC2201M MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		V
			Full range	– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TLC2201M TYP	TLC2201M MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

lectrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	200			200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	45			45			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

ɔperating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TLC2201M TYP	TLC2201M MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			700	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mc
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201M MIN	TLC2201M TYP	TLC2201M MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is – 55°C to 125°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			400			400	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	75			75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	10			10			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AM			TLC2201BM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/μs
			Full range	1.1			1.1			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	µV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		V
			Full range	– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	250			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	65			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/µs
			Full range	1.4			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is – 40°C to 85°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	µV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	250			250			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	65			65			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/µs
			Full range	1.4			1.4			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

† Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			650	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			150	
I_{IB}	Input bias current		25°C		1		pA
			Full range			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201I MIN	TLC2201I TYP	TLC2201I MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.2			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
PP	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

is – 40°C to 85°C.
/pical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolate T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			350			350	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AI			TLC2201BI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/μs
			Full range	1.2			1.2			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		V
			Full range	−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ,	25°C	400	560		V/mV
			Full range	300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	70			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.5			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		400	560		V/mV
			Full range	300			300			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		90	100		
			Full range	70			70			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	115		90	115		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.1	1.5		1.1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		2	2.7		V/μs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		100	500	μV
			Full range			600	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			100	
I_{IB}	Input bias current		25°C		1		pA
			Full range			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ,	25°C	150	315		V/mV
			Full range	100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5	mA
			Full range			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201C MIN	TLC2201C TYP	TLC2201C MAX	UNIT
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

†Full range is 0°C to 70°C.

NOTE 4: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200		80	200	μV
			Full range			300			300	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.5			0.5		μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.001	0.005		0.001	0.005	μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50		0	50	mV
			Full range			50			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		150	315		V/mV
			Full range	100			100			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		25	55		
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	90	110		90	110		dB
			Full range	85			85			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		90	110		dB
			Full range	85			85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1	1.5		1	1.5	mA
			Full range			1.5			1.5	

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2201AC			TLC2201BC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		1.8	2.5		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage (see Note 5)	f = 10 Hz	25°C		18	35		18	25	nV/√Hz
		f = 1 kHz	25°C		8	15		8	12	
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5			0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7			0.7		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.8			1.8		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°			45°		

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. This parameter is tested on a sample basis for the TLC2201A and on all devices for the TLC2201B. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

PARAMETER MEASUREMENT INFORMATION

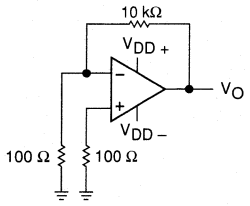
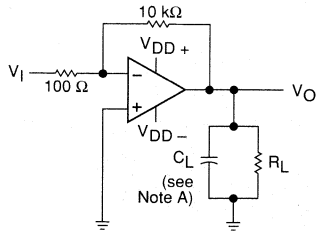
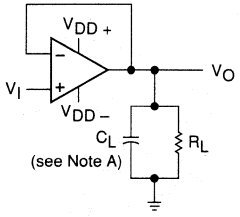


FIGURE 1. NOISE VOLTAGE TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 2. PHASE MARGIN TEST CIRCUIT



NOTE A: C_L includes fixture capacitance.

FIGURE 3. SLEW RATE TEST CIRCUIT

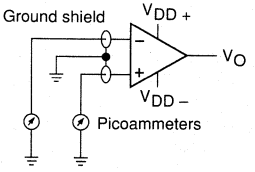


FIGURE 4. INPUT BIAS AND OFFSET CURRENT TEST CIRCUIT

typical values

Typical values as presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoamp bias current level typical of the TLC2201, TLC2201A, and TLC2201B, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

Texas Instruments offers automated production noise testing to meet individual applications requirements. Noise voltage at f = 10 Hz and f = 1 kHz is 100% tested on every TLC2201B device, while lot sample testing is performed on the TLC2201A. For other noise test requirements, please contact the factory.

TYPICAL CHARACTERISTICS

able of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	5
I_{IB}	Input bias current	vs Common-mode voltage	6
		vs Temperature	7
CMRR	Common-mode rejection ratio	vs Frequency	8
V_{OM}	Maximum peak output voltage	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage	vs Frequency	11
V_{OH}	High-level output voltage	vs Frequency	12
		vs Current	13
		vs Temperature	14
V_{OL}	Low-level output voltage	vs Output current	15
		vs Temperature	16
A_{VD}	Differential voltage amplification	vs Frequency	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
I_{DD}	Supply current	vs Supply voltage	21
		vs Temperature	22
SR	Slew rate	vs Supply voltage	23
		vs Temperature	24
	Pulse response	Small-signal	25, 26
		Large-signal	27, 28
V_{NPP}	Peak-to-peak equivalent input noise voltage	0.1 to 1 Hz	29
		0.1 to 10 Hz	30
	Gain-bandwidth product	vs Supply voltage	31
		vs Temperature	32
ϕ_m	Phase margin	vs Supply voltage	33
		vs Temperature	34
	Phase shift	vs Frequency	17

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2201
INPUT OFFSET VOLTAGE

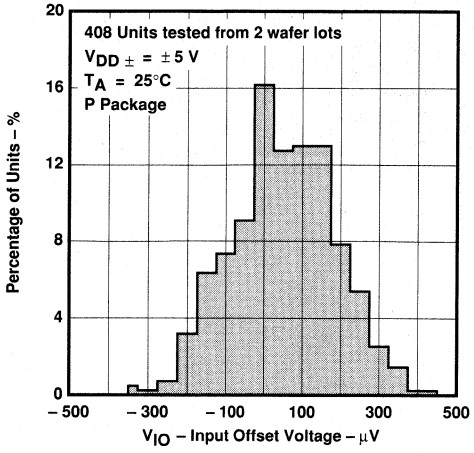


FIGURE 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

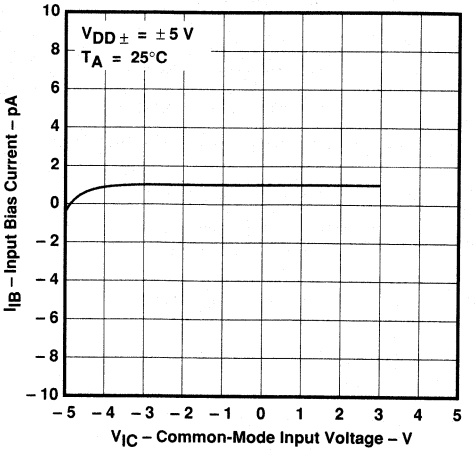


FIGURE 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

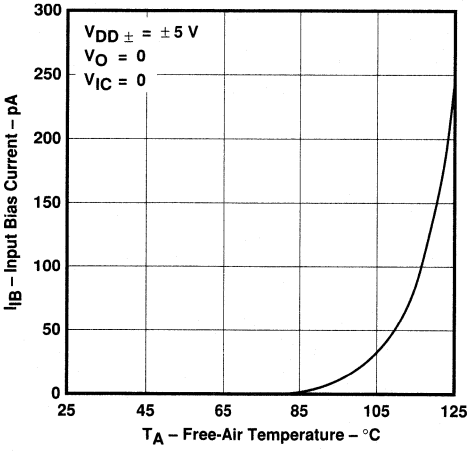


FIGURE 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

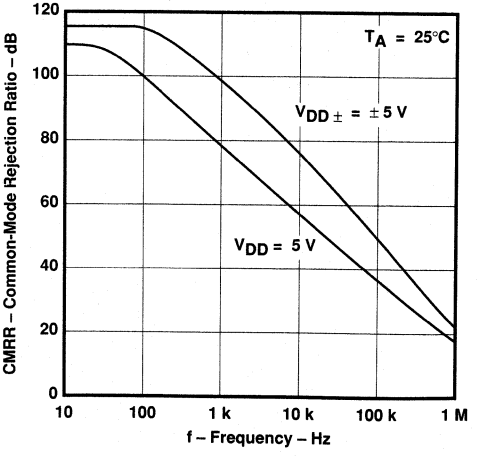


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

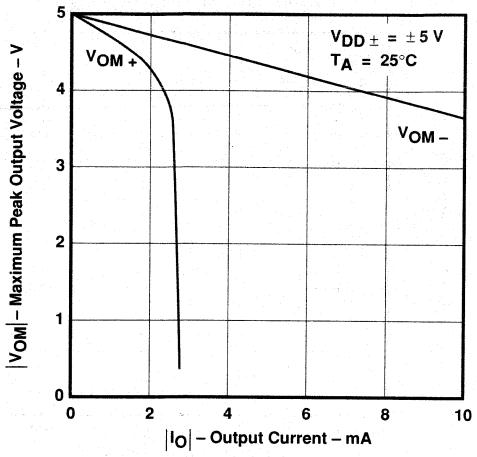


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

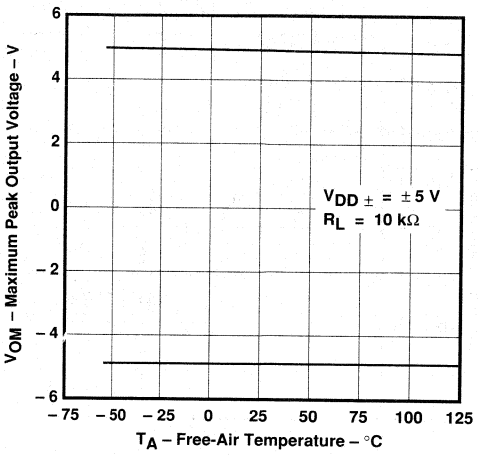


FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

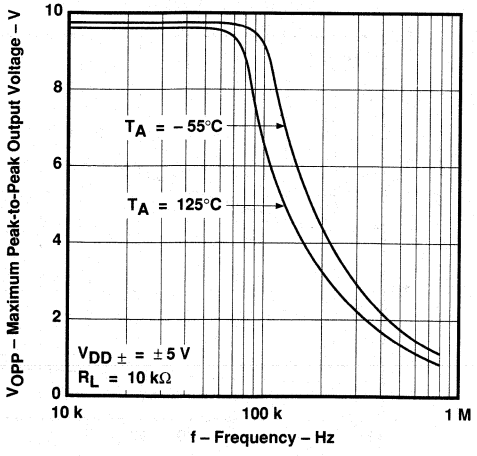


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREQUENCY

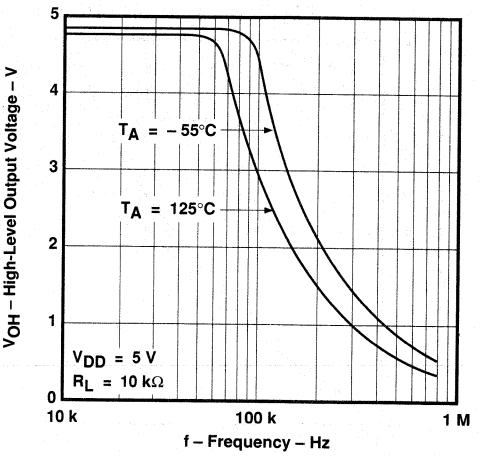


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

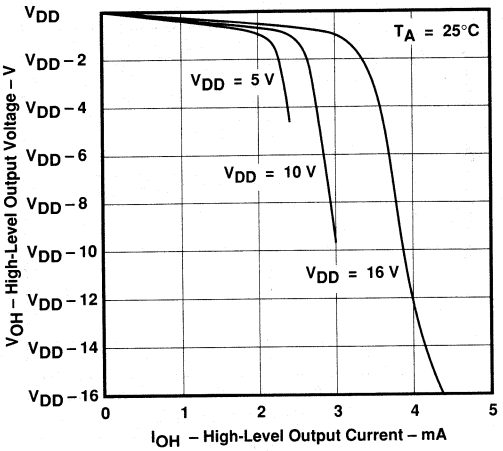


FIGURE 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

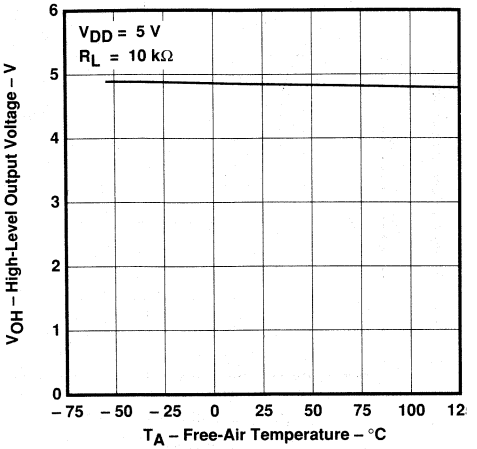


FIGURE 14

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

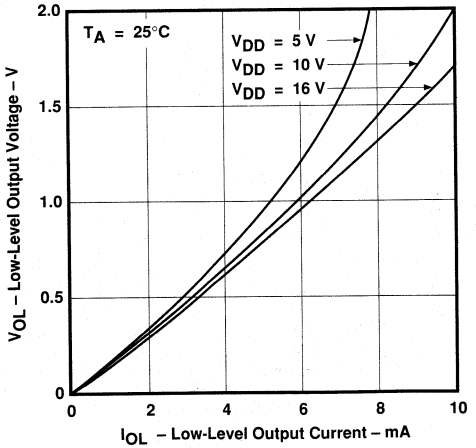


FIGURE 15

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

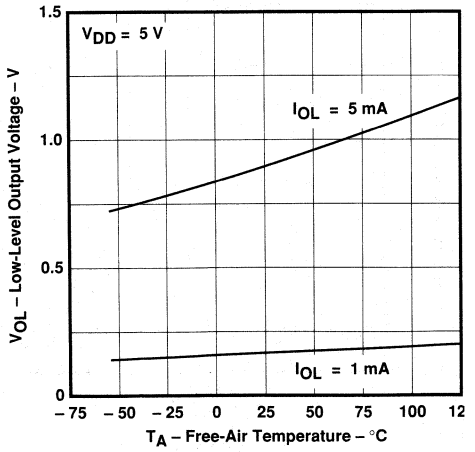


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

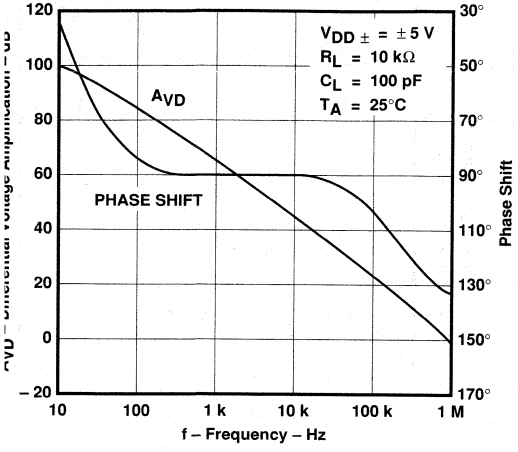


FIGURE 17

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

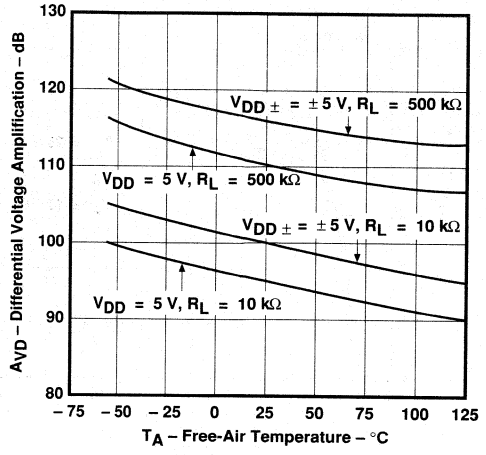


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

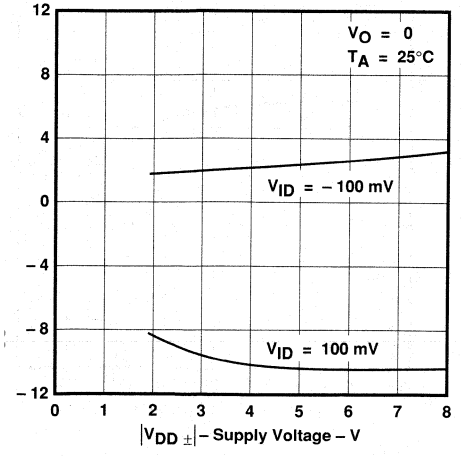


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

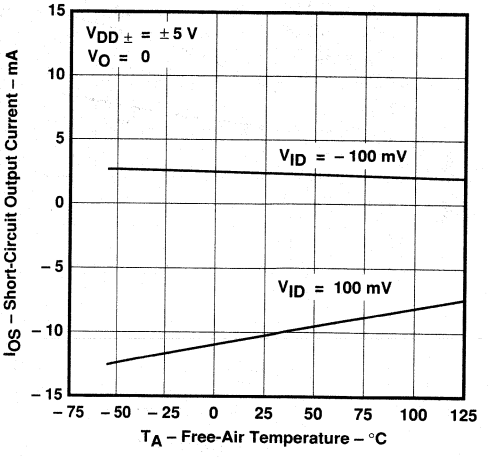


FIGURE 20

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

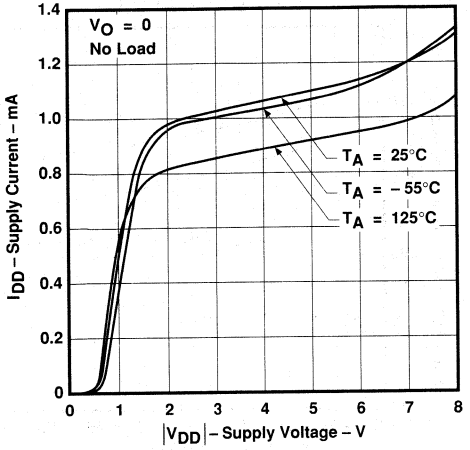


FIGURE 21

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

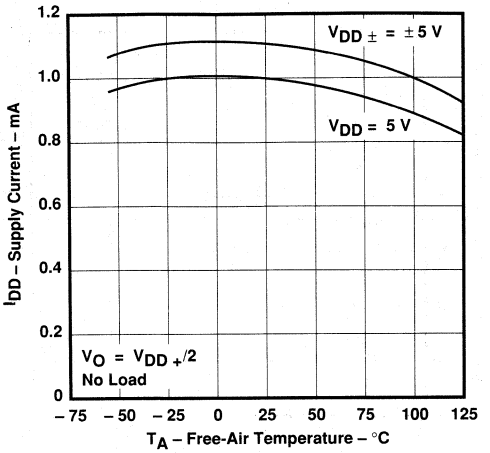


FIGURE 22

SLEW RATE
vs
SUPPLY VOLTAGE

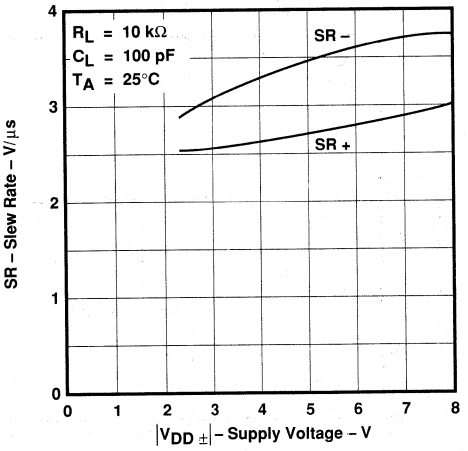


FIGURE 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

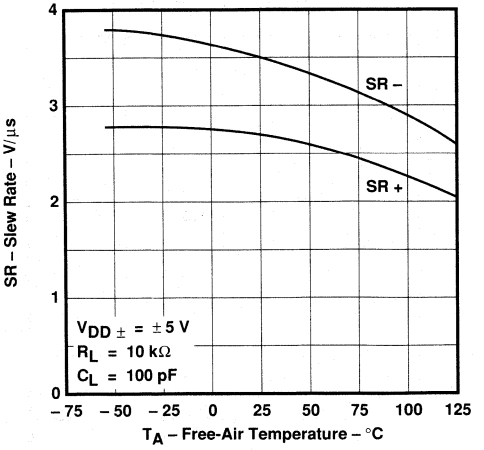


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

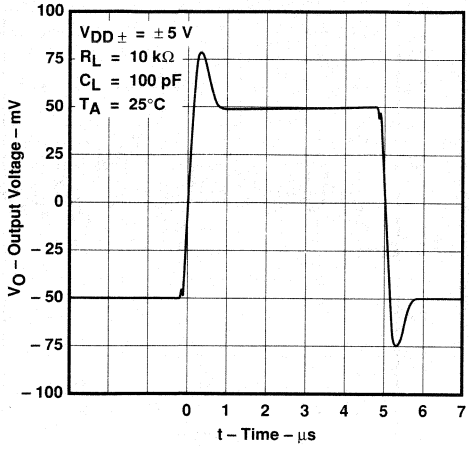


FIGURE 25

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

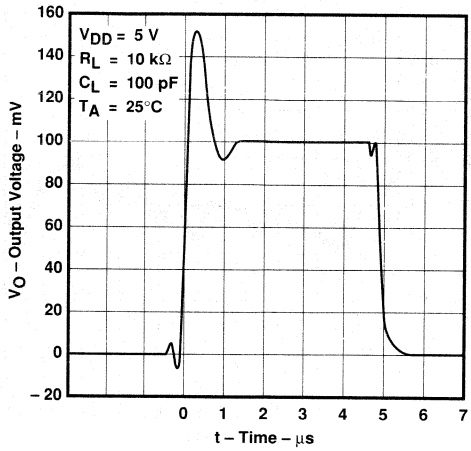


FIGURE 26

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

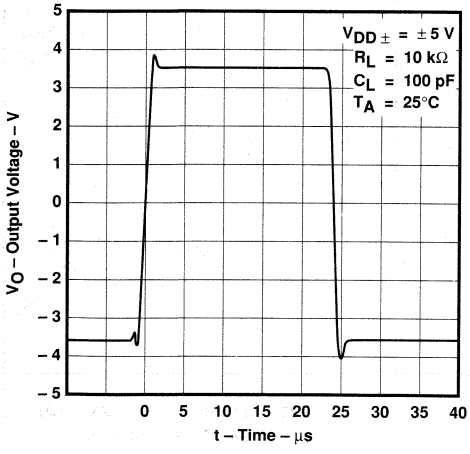


FIGURE 27

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

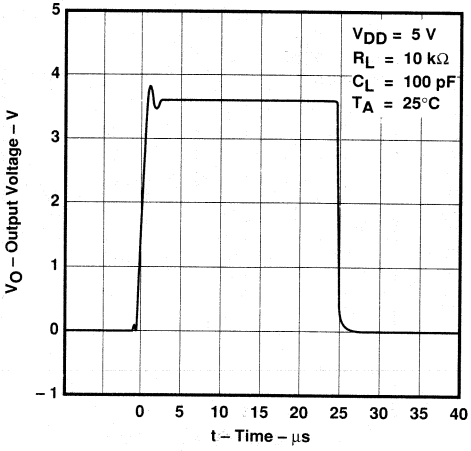


FIGURE 28

TYPICAL CHARACTERISTICS†

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 1 Hz

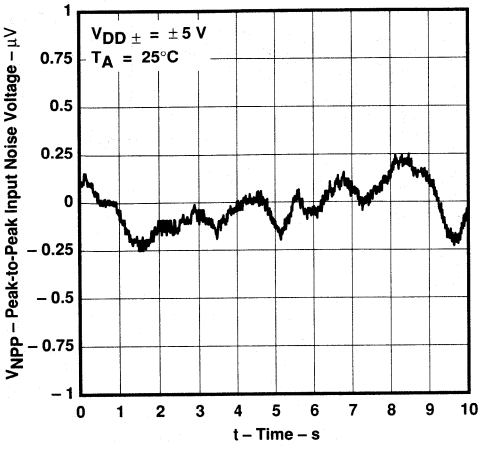


FIGURE 29

PEAK-TO-PEAK EQUIVALENT
INPUT NOISE VOLTAGE
0.1 TO 10 Hz

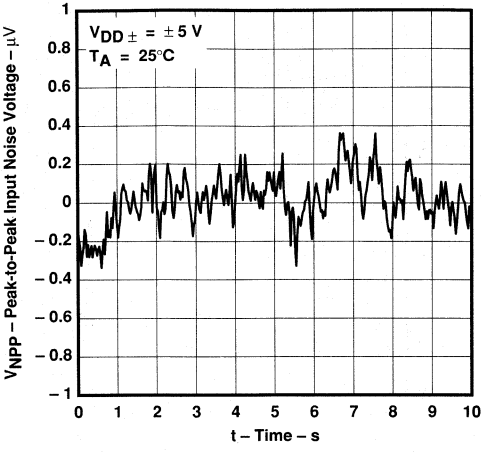


FIGURE 30

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

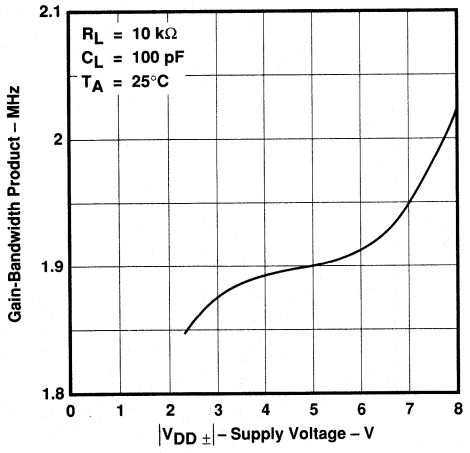


FIGURE 31

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

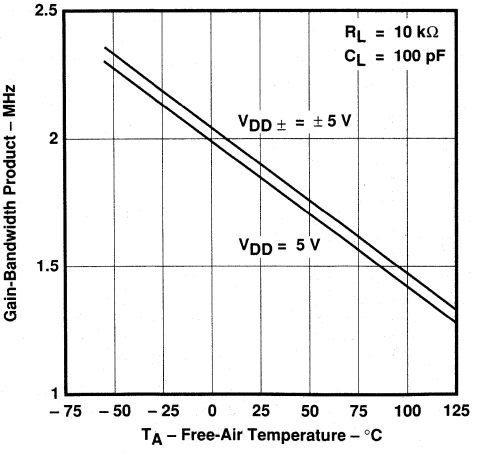


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

PHASE MARGIN
vs
SUPPLY VOLTAGE

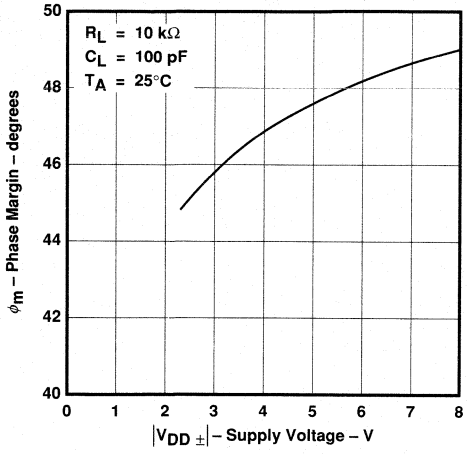


FIGURE 33

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

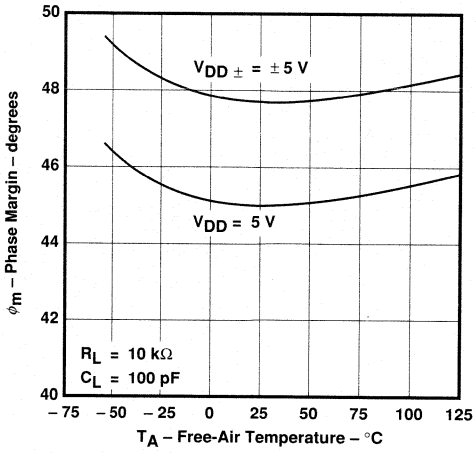


FIGURE 34

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

latchup avoidance

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2201, TLC2201A, and TLC2201B inputs and outputs are designed to withstand –100-mA surge currents without sustaining latchup; however, techniques reducing the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

electrostatic discharge protection

These devices use internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

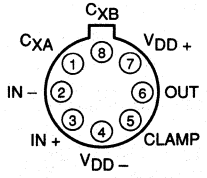
2 Operational Amplifiers

- **Extremely Low Offset Voltage ... 1 μV Max**
- **Extremely Low Change in Offset Voltage with Temperature ... 0.003 μV/°C Typ**
- **Low Input Offset Current ... 500 pA Max at T_A = −55°C to 125°C**
- **AVD ... 135 dB Min**
- **CMRR and kSVR ... 120 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Includes the Negative Rail**
- **No Noise Degradation with External Capacitors Connected to V_{DD-}**

lescription

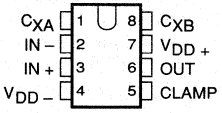
The TLC2652 and TLC2652A are high-precision chopper-stabilized operational amplifiers using Texas Instruments **Advanced LinCMOS™** process. This process in conjunction with unique chopper-stabilization circuitry produces operational amplifiers whose performance matches or exceeds that of similar devices available today.

L PACKAGE
(TOP VIEW)

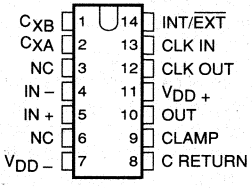


'in 4 of the L package is in electrical contact with the case.

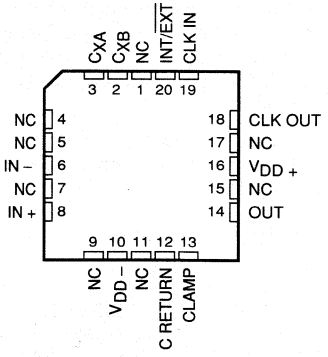
D008, JG, or P PACKAGE
(TOP VIEW)



D014, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE							
		8-PIN				14-PIN			20-PIN
		SMALL-OUTLINE (D008)	PLASTIC DIP (P)	CERAMIC DIP (JG)	METAL CAN (L)	SMALL-OUTLINE (D014)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	1 μV	TLC2652AC-8D	TLC2652ACP	TLC2652ACJG	TLC2652ACL	TLC2652AC-14D	TLC2652ACN	TLC2652ACJ	—
	3 μV	TLC2652C-8D	TLC2652CP	TLC2652CJG	TLC2652CL	TLC2652C-14D	TLC2652CN	TLC2652CJ	—
− 40°C to 85°C	1 μV	TLC2652AI-8D	TLC2652AIP	TLC2652AIJG	TLC2652AIL	TLC2652AI-14D	TLC2652AIN	TLC2652AIJ	—
	3 μV	TLC2652I-8D	TLC2652IP	TLC2652IJG	TLC2652IL	TLC2652I-14D	TLC2652IN	TLC2652IJ	—
− 55°C to 125°C	1 μV	TLC2652AM-8D	TLC2652AMP	TLC2652AMJG	TLC2652AML	TLC2652AM-14D	TLC2652AMN	TLC2652AMJ	TLC2652AMFK
	3 μV	TLC2652M-8D	TLC2652MP	TLC2652MJG	TLC2652ML	TLC2652M-14D	TLC2652MN	TLC2652MJ	TLC2652MFK

)008 and D014 packages are available taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC2652AC-8DR).
ıdvanced LinCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

Chopper stabilization techniques make possible extremely high dc precision by continuously nulling inpu offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage In addition, low-frequency noise voltage is significantly reduced. This high precision, coupled with th extremely high input impedance of the CMOS input stage, makes the TLC2652 and TLC2652A an ideal choic for low-level signal processing applications such as strain gauges, thermocouples, and other transduce amplifiers. (For applications that require extremely low noise and higher usable bandwidth, use the TLC265 or TLC2654A device, which has a chopping frequency of 10 kHz.)

The TLC2652 and TLC2652A input common-mode range includes the negative rail, thereby providing superio performance in either single-supply or split-supply applications, even at power supply voltage levels as low a ±1.9 V.

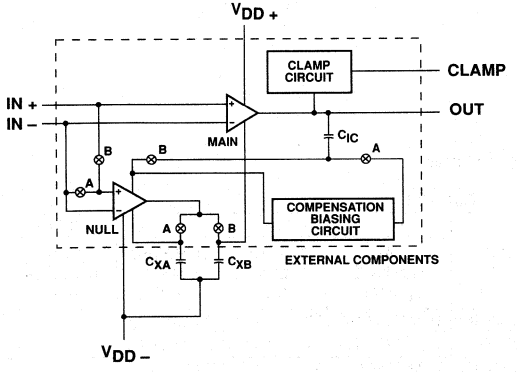
Two external capacitors are required for operation of the device; however, the on-chip chopper control circuitr is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is mad accessible to allow the user the option of controlling the clock frequency with an external frequency source In addition, the clock threshold level of the TLC2652 and TLC2652A require no level shifting when used in th single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques are used on the TLC2652 and TLC2652A to allow exceptionally fast overloa recovery time. If desired, an output clamp pin is available to reduce the recovery time even further.

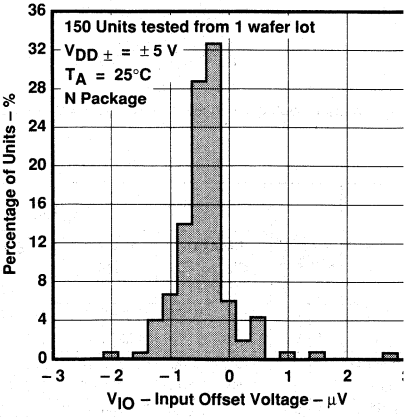
The device inputs and output are designed to withstand –100-mA surge currents without sustaining latchup Additionally, the TLC2652 and TLC2652A incorporate internal ESD protection circuits that prevent functiona failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should b exercised in handling these devices as exposure to ESD may result in degradation of the device parametri performance.

The M-suffix devices are characterized for operation over the full military temperature range of –55°C t 125°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The C-suffix devices ar characterized for operation from 0°C to 70°C.

functional block diagram



DISTRIBUTION OF TLC2652
INPUT OFFSET VOLTAGE



ıbsolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins . . . . . V_{DD-} to V_{DD-} +5.2 V
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins . . . . . ±5 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package . . . . . 300°C

ıOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

ecommended operating conditions

	M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	± 1.9		± 8	± 1.9		± 8	± 1.9		± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V_{DD-}		$V_{DD+} - 1.9$	V
Clock Input voltage	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V_{DD-}		$V_{DD-} + 5$	V
Operating free-air temperature, T_A	− 55		125	− 40		85	0		70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AM			TLC2652M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	1		0.6	3	µV
			Full range			4			6	
α_{VIO}	Temperature coefficient of input offset voltage		−55°C to 125°C		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	150		120	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	V_O = −4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±1.9 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is −55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AM			TLC2652M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.3			1.3			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.6			1.6			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		94			94		nV/√Hz
		f = 1 kHz	25°C		23			23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is − 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AI			TLC2652I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	1		0.6	3	µV
			Full range			2.95			4.95	
α_{VIO}	Temperature coefficient of input offset voltage		– 40°C to 85°C		0.003	0.03		0.003	0.03	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 3.1			– 5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	150		120	150		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	V_O = – 4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±1.9 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is – 40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2652AI			TLC2652I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.4			1.4			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is − 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AC			TLC2652C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	1		0.6	3	μV
			Full range			2.35			4.35	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.003	0.03		0.003	0.03	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		2			2		pA
			Full range			100			100	
I_{IB}	Input bias current		25°C		4			4		pA
			Full range			100			100	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 3.1			−5 to 3.1			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	150		120	150		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		450			450		Hz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	V_O = −4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±1.9 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	135		120	135		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.4		1.5	2.4	mA
			Full range			2.5			2.5	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2652AC			TLC2652C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.8		2	2.8		V/μs
			Full range	1.5			1.5			
SR−	Negative slew rate at unity gain		25°C	2.3	3.1		2.3	3.1		V/μs
			Full range	1.8			1.8			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		94	140		94		nV/√Hz
		f = 1 kHz	25°C		23	35		23		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.8			0.8		μV
		f = 0 to 10 Hz	25°C		2.8			2.8		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is 0°C to 70°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2652A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Normalized Input offset voltage	vs Chopping frequency	1
I_{IB}	Input bias current	vs Common-mode input voltage	2
		vs Chopping frequency	3
		vs Temperature	4
I_{IO}	Input offset current	vs Chopping frequency	5
		vs Temperature	6
	Clamp current	vs Output voltage	7
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9, 10
		vs Temperature	11, 12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
	Gain-bandwidth product	vs Supply voltage	28
		vs Temperature	29
ϕ_m	Phase margin	vs Supply voltage	30
		vs Temperature	31
		vs Load capacitance	32
	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

NORMALIZED INPUT OFFSET VOLTAGE
vs
CHOPPING FREQUENCY

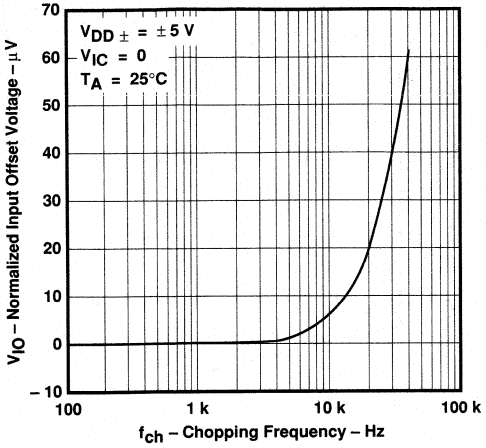


FIGURE 1

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

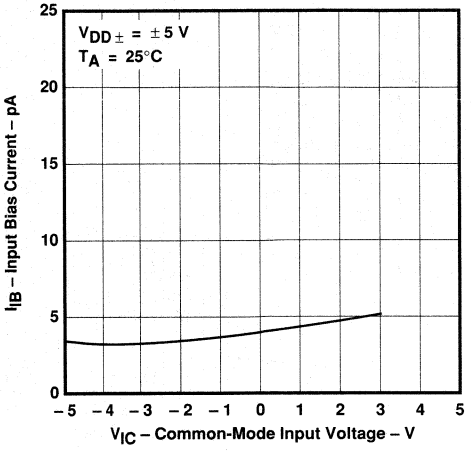


FIGURE 2

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

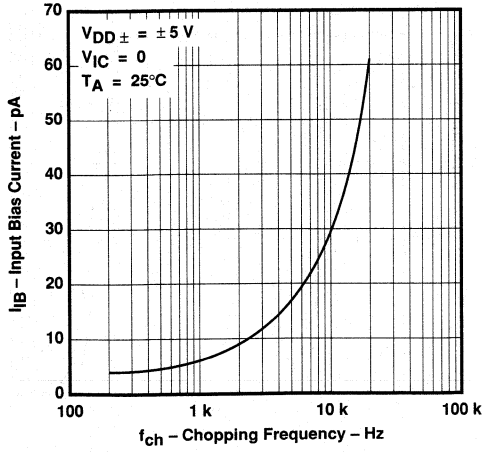


FIGURE 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

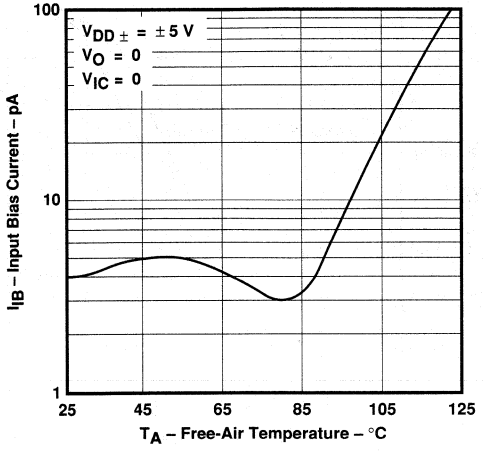


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT OFFSET CURRENT
vs
CHOPPING FREQUENCY

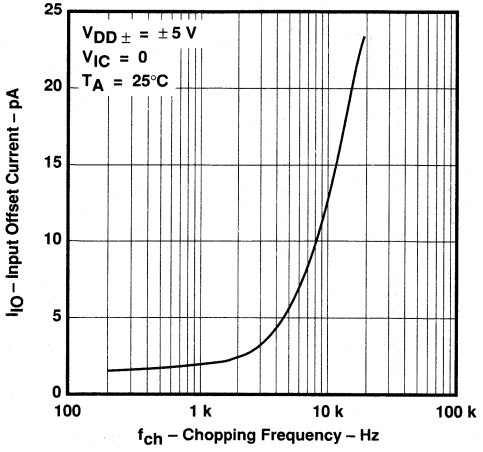


FIGURE 5

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

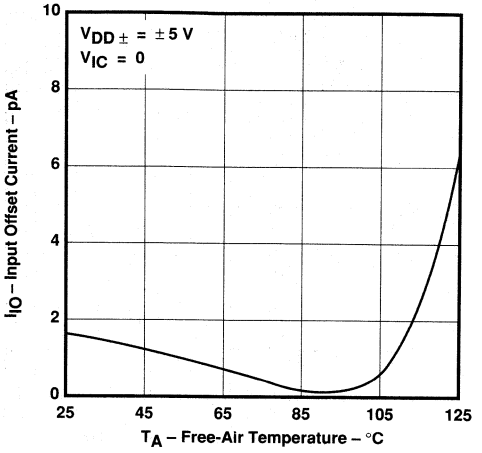


FIGURE 6

CLAMP CURRENT
vs
OUTPUT VOLTAGE

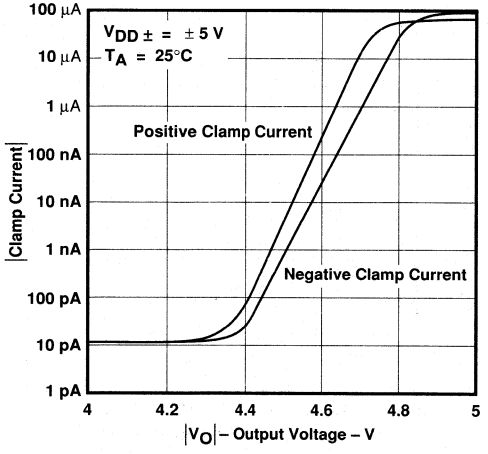


FIGURE 7

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

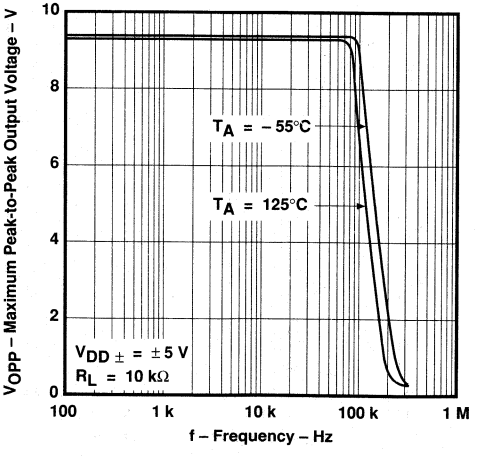


FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

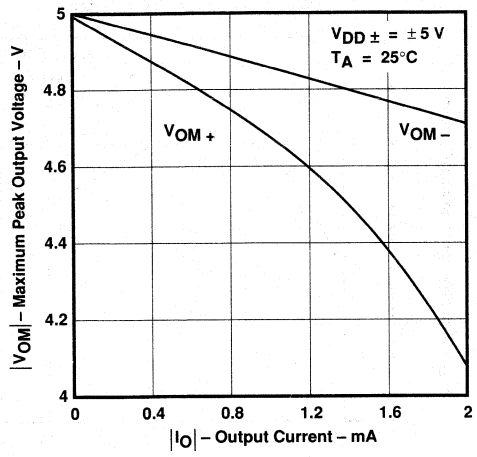


FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

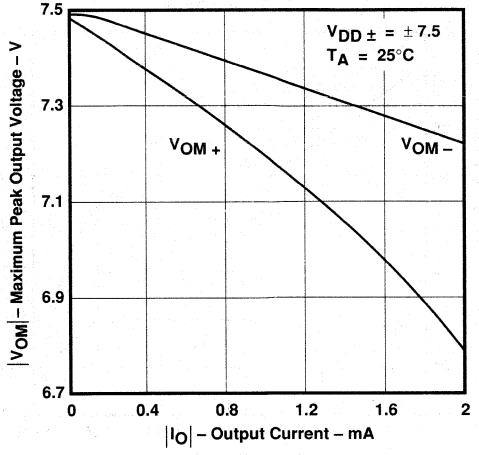


FIGURE 10

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

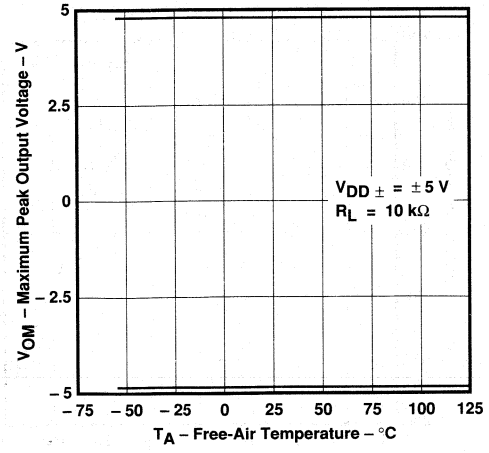


FIGURE 11

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

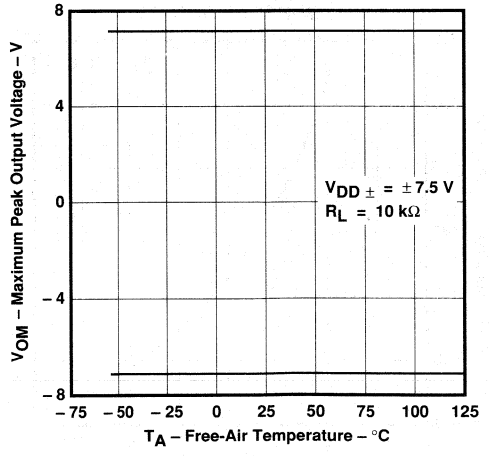


FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

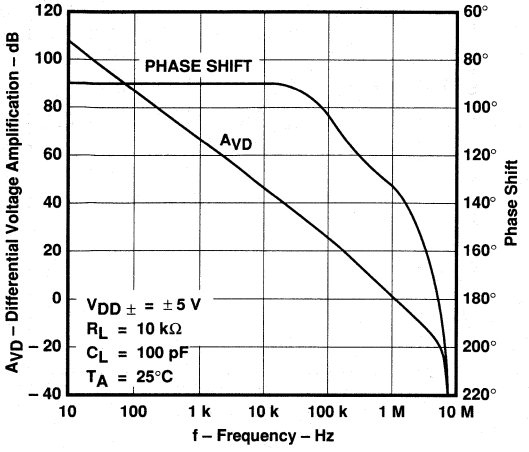


FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

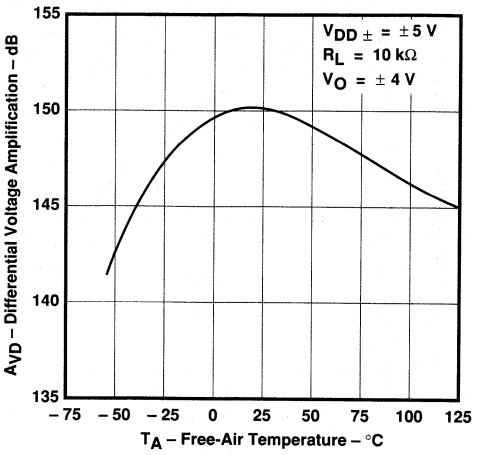


FIGURE 14

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

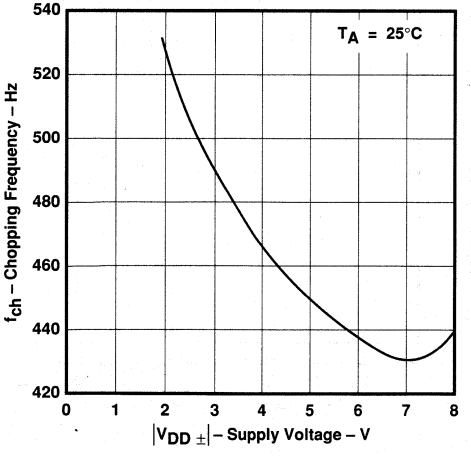


FIGURE 15

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

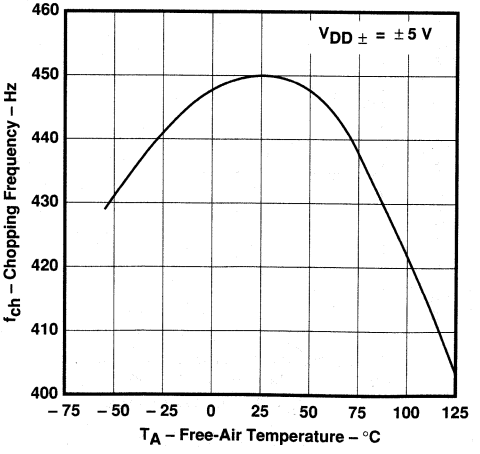


FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

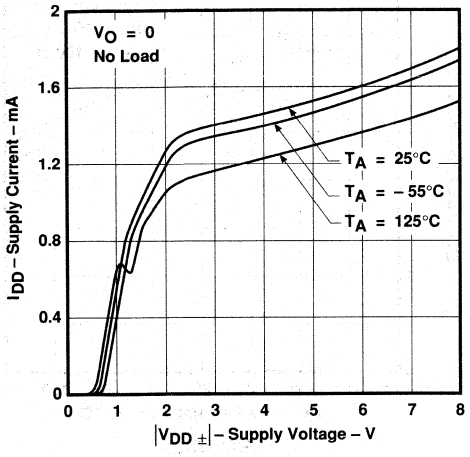


FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

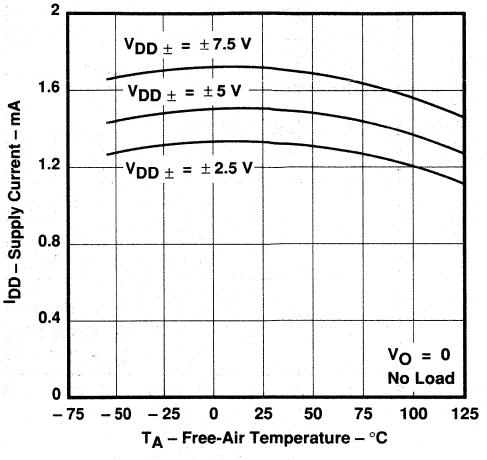


FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

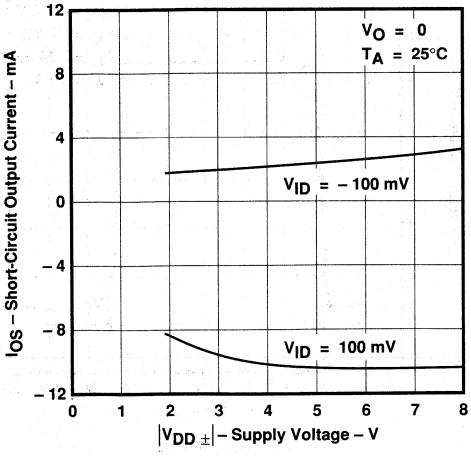


FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

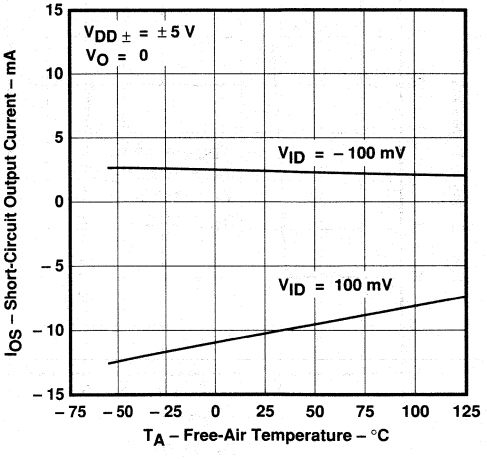


FIGURE 20

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

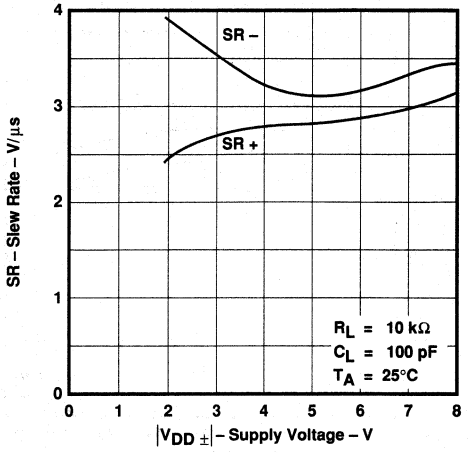


FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

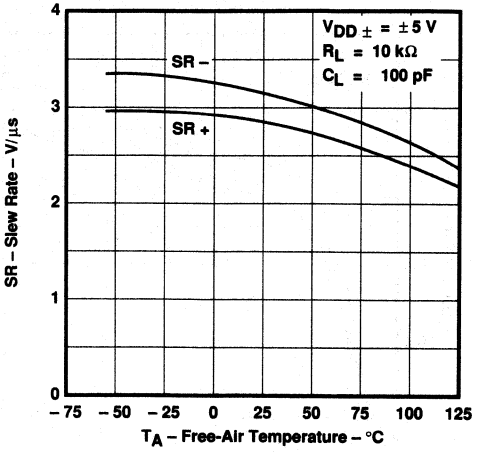


FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

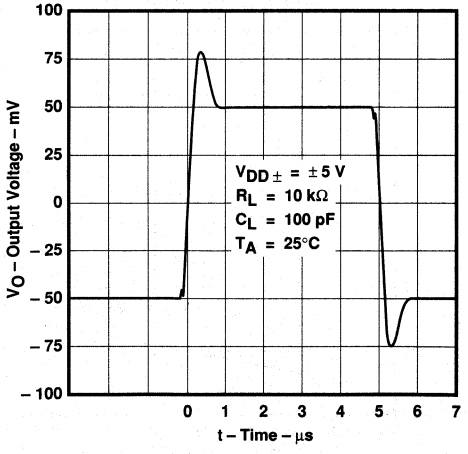


FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

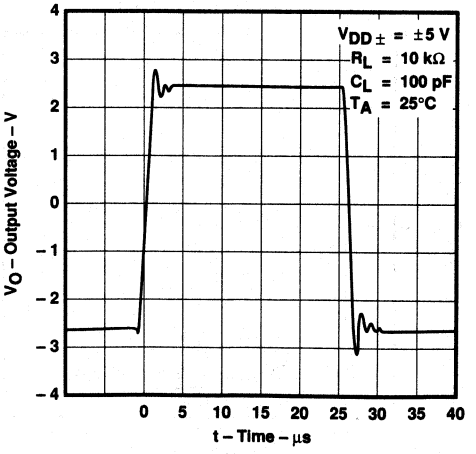


FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

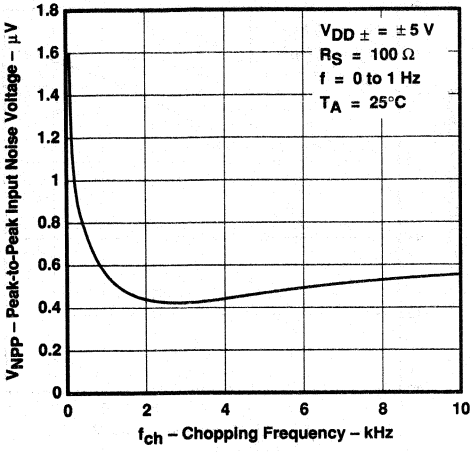


FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

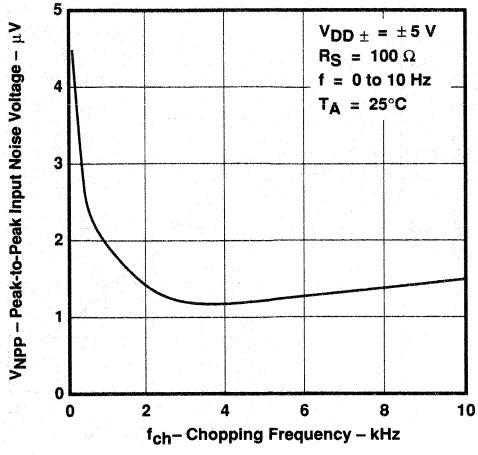


FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

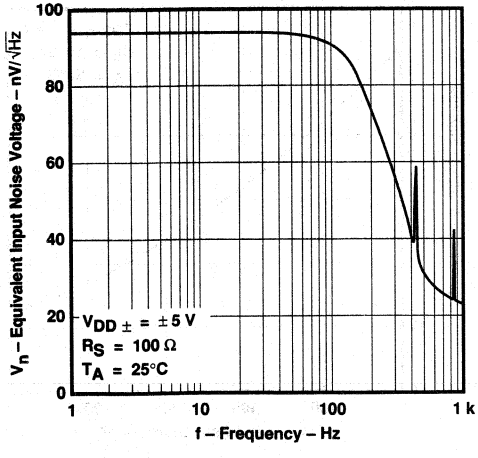


FIGURE 27

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

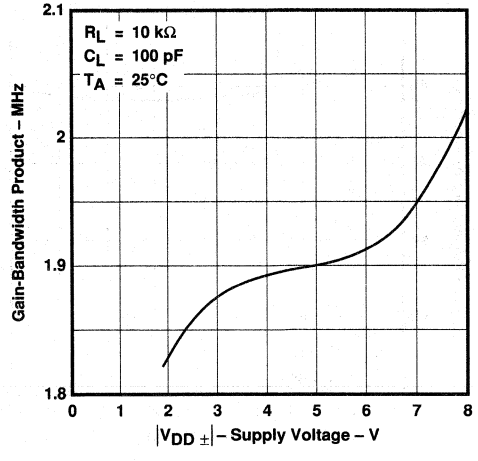


FIGURE 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

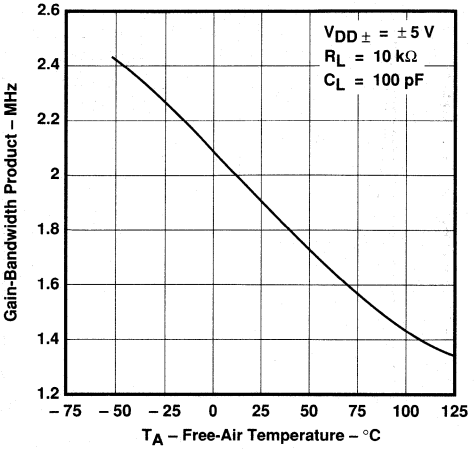


FIGURE 29

PHASE MARGIN
vs
SUPPLY VOLTAGE

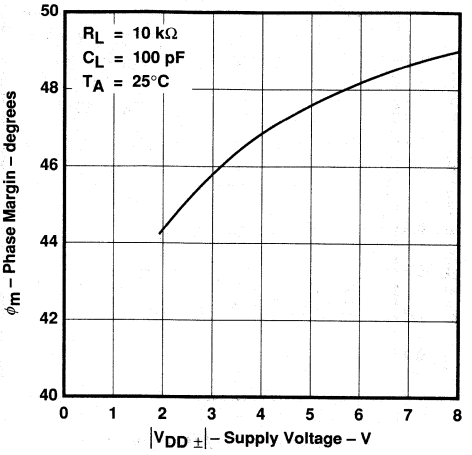


FIGURE 30

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

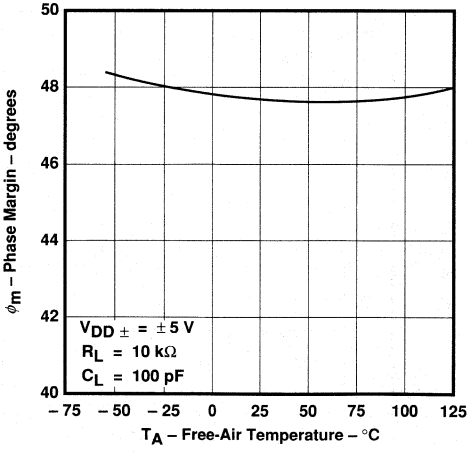


FIGURE 31

PHASE MARGIN
vs
LOAD CAPACITANCE

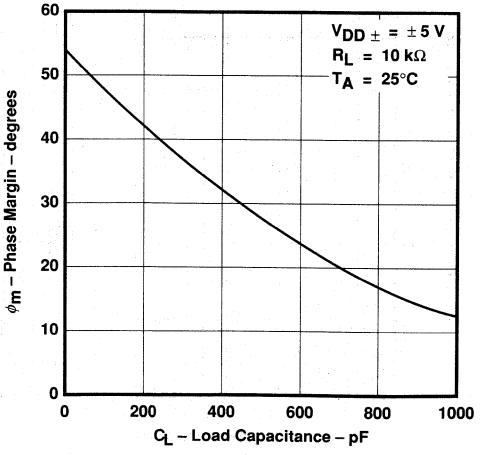


FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL APPLICATION DATA

apacitor selection and placement

The two important factors to consider when selecting external capacitors C_{XA} and C_{XB} are leakage and dielectric absorption. Both factors can cause system degradation that can negate the performance advantages realized by using the TLC2652.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at $T_A = 125°C$. In addition, guardbands are recommended around the capacitor connections on both sides of the printed circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset voltage is needed, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2652 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 μF to 1 μF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin will cause degradation in the noise performance. This problem is eliminated on the TLC2652.

nternal/external clock

The TLC2652 has an internal clock that sets the chopping frequency to a nominal value of 450 Hz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 450-Hz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. If this level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. When operating in the single-supply configuration, this feature allows the TLC2652 to be driven directly by 5-V TTL and CMOS logic. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin. The duty cycle of the external clock is not critical but should be kept between 30% and 60%.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2652, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2652 is significantly faster than competitive products; however, if required, this time can be

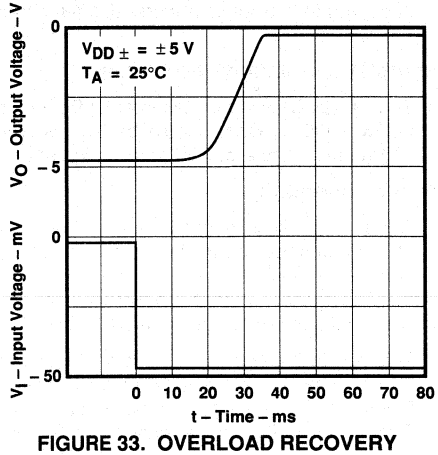


FIGURE 33. OVERLOAD RECOVERY

reduced further by using internal clamp circuitry accessible through the CLAMP pin.
The clamp is simply a switch that is automatically activated when the output is approximately 1 V from eithe supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed- loop gain is reduced and the TLC2652 output is prevented from going into saturation. Since the outpu must source or sink current through the switch (see Figure 7), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage drift of the TLC2652, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each othe (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greate than the 0.003 μV °C typical of the TLC2652).

To help minimize thermoelectric effects, careful attention should be paid to component selection and circui board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the inpu signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptable to latchup due to their inherent parasitic thyristors, the TLC2652 inputs and output were designed to withstand –100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as is possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2652 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2652 on-chip control logic produces two dominant clock phases; a nulling phase and an amplifying phase. The term *chopper-stabilized* derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2652. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the

TYPICAL APPLICATION DATA

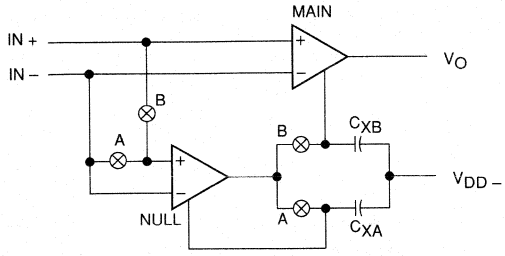


FIGURE 34. TLC2652 SIMPLIFIED BLOCK DIAGRAM

nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power-supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process with its low-noise analog MOS transistors and patent-pending input stage design significantly reduces the input noise voltage.

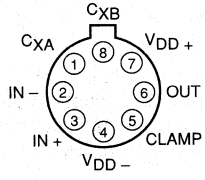
The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches.

As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2652 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2652 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

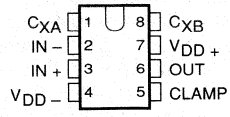
- Input Noise Voltage ...
  0.5 μV p-p Typ, f = 0 to 1 Hz
  1.5 μV p-p Typ, f = 0 to 10 Hz
  47 nV/√Hz Typ, f = 10 Hz
  13 nV/√Hz Typ, f = 1 kHz
- High Chopping Frequency ... 10 kHz Typ
- No Clock Noise Below 10 kHz
- No Intermodulation Error Below 5 kHz
- Low Input Offset Voltage ... 10 μV Max
- Excellent Offset Voltage Stability with Temperature ... 0.3 μV/°C Max
- A_{VD} ... 135 dB Min
- CMRR ... 110 dB Min
- k_{SVR} ... 120 dB Min
- Single-Supply Operation
- Common-Mode Input Voltage Range Includes the Negative Rail
- No Noise Degradation with External Capacitors Connected to V_{DD-}

L PACKAGE
(TOP VIEW)

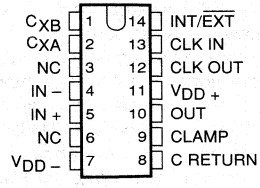


Pin 4 of the L package is in electrical contact with the case

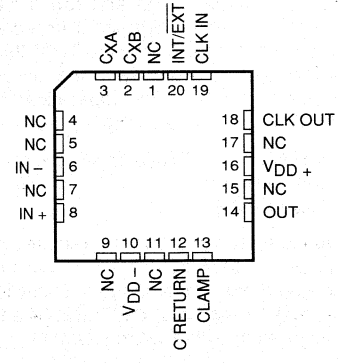
D008, JG, or P PACKAGE
(TOP VIEW)



D014, J, or N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE							
		8-PIN				14-PIN			20-PIN
		SMALL-OUTLINE (D008)	PLASTIC DIP (P)	CERAMIC DIP (JG)	METAL CAN (L)	SMALL-OUTLINE (D014)	PLASTIC DIP (N)	CERAMIC DIP (J)	CHIP CARRIER (FK)
0°C to 70°C	10 μV	TLC2654AC-8D	TLC2654ACP	TLC2654ACJG	TLC2654ACL	TLC2654AC-14D	TLC2654ACN	TLC2654ACJ	—
	20 μV	TLC2654C-8D	TLC2654CP	TLC2654CJG	TLC2654CL	TLC2654C-14D	TLC2654CN	TLC2654CJ	—
– 40°C to 85°C	10 μV	TLC2654AI-8D	TLC2654AIP	TLC2654AIJG	TLC2654AIL	TLC2654AI-14D	TLC2654AIN	TLC2654AIJ	—
	20 μV	TLC2654I-8D	TLC2654IP	TLC2654IJG	TLC2654IL	TLC2654I-14D	TLC2654IN	TLC2654IJ	—
– 55°C to 125°C	10 μV	TLC2654AM-8D	TLC2654AMP	TLC2654AMJG	TLC2654AML	TLC2654AM-14D	TLC2654AMN	TLC2654AMJ	TLC2654AMFK
	20 μV	TLC2654M-8D	TLC2654MP	TLC2654MJG	TLC2654ML	TLC2654M-14D	TLC2654MN	TLC2654MJ	TLC2654MFK

D008 and D014 packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., TLC2654AC-8DR).

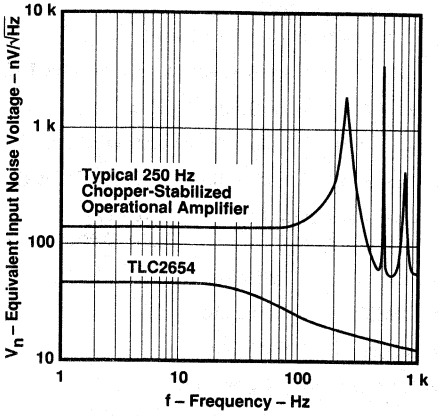
Advanced LinCMOS is a trademark of Texas Instruments Incorporated.

description

The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper stabilization circuitry makes possible excellent dc precision. In addition, circuit techniques have been added that give the TLC2654 and TLC2654A noise performance unsurpassed by similar devices.

Chopper stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power supply voltage. The high chopping frequency of the TLC2654 and TLC2654A provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, make the TLC2654 and TLC2654A an ideal choice for a broad range of applications such as low-level low-frequency thermocouple amplifiers and strain gauges, as well as wide-bandwidth and subsonic circuits. (For applications requiring even greater dc precision, use the TLC2652 or TLC2652A device, which has a chopping frequency of 450 Hz.)

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ±2.3 V.

Two external capacitors are required to operate the device; however, the on-chip chopper control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2654 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time further.

The device inputs and output are designed to withstand –100 mA surge currents without sustaining latchup. In addition, the TLC2654 and TLC2654A incorporate internal ESD protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The C-suffix devices are characterized for operation from 0°C to 70°C.

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absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{DD+} (see Note 1) . . . . . 8 V
Supply voltage, V_{DD-} (see Note 1) . . . . . −8 V
Differential input voltage (see Note 2) . . . . . ±16 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±8 V
Voltage on CLK IN and INT/$\overline{EXT}$ pins . . . . . V_{DD-} to V_{DD-} + 5.2 V
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . Unlimited
Current into CLK IN and INT/$\overline{EXT}$ pins . . . . . ±5 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
I-suffix . . . . . −40°C to 85°C
C-suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J, JG, or L package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D008	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D014	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
L	650 mW	5.2 mW/°C	416 mW	338 mW	130 mW
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	315 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	M-SUFFIX		I-SUFFIX		C-SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	±2.3	±8	±2.3	±8	±2.3	±8	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} − 2.3	V_{DD-}	V_{DD+} − 2.3	V_{DD-}	V_{DD+} − 2.3	V
Clock input voltage	V_{DD-}	V_{DD-} + 5	V_{DD-}	V_{DD-} + 5	V_{DD-}	V_{DD-} + 5	V
Operating free-air temperature, T_A	−55	125	−40	85	0	70	°C

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		4	10		5	20	μV
			Full range			40			50	
α_{VIO}	Temperature coefficient of input offset voltage		– 55°C to 125°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			500			500	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			500			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	– 5 to 2.7			– 5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	– 4.7	– 4.9		– 4.7	– 4.9		V
			Full range	– 4.7			– 4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	155		120	155		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	V_O = – 4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	125		110	125		dB
			Full range	115			105			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is – 55°C to 125°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

operating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AM			TLC2654M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.1			1.1			
SR−	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.3			1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		47			47		nV/√Hz
		f = 1 kHz	25°C		13			13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†Full range is − 55°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AI			TLC2654I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		4	10		5	20	μV
			Full range			30			40	
α_{VIO}	Temperature coefficient of input offset voltage		−40°C to 85°C		0.004	0.3		0.004	0.3	μV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	μV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			200			200	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			200			200	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	155		120	155		dB
			Full range	125			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			μA
			Full range	25			25			
	Clamp off-state current	V_O = −4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}$ / ΔV_{IO})	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is −40°C to 85°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

›perating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC2654AI			TLC2654I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.2			1.2			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.5			1.5			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1 kHz	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

Full range is – 40°C to 85°C.

NOTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted

PARAMETER		TEST CONDITIONS†		TLC2654AC			TLC2654C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		4	10		5	20	µV
			Full range			24			34	
α_{VIO}	Temperature coefficient of input offset voltage		0°C to 70°C		0.004	0.3		0.004	0.3	µV/°C
	Input offset voltage long-term drift (see Note 4)		25°C		0.003	0.02		0.003	0.06	µV/mo
I_{IO}	Input offset current		25°C		30			30		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		50			50		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	4.7	4.8		4.7	4.8		V
			Full range	4.7			4.7			
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10 kΩ, See Note 5	25°C	−4.7	−4.9		−4.7	−4.9		V
			Full range	−4.7			−4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	135	155		120	155		dB
			Full range	130			120			
f_{ch}	Internal chopping frequency		25°C		10			10		kHz
	Clamp on-state current	R_L = 100 kΩ	25°C	25			25			µA
			Full range	25			25			
	Clamp off-state current	V_O = −4 V to 4 V	25°C			100			100	pA
			Full range			100			100	
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	110	125		105	125		dB
			Full range	110			105			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm}$ = ±2.3 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	125		110	125		dB
			Full range	120			110			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.5	2.1		1.5	2.1	mA
			Full range			2.2			2.2	

†Full range is 0°C to 70°C.

NOTES: 4. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

5. Output clamp is not connected.

perating characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		TLC2654AC			TLC2654C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.3			1.3			
SR −	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.7			1.7			
V_n	Equivalent input noise voltage (see Note 6)	f = 10 Hz	25°C		47	75		47		nV/√Hz
		f = 1 kHz	25°C		13	20		13		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C		0.5			0.5		μV
		f = 0 to 10 Hz	25°C		1.5			1.5		
I_n	Equivalent input noise current	f = 1 kHz	25°C		0.004			0.004		pA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF	25°C		1.9			1.9		MHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°			48°		

†ull range is 0°C to 70°C.

OTE 6: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1
	Normalized input offset voltage	vs Chopping frequency	2
I_{IO}	Input offset current	vs Chopping frequency	3
		vs Temperature	4
I_{IB}	Input bias current	vs Common-mode voltage	5
		vs Chopping frequency	6
		vs Temperature	7
	Clamp current	vs Output voltage	8
V_{OM}	Maximum peak output voltage swing	vs Output current	9
		vs Temperature	10
V_{OPP}	Maximum peak-to-peak output voltage swing	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
A_{VD}	Differential voltage amplification	vs Frequency	13
		vs Temperature	14
f_{ch}	Chopping frequency	vs Supply voltage	15
		vs Temperature	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
I_{OS}	Short-circuit output current	vs Supply voltage	19
		vs Temperature	20
SR	Slew rate	vs Supply voltage	21
		vs Temperature	22
	Pulse response	Small-signal	23
		Large-signal	24
V_{NPP}	Peak-to-peak equivalent input noise voltage	vs Chopping frequency	25, 26
V_n	Equivalent input noise voltage	vs Frequency	27
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	28
	Gain-bandwidth product	vs Supply voltage	29
		vs Temperature	30
	Phase margin	vs Supply voltage	31
		vs Temperature	32
ϕ_m	Phase shift	vs Frequency	13

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF TLC2654
INPUT OFFSET VOLTAGE

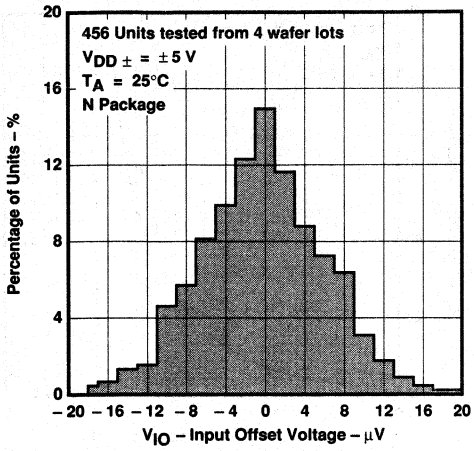

FIGURE 1

NORMALIZED INPUT OFFSET VOLTAGE
VS
CHOPPING FREQUENCY

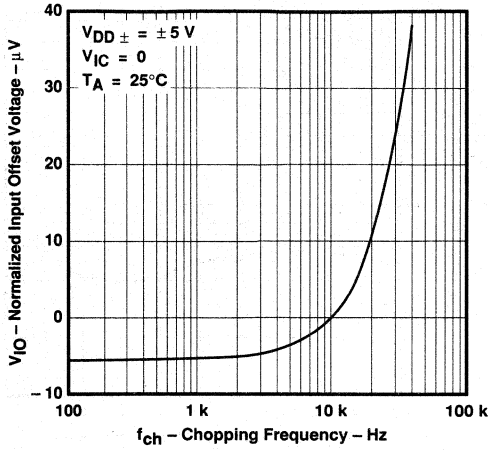

FIGURE 2

INPUT OFFSET CURRENT
VS
CHOPPING FREQUENCY

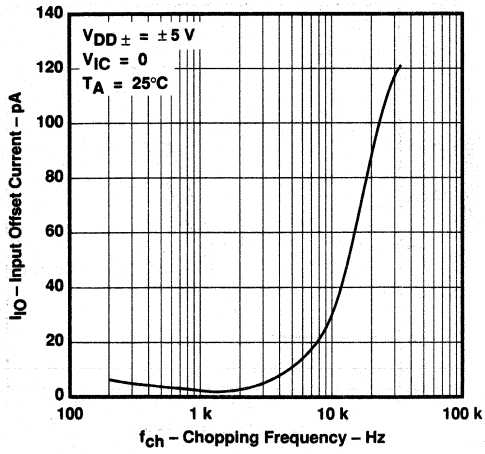

FIGURE 3

INPUT OFFSET CURRENT
VS
FREE-AIR TEMPERATURE

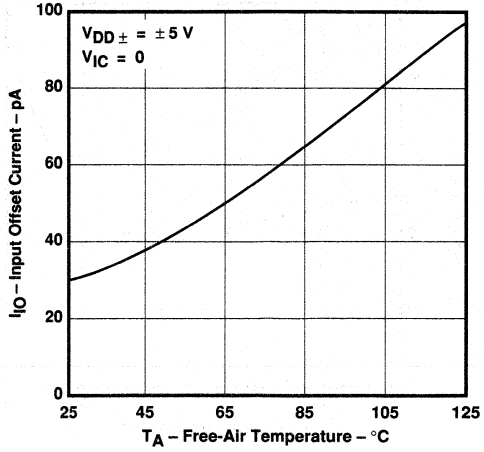

FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

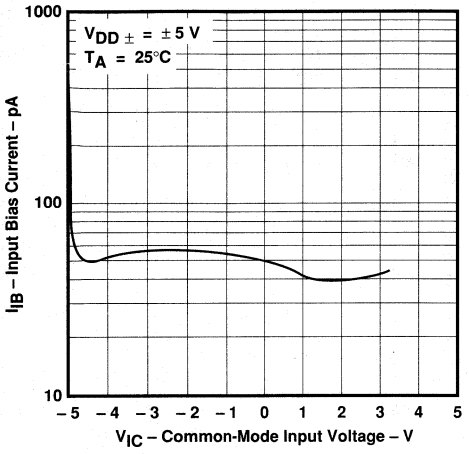

FIGURE 5

INPUT BIAS CURRENT
vs
CHOPPING FREQUENCY

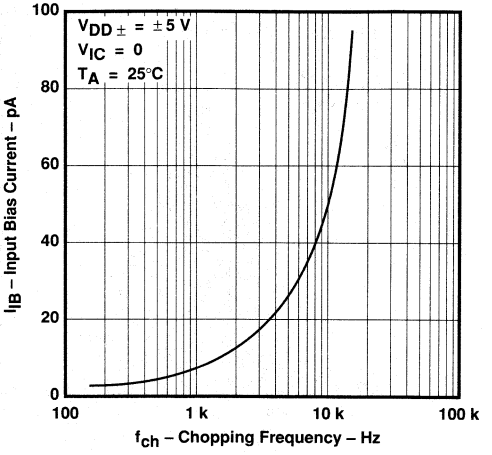

FIGURE 6

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

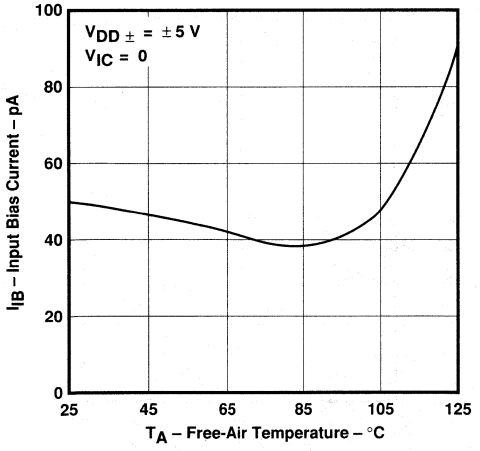

FIGURE 7

CLAMP CURRENT
vs
OUTPUT VOLTAGE

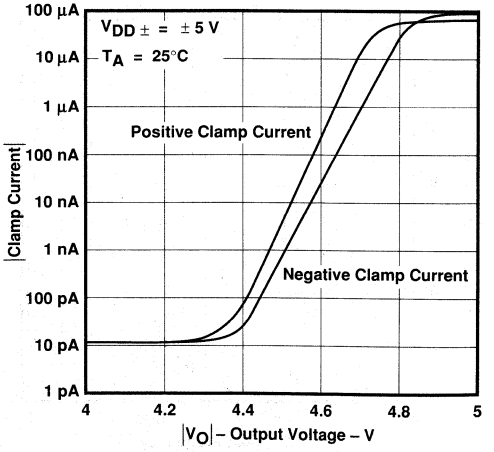

FIGURE 8

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT

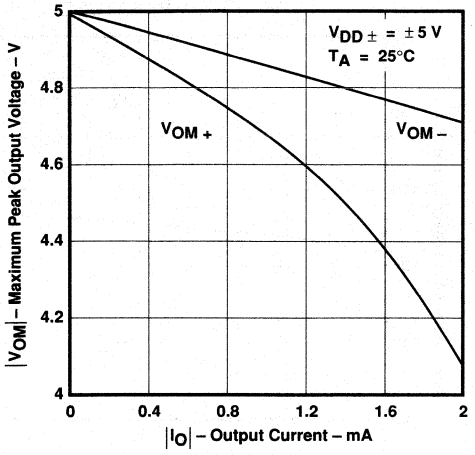

FIGURE 9

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

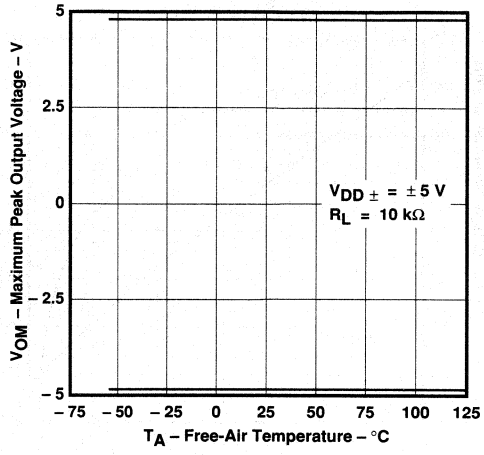

FIGURE 10

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

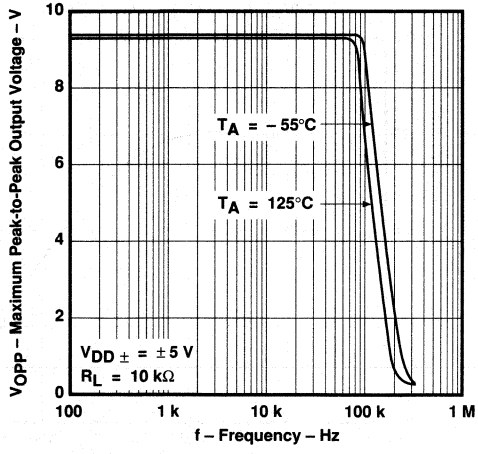

FIGURE 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

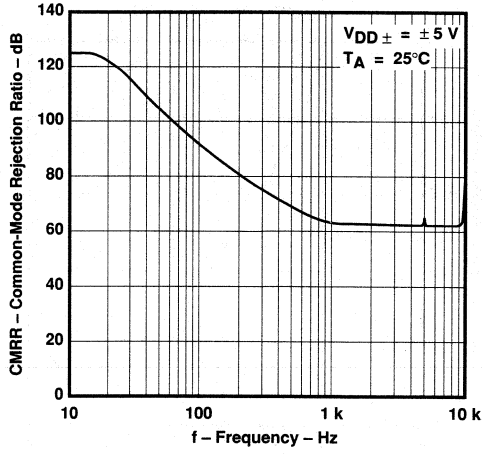

FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

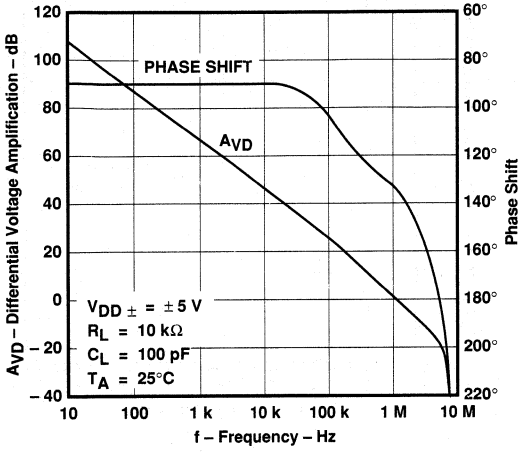

FIGURE 13

LARGE-SIGNAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

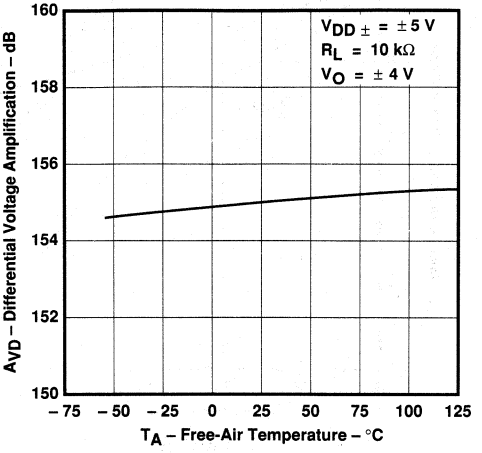

FIGURE 14

CHOPPING FREQUENCY
vs
SUPPLY VOLTAGE

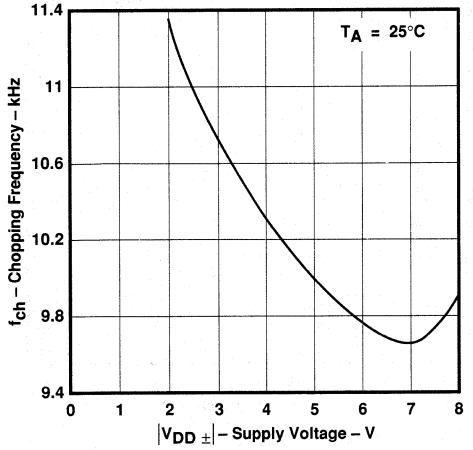

FIGURE 15

CHOPPING FREQUENCY
vs
FREE-AIR TEMPERATURE

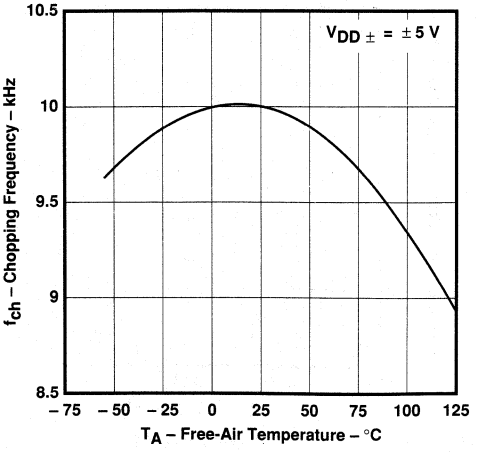

FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

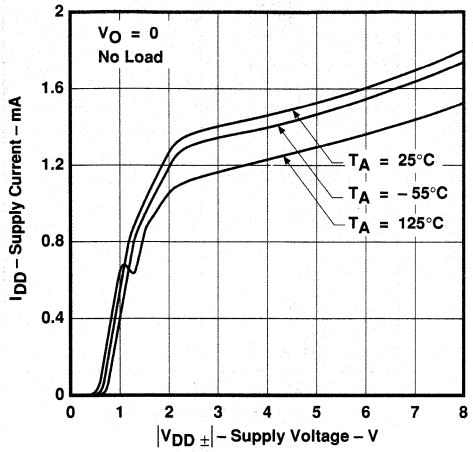

FIGURE 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

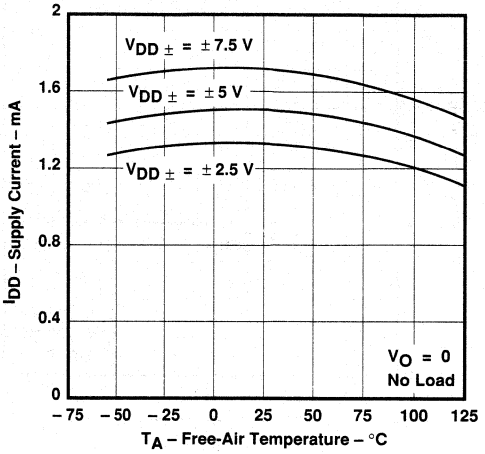

FIGURE 18

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

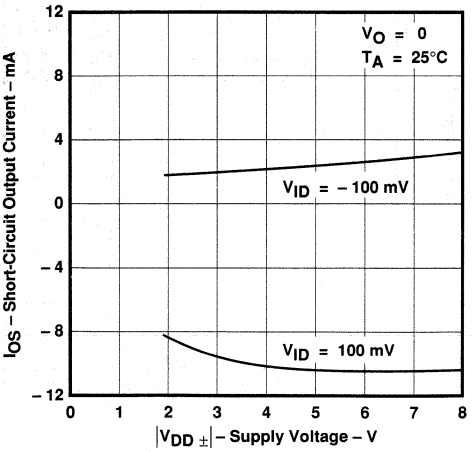

FIGURE 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

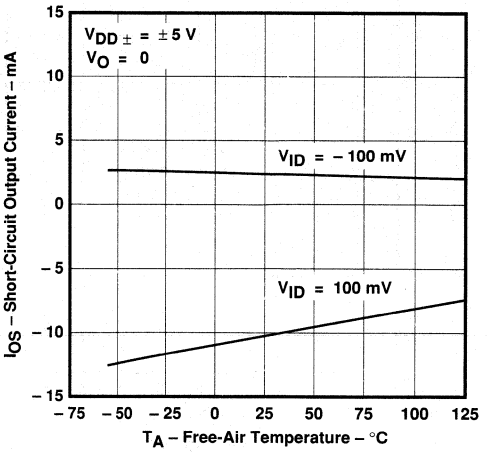

FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SLEW RATE
vs
SUPPLY VOLTAGE

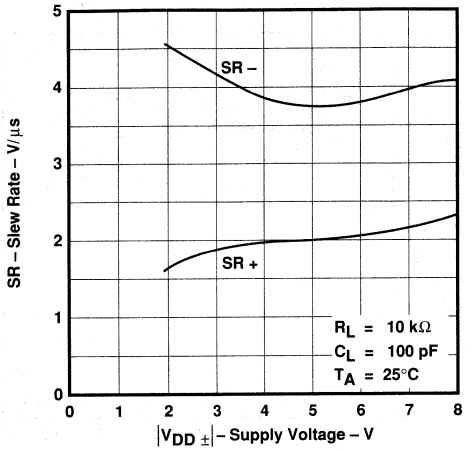

FIGURE 21

SLEW RATE
vs
FREE-AIR TEMPERATURE

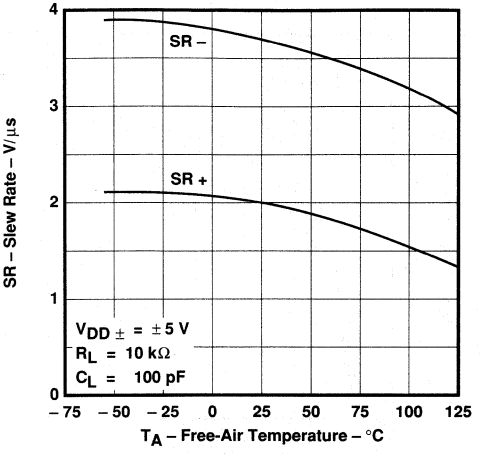

FIGURE 22

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

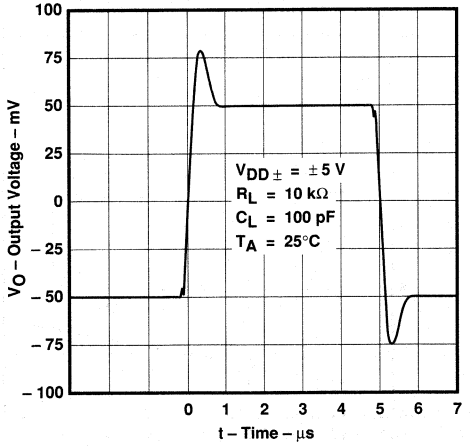

FIGURE 23

VOLTAGE-FOLLOWER
LARGE-SIGNAL
PULSE RESPONSE

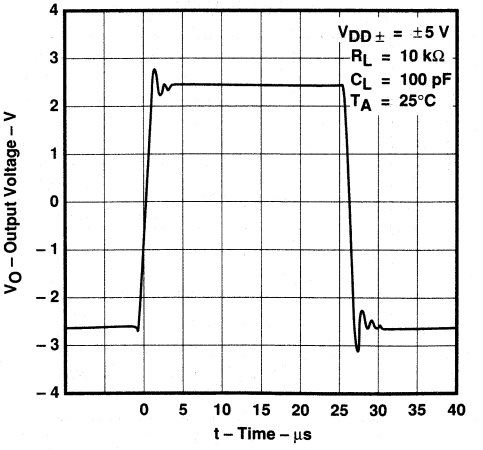

FIGURE 24

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

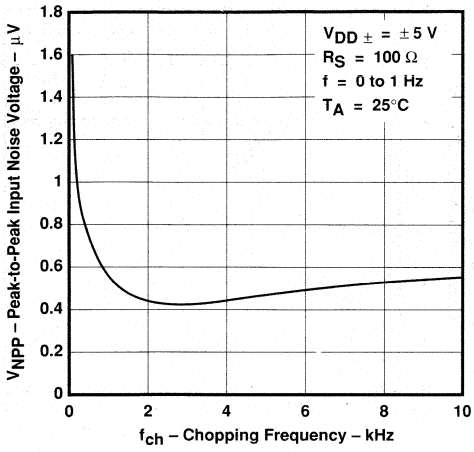

FIGURE 25

PEAK-TO-PEAK INPUT NOISE VOLTAGE
vs
CHOPPING FREQUENCY

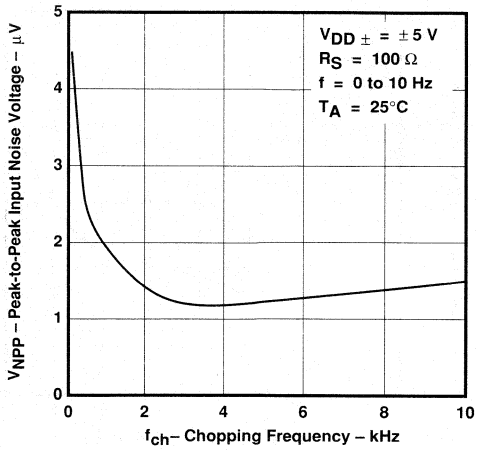

FIGURE 26

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

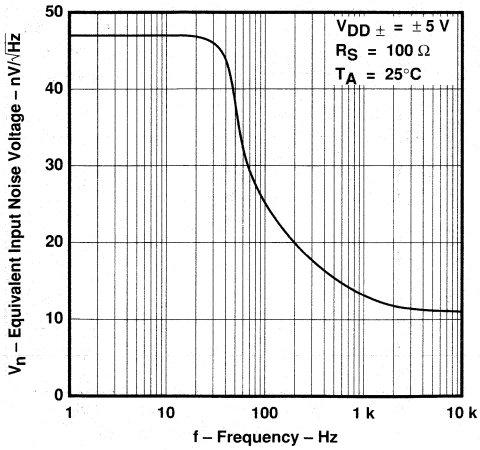

FIGURE 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

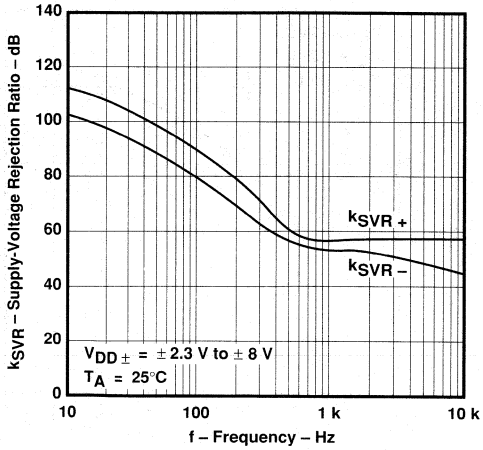

FIGURE 28

TYPICAL CHARACTERISTICS†

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

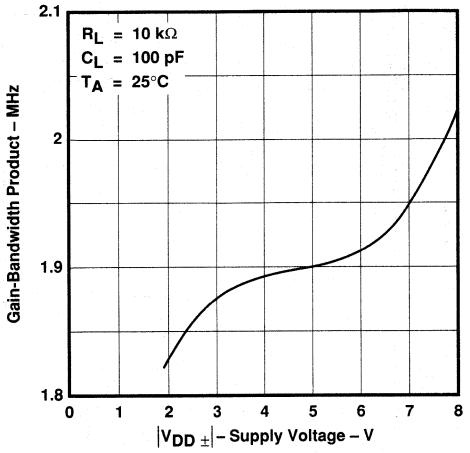

FIGURE 29

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

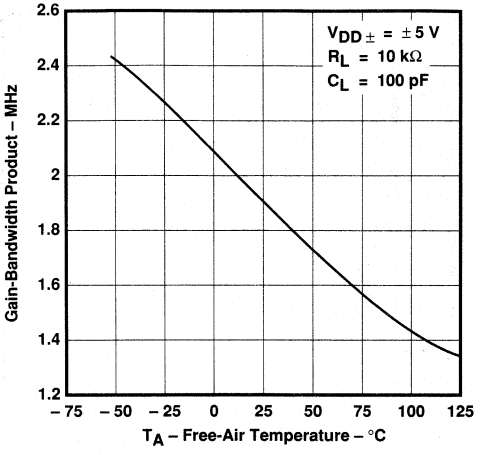

FIGURE 30

PHASE MARGIN
vs
SUPPLY VOLTAGE

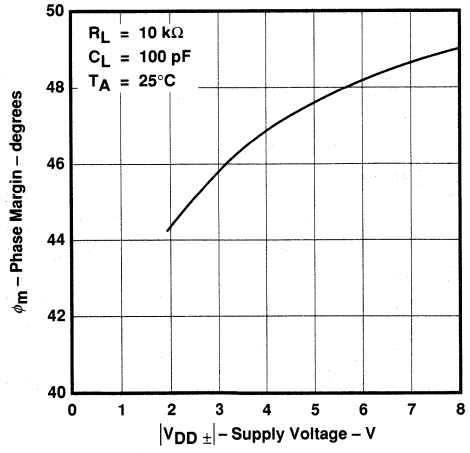

FIGURE 31

PHASE MARGIN
vs
LOAD CAPACITANCE

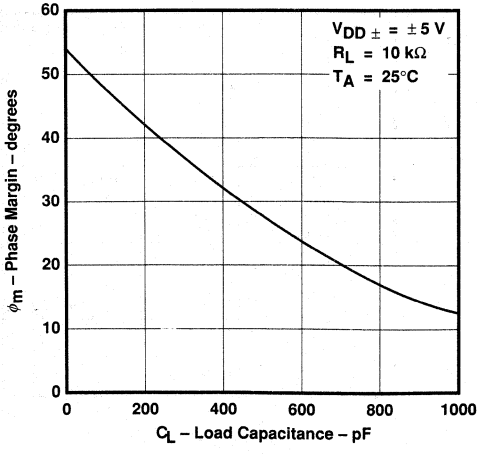

FIGURE 32

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL APPLICATION DATA

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB}. Both factors can cause system degradation negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands around the capacitor connections on both sides of the printed circuit board are recommended to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input offset voltage, it is recommended that high-quality film capacitors, such as mylar, polystyrene, or polypropylene, be used. In other applications, however, a ceramic or other low-grade capacitor may suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of 0.1 µF to 1 µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that on many choppers, connecting these capacitors to the V_{DD-} pin causes degradation in noise performance, a problem that is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package, the device chopping frequency may be set by the internal clock or controlled externally by use of the INT/$\overline{\text{EXT}}$ and CLK IN pins. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect the INT/$\overline{\text{EXT}}$ pin to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, the CLK IN pin may be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into the CLK IN pin is limited to ±5 mA. A divide-by-two frequency divider interfaces with the CLK IN pin and sets the chopping frequency. The chopping frequency appears on the CLK OUT pin.

overload recovery/output clamp

When large differential input voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 33). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, if required, this time can be reduced further by use of internal clamp circuitry accessible through the CLAMP pin.

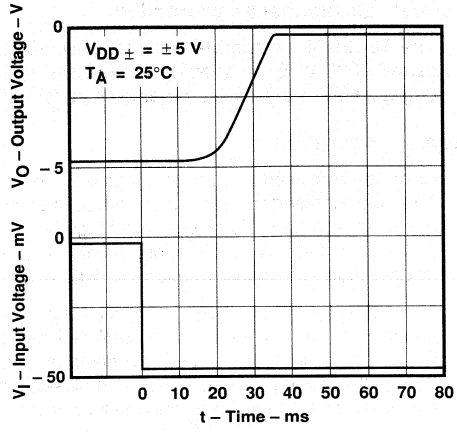

FIGURE 33. OVERLOAD RECOVERY

TYPICAL APPLICATION DATA

The clamp is simply a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 8), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01-μV/°C typical of the TLC2654).

To help minimize thermoelectric effects, careful attention should be paid to componet selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latchup avoidance

Because CMOS devices are susceptible to latchup due to their inherent parasitic thyristors, the TLC2654 inputs and output are designed to withstand –100-mA surge currents without sustaining latchup; however, techniques to reduce the chance of latchup should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by using decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latchup occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latchup occurring increases with increasing temperature and supply voltage.

electrostatic discharge protection

The TLC2654 incorporates internal ESD protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers – a main amplifier and a nulling amplifier – plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the nV/°C range.

The TLC2654 on-chip control logic produces two dominant clock phases – a nulling phase and an amplifying phase. The term "chopper-stabilized" derives from the process of switching between these two clock phases. Figure 34 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types. During the nulling phase, switch A is closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input

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TYPICAL APPLICATION DATA

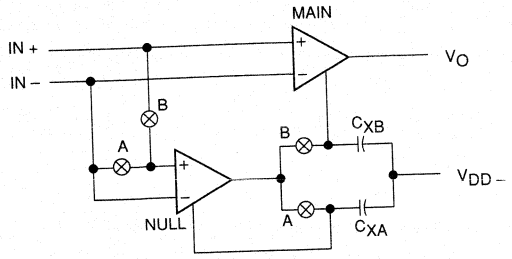


FIGURE 34. TLC2654 SIMPLIFIED BLOCK DIAGRAM

node. Simultaneously, external capacitor C_{XA} stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switch B is closed, connecting the output of the nulling amplifier to a noninverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor C_{XB} stores the nulling potential to allow the offset voltage of the main amplifier to remain nulled during the next nulling phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common-mode input voltage range and power supply range. In addition, because the low-frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low-frequency noise of a chopper amplifier depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The use of the Advanced LinCMOS process, with its low-noise analog MOS transistors and patent-pending input stage design, significantly reduces the input noise voltage.

The primary source of nonideal operation in chopper-stabilized amplifiers is error charge from the switches. As charge imbalance accumulates on critical nodes, input offset voltage can increase, especially with increasing chopping frequency. This problem has been significantly reduced in the TLC2654 by use of a patent-pending compensation circuit and the Advanced LinCMOS process.

The TLC2654 incorporates a feed-forward design that ensures continuous frequency response. Essentially, the gain magnitude of the nulling amplifier and compensation network crosses unity at the break frequency of the main amplifier. As a result, the high-frequency response of the system is the same as the frequency response of the main amplifier. This approach also ensures that the slewing characteristics remain the same during both the nulling and amplifying phases.

The primary limitation on ac performance is the chopping frequency. As the input signal frequency approaches the chopper's clock frequency, intermodulation (or aliasing) errors result from the mixing of these frequencies. To avoid these error signals, the input frequency must be less than half the clock frequency. Most choppers available today limit the internal chopping frequency to less than 500 Hz in order to eliminate errors due to the charge imbalancing phenomenon mentioned previously. However, to avoid intermodulation errors on a 500-Hz chopper, the input signal frequency must be limited to less than 250 Hz. The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

D942, FEBRUARY 1971 REVISED MAY 1988

- **Common-Mode Input Range . . . ±10 V Typical**
- **Designed to be Interchangeable with Fairchild μA709A, μA709, and μA709C**
- **Maximum Peak-to-Peak Output Voltage Swing . . . 28-V Typical with 15-V Supplies**

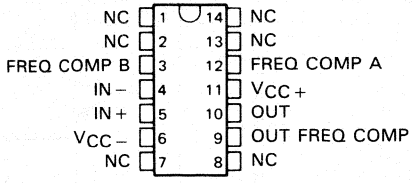
description

These circuits are general-purpose operational amplifiers, each having high-impedance differential inputs and a low-impedance output. Component matching, inherent with silicon monolithic circuit-fabrication techniques, produces an amplifier with low-drift and low-offset characteristics. Provisions are incorporated within the circuit whereby external components may be used to compensate the amplifier for stable operation under various feedback or load conditions. These amplifiers are particularly useful for applications requiring transfer or generation of linear or nonlinear functions.

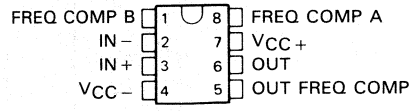
The uA709A circuit features improved offset characteristics, reduced input-current requirements, and lower power dissipation when compared to the uA709 circuit. In addition, maximum values of the average temperature coefficients of offset voltage and current are specified for the uA709A.

The uA709AM and uA709M are characterized for operation over the full military temperature range of −55°C to 125°C. The uA709C is characterized for operation from 0°C to 70°C.

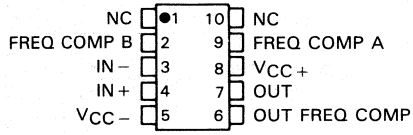
uA709AM, uA709M . . . J OR W PACKAGE
(TOP VIEW)



uA709AM, uA709M . . . JG PACKAGE
uA709C . . . D, JG, OR P PACKAGE
(TOP VIEW)

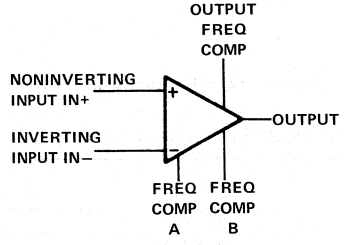


uA709AM, uA709M . . . U FLAT PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

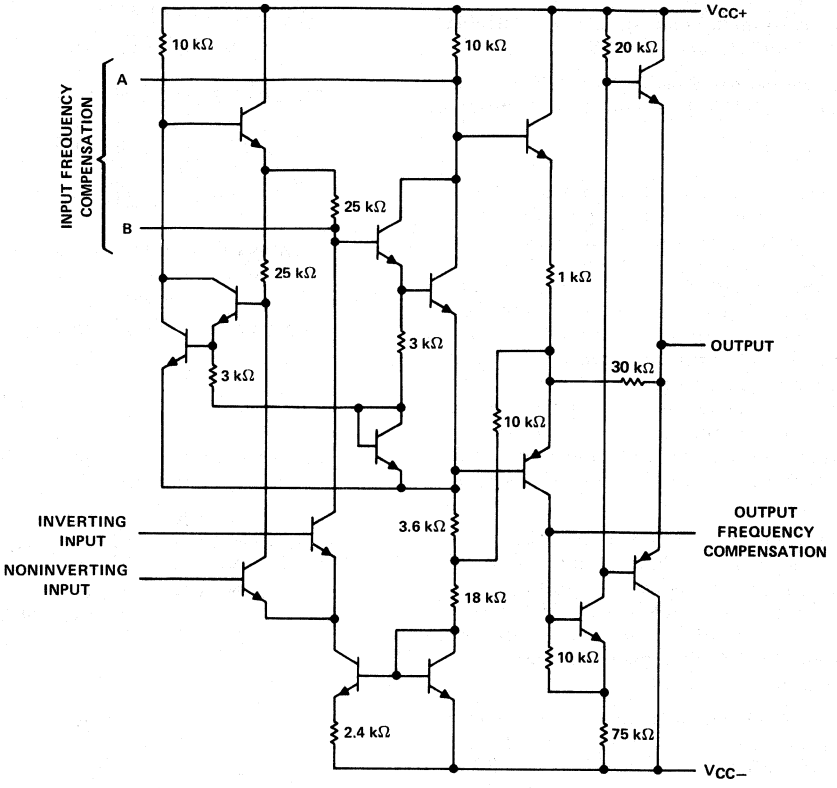


AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE					
		SMALL OUTLINE (D)	CERAMIC (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	FLAT PACK (U)	FLAT PACK (W)
0°C to 70°C	7.5 mV	uA709CD	—	uA709CJG	uA709CP	—	—
−55°C to 125°C	5 mV	—	uA709MJ	uA709MJG	—	uA709MU	uA709MW
	2 mV		uA709AMJ	uA709AMJG		uA709AMU	uA709AMW

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., uA709CDR)

schematic



Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA709AM uA709M	uA709C	UNIT
Supply voltage V_{CC+} (see Note 1)		18	18	V
Supply voltage V_{CC-} (see Note 1)		−18	−18	V
Differential input voltage (see Note 2)		±5	±5	V
Input voltage (either input, see Notes 1 and 3)		±10	±10	V
Duration of output short-circuit (see Note 4)		5	5	s
Continuous total dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 10 V, whichever is less.
4. The output may be shorted to ground or either power supply.

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DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	300 mW	N/A	N/A	300 mW	N/A
J (uA709__M)	300 mW	11.0 mW/°C	123°C	300 mW	275 mW
JG (uA709__M)	300 mW	8.4 mW/°C	114°C	300 mW	210 mW
JG (uA709C)	300 mW	N/A	N/A	300 mW	N/A
P	300 mW	N/A	N/A	300 mW	N/A
U	300 mW	5.4 mW/°C	94°C	300 mW	135 mW
W	300 mW	8.0 mW/°C	113°C	300 mW	200 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±9 V to ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			uA709AM			uA709M			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	V_O = 0	$R_S \le 10$ kΩ	25°C		0.6	2		1	5	mV
				Full range			3			6	
α_{VIO}	Average temperature coefficient of input offset voltage	V_O = 0,	R_S = 50 Ω	Full range		1.8	10		3		μV/°C
		V_O = 0,	R_S = 10 kΩ	Full range		4.8	25		6		
I_{IO}	Input offset current	V_O = 0		25°C		10	50		50	200	nA
				−55°C		40	250		100	500	
				125°C		3.5	50		20	200	
α_{IIO}	Average temperature coefficient of input offset current	V_O = 0		−55°C to 25°C		0.45	2.8				nA/°C
				25°C to 125°C		0.08	0.5				
I_{IB}	Input bias current	V_O = 0		25°C		0.1	0.2		0.2	0.5	μA
				−55°C		0.3	0.6		0.5	1.5	
V_{ICR}	Common-mode input voltage range	$V_{CC\pm}$ = ±15 V		25°C	±8	±10		±8	±10		V
				Full range	±8			±8			
V_{OPP}	Maximum peak-to-peak output voltage swing	$V_{CC\pm}$ = ±15 V,	$R_L \ge 10$ kΩ	25°C	24	28		24	28		V
				Full range	24			24			
		$V_{CC\pm}$ = ±15 V,	R_L = 2 kΩ	25°C	20	26		20	26		
		$V_{CC\pm}$ = ±15 V,	$R_L \ge 2$ kΩ	Full range	20			20			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±15 V, V_O = ±10 V	$R_L \ge 2$ kΩ,	25°C		45			45		V/mV
				Full range	25		70	25		70	
r_i	Input resistance			25°C	350	750		150	400		kΩ
				−55°C	85	185		40	100		
r_o	Output resistance	V_O = 0,	See Note 5	25°C		150			150		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min		25°C	80	110		70	90		dB
				Full range	80			70			
k_{SVS}	Power supply sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V		25°C		40	100		25	150	μV/V
				Full range			100			150	
I_{CC}	Supply current	$V_{CC\pm}$ = ±15 V, No load, V_O = 0		25°C		2.5	3.6		2.6	5.5	mA
				−55°C		2.7	4.5				
				125°C		2.1	3				
P_D	Total power dissipation	$V_{CC\pm}$ = ±15 V, No load, V_O = 0		25°C		75	108		78	165	mW
				−55°C		81	135				
				125°C		63	90				

†All characteristics are specified under open-loop with zero common-mode input voltage unless otherwise specified. Full range for uA709AM and uA709M is −55°C to 125°C.
‡All typical values are at $V_{CC\pm}$ = ±15 V.
NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

electrical characteristics at specified free-air temperature (unless otherwise noted $V_{CC\pm}$ = ±15 V)

PARAMETER		TEST CONDITIONS†			uA709C MIN	uA709C TYP	uA709C MAX	UNIT
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C		2	7.5	mV
				Full range			10	
I_{IO}	Input offset current	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C		100	500	nA
				Full range			750	
I_{IB}	Input bias current	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		25°C		0.3	1.5	μA
				Full range			2	
V_{ICR}	Common-mode input voltage range			25°C	±8	±10		V
V_{OPP}	Maximum peak-to-peak output voltage swing	R_L ≥ 10 kΩ		25°C	24	28		V
				Full range	24			
		R_L = 2 kΩ		25°C	20	26		
		R_L ≥ 2 kΩ		Full range	20			
A_{VD}	Large-signal differential voltage amplification	R_L ≤ 2 kΩ,	V_O = ±10 V	25°C	15	45		V/mV
				Full range	12			
r_i	Input resistance			25°C	50	250		kΩ
				Full range	35			
r_o	Output resistance	V_O = 0,	See Note 5	25°C		150		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min		25°C	65	90		dB
k_{SVS}	Supply voltage sensitivity	V_{CC} = ±9 V to ±15 V		25°C		25	200	μV/V
P_D	Total power dissipation	V_O = 0,	No load	25°C		80	200	mW

† All characteristics are specified under open-loop operation with zero volts common-mode voltage unless otherwise specified. Full range for uA709C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics $V_{CC\pm}$ = ±9 V to ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		uA709AM uA709M uA709C MIN	TYP	MAX	UNIT
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, See Figure 1	C_L = 0		0.3	1	μs
	Overshoot factor		C_L = 100 pF		6%	30%	

PARAMETER MEASUREMENT INFORMATION

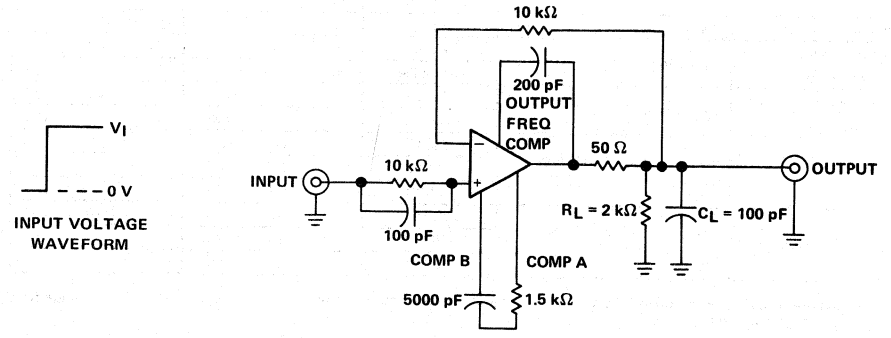

FIGURE 1. RISE TIME AND SLEW RATE

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D920, NOVEMBER 1970—REVISED NOVEMBER 1988

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-up**
- **Designed to be Interchangeable with Fairchild μA741M, μA741C**

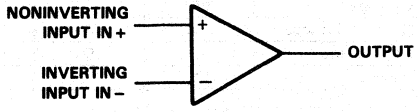
description

The uA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

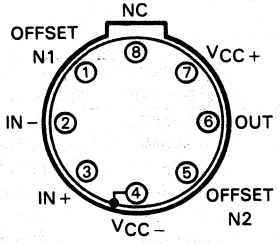
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The uA741M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA741C is characterized for operation from 0°C to 70°C.

symbol

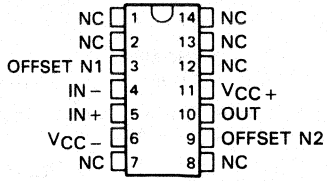


uA741M . . . L PACKAGE
(TOP VIEW)

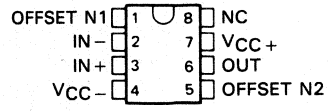


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

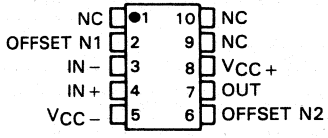
uA741M . . . J PACKAGE
(TOP VIEW)



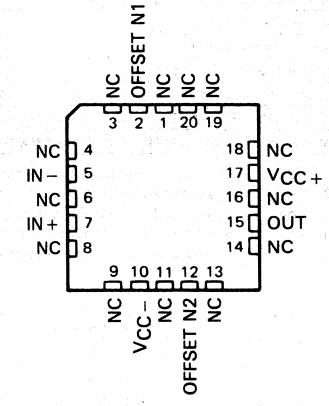
uA741M . . . JG PACKAGE
uA741C . . . D, JG, OR P PACKAGE
(TOP VIEW)



uA741M . . . U FLAT PACKAGE
(TOP VIEW)

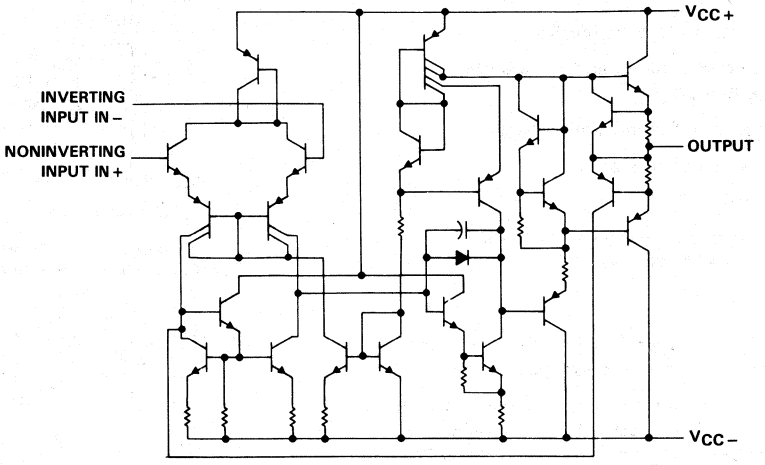


uA741M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA741M	uA741C	UNIT
Supply voltage V_{CC+} (see Note 1)		22	18	V
Supply voltage V_{CC-} (see Note 1)		−22	−18	V
Differential input voltage (see Note 2)		±30	±30	V
Input voltage any input (see Notes 1 and 3)		±15	±15	V
Voltage between either offset null terminal (N1/N2) and V_{CC-}		±0.5	±0.5	V
Duration of output short-circuit (see Note 4)		unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	L package	300		°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V whichever is less.
4. The output may be shorted to ground or either power supply. For the uA741M only, the unlimited duration of the short-circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATING ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	275 mW
J (uA741M)	500 mW	11.0 mW/°C	105°C	500 mW	275 mW
JG (uA741M)	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
JG (all others)	500 mW	N/A	N/A	500 mW	N/A
L	500 mW	6.7 mW/°C	75°C	500 mW	167 mW
P	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

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electrical characteristics at specified free-air temperature, V_{CC+} = 15 V, V_{CC-} = −15 V

PARAMETER		TEST CONDITIONS†		uA741M			uA741C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0	25°C		1	5		1	6	mV
			Full range			6			7.5	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	V_O = 0	25°C		±15			±15		mV
I_{IO}	Input offset current	V_O = 0	25°C		20	200		20	200	nA
			Full range			500			300	
I_{IB}	Input bias current	V_O = 0	25°C		80	500		80	500	nA
			Full range			1500			800	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	50	200		20	200		V/mV
		V_O = ±10 V	Full range	25			15			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	V_O = 0, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	μV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	No load, V_O = 0	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	No load, V_O = 0	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for uA741M is −55°C to 125°C and for uA741C is 0°C to 70°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		uA741M			uA741C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.3			0.3		μs
	Overshoot factor				5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.5			0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

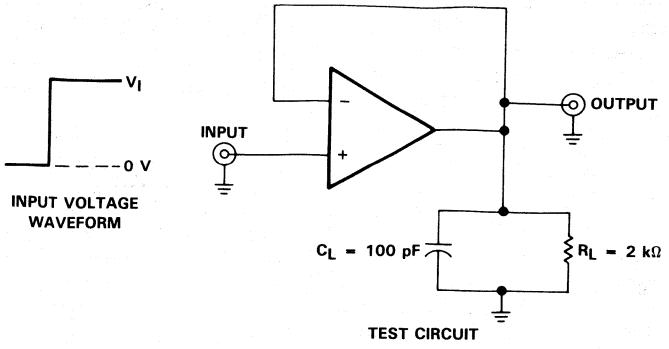

FIGURE 1. RISE TIME, OVERSHOOT, AND SLEW RATE

TYPICAL APPLICATION DATA

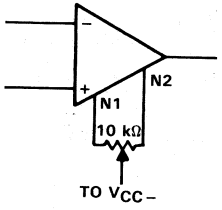

FIGURE 2. INPUT OFFSET VOLTAGE NULL CIRCUIT

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D1312, SEPTEMBER 1973—REVISED MARCH 1988

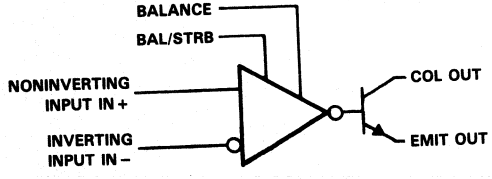
- **Fast Response Times**
- **Strobe Capability**
- **Designed to be Interchangeable with National Semiconductor LM111, LM211, and LM311**
- **Maximum Input Bias Current . . . 300 nA**
- **Maximum Input Offset Current . . . 70 nA**
- **Can Operate from Single 5-V Supply**

description

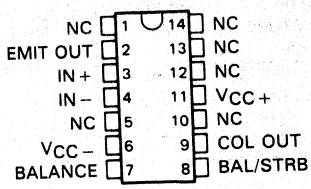
The LM111, LM211, and LM311 are single high-speed voltage comparators. These devices are designed to operate from a wide range of power supply voltage, including ±15-V supplies for operational amplifiers and 5-V supplies for logic systems. The output levels are compatible with most TTL and MOS circuits. These comparators are capable of driving lamps or relays and switching voltages up to 50 V at 50 mA. All inputs and outputs can be isolated from system ground. The outputs can drive loads referenced to ground, V_{CC+} or V_{CC-}. Offset balancing and strobe capability are available and the outputs can be wire-OR connected. If the strobe is low, the output will be in the off state regardless of the differential input.

The LM111 is characterized for operation over the full military range of −55°C to 125°C. The LM211 is characterized for operation from −25°C to 85°C, and the LM311 is characterized for operation from 0°C to 70°C.

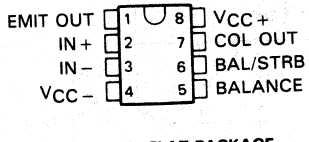
functional block diagram



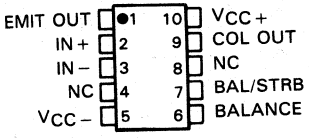
LM111 . . . J PACKAGE
(TOP VIEW)



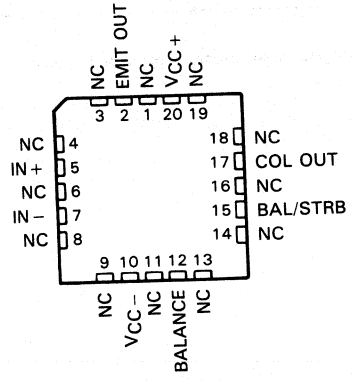
LM111 . . . JG PACKAGE
LM211, LM311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LM111 . . . U FLAT PACKAGE
(TOP VIEW)



LM111 . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)



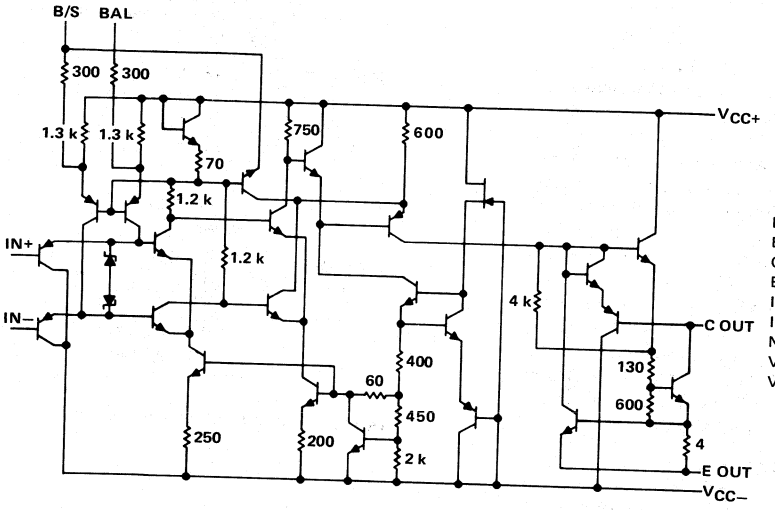
NC—No internal connection

AVAILABLE OPTIONS

OPERATING TEMPERATURE RANGE	V_{IO} MAX AT T_A = 25°C	PACKAGE					
		D SMALL OUTLINE	FK CERAMIC CHIP CARRIER	J CERAMIC DIP	JG CERAMIC DIP	P PLASTIC DIP	U FLATPACK
−55°C to 125°C	3 mV		LM111FK	LM111J			LM111U
−40°C to 85°C	3 mV	LM211D			LM211JG	LM211P	
0°C to 70°C	7.5 mV	LM311D			LM311JG	LM311P	

The D package is available in tape and reel. Add an R suffix when ordering, e.g., LM311DR.

schematic



BAL	Balance
B/S	Balance/Strobe
C OUT	Collector Output
E OUT	Emitter Output
IN+	Noninverting Input
IN−	Inverting Input
NC	No Internal Connection
V_{CC+}	Positive Supply Voltage
V_{CC-}	Negative Supply Voltage

Resistor values shown are nominal and in ohms.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	LM111	LM211	LM311	UNIT
Supply voltage, V_{CC+} (see Note 1)	18	18	18	V
Supply voltage, V_{CC-} (see Note 1)	−18	−18	−18	V
Differential input voltage (see Note 2)	±30	±30	±30	V
Input voltage (either input, see Notes 1 and 3)	±15	±15	±15	V
Voltage from emitter output to V_{CC-}	30	30	30	V
Voltage from collector output to V_{CC-}	50	50	40	V
Duration of output short-circuit (see Note 4)	10	10	10	s
Continuous total dissipation	See Dissipation Rating Table			
Operating free-air temperature range	−55 to 125	−25 to 85	0 to 70	°C
Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds: FK Package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or U package	300	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D or P package		260	260	°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	—
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J (LM111)	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	8.2 mW/°C	89°C	500 mW	500 mW	—
JG (LM111)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	—
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	—
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or ±15 volts, whichever is less.
4. The output may be shorted to ground or either power supply.

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM111, LM211			LM311			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	See Note 5		25°C		0.7	3		2	7.5	mV
				Full range			4			10	
I_{IO}	Input offset current	See Note 5		25°C		4	10		6	50	nA
				Full range			20			70	
I_{IB}	Input bias current	V_O = 1 V to 14 V		25°C		75	100		100	250	nA
				Full range			150			300	
$I_{IL(S)}$	Low-level strobe current (see Note 6)	$V_{(strobe)}$ = 0.3 V, $V_{ID} \le -10$ mV		25°C		−3			−3		mA
V_{ICR}	Common-mode input voltage range			Full range	13 to −14.5	13.8 to −14.7		13 to −14.5	13.8 to −14.7		V
A_{VD}	Large-signal differential voltage amplification	V_O = 5 V to 35 V, R_L = 1 kΩ		25°C	40	200		40	200		V/mV
I_{OH}	High-level (collector) output current	I_{strobe} = −3 mA, V_{ID} = 5 mV,	V_{OH} = 35 V	25°C		0.2	10				nA
				Full range			0.5				μA
		V_{ID} = 5 mV,	V_{OH} = 35 V	25°C					0.2	50	nA
V_{OL}	Low-level (collector-to-emitter) output voltage	I_{OL} = 50 mA	V_{ID} = −5 mV	25°C		0.75	1.5				V
			V_{ID} = −10 mV	25°C					0.75	1.5	
		V_{CC+} = 4.5 V, V_{CC-} = 0, I_{OL} = 8 mA	V_{ID} = −6 mV	Full range		0.23	0.4				
			V_{ID} = −10 mV	Full range					0.23	0.4	
I_{CC+}	Supply current from V_{CC+}, output low	V_{ID} = −10 mV,	No load	25°C		5.1	6		5.1	7.5	mA
I_{CC-}	Supply current from V_{CC-}, output high	V_{ID} = 10 mV,	No load	25°C		−4.1	−5		−4.1	−5	mA

†Unless otherwise noted, all characteristics are measured with the balance and balance/strobe terminals open and the emitter output grounded. Full range for LM111 is −55°C to 125°C, for LM211 is −25°C to 85°C, and for LM311 is 0°C to 70°C.

‡All typical values are at T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the collector output up to 14 V or down to 1 V with a pull-up resistor of 7.5 kΩ to V_{CC+}. Thus these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

6. The strobe should not be shorted to ground; it should be current driven at −3 to −5 mA, e.g., see Figures 13 and 27.

switching characteristics, V_{CC+} = 15 V, V_{CC-} = −15 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time, low-to-high-level output	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 7		115		ns
Response time, high-to-low-level output			165		ns

NOTE 7: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

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TYPICAL CHARACTERISTICS

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

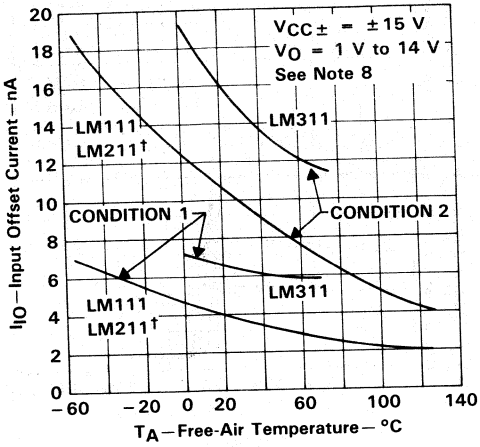


FIGURE 1

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

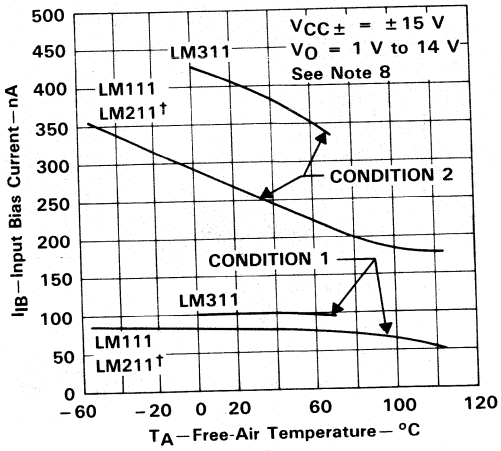


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS

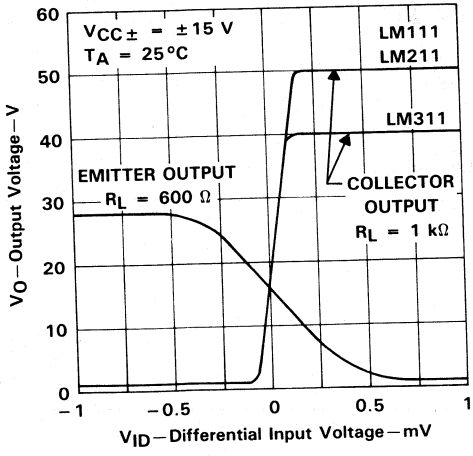
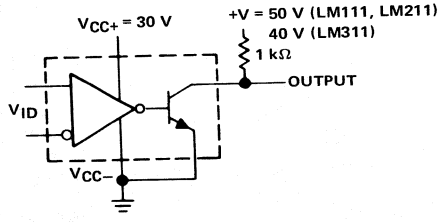
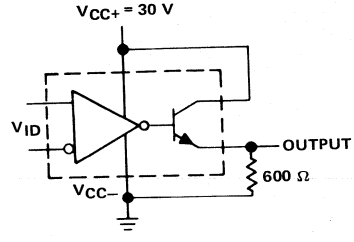


FIGURE 3



COLLECTOR OUTPUT TRANSFER CHARACTERISTIC
TEST CIRCUIT FOR FIGURE 3



EMITTER OUTPUT TRANSFER CHARACTERISTIC
TEST CIRCUIT FOR FIGURE 3

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
NOTE 8: Condition 1 is with the balance and balance/strobe terminals open. Condition 2 is with the balance and balance/strobe terminals connected to V_{CC+}.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

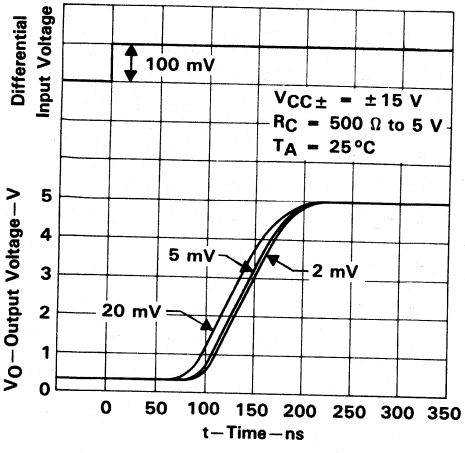


FIGURE 4

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

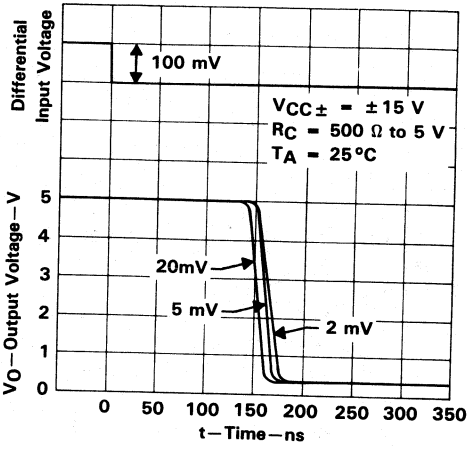
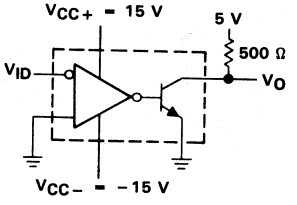


FIGURE 5



TEST CIRCUIT FOR FIGURES 4 AND 5

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

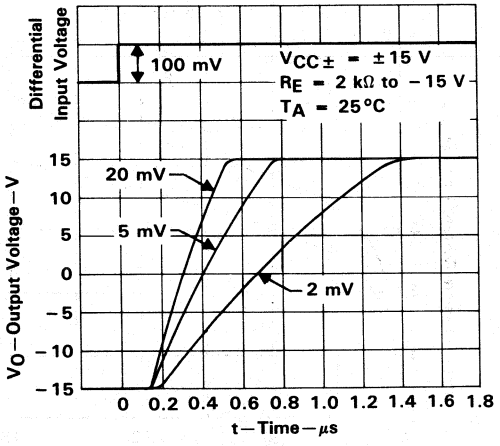


FIGURE 6

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

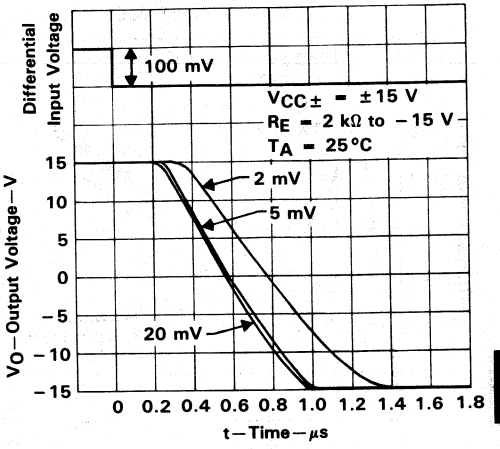
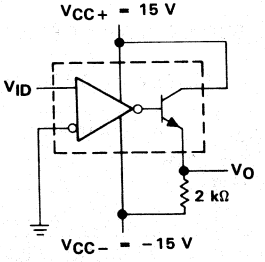


FIGURE 7



TEST CIRCUIT FOR FIGURES 6 AND 7

TYPICAL CHARACTERISTICS

OUTPUT CURRENT and DISSIPATION
vs
OUPUT VOLTAGE

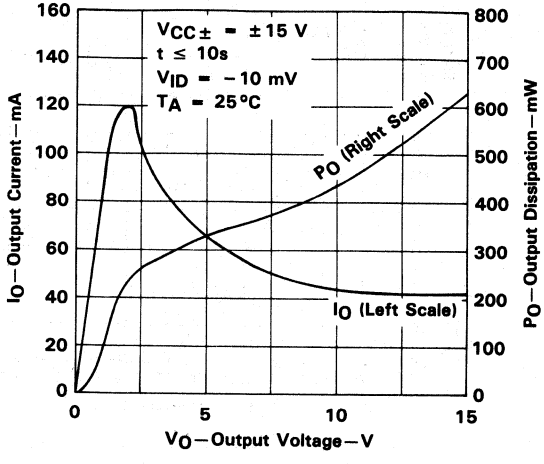


FIGURE 8

SUPPLY CURRENT FROM V_{CC+}
vs
SUPPLY VOLTAGE V_{CC+}

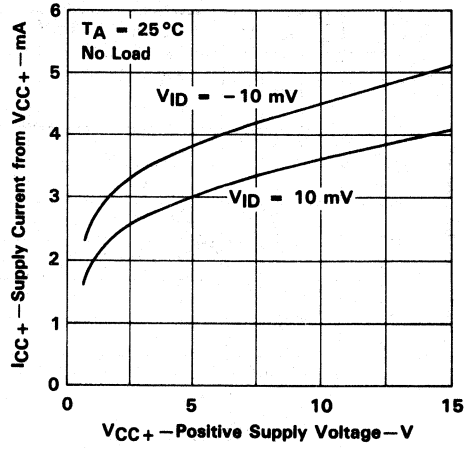


FIGURE 9

SUPPLY CURRENT FROM V_{CC-}
vs
SUPPLY VOLTAGE V_{CC-}

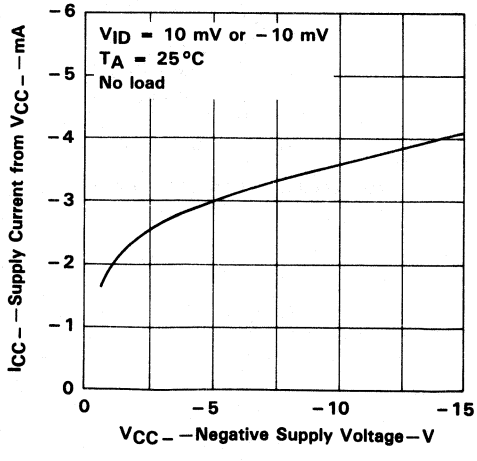


FIGURE 10

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

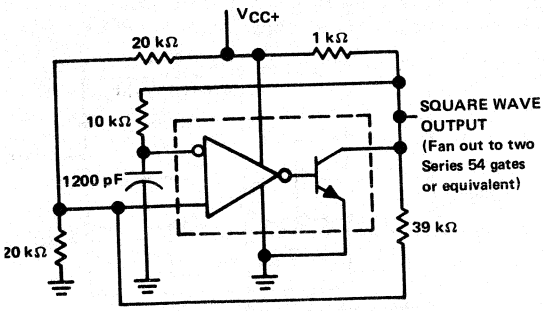


FIGURE 11. 100 kHz
FREE-RUNNING MULTIVIBRATOR

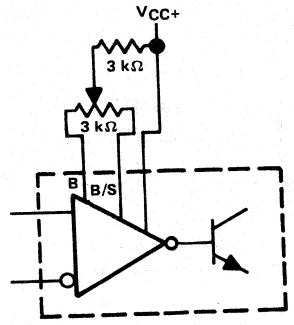


FIGURE 12. OFFSET BALANCING

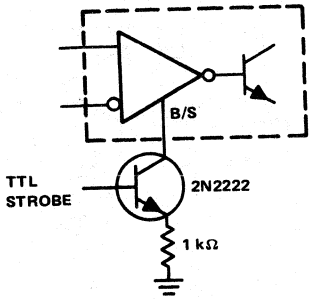


FIGURE 13. STROBING

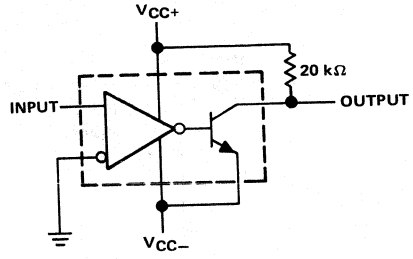
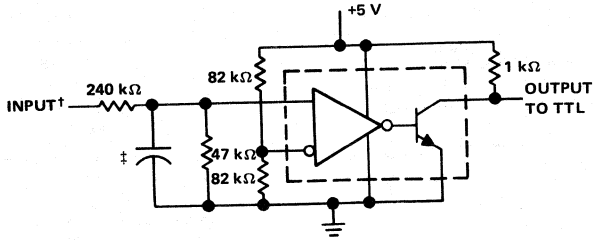


FIGURE 14. ZERO-CROSSING DETECTOR



†Resistor values shown are for a 0-to-30-V logic swing and a 15-V threshold.
‡May be added to control speed and reduce susceptibility to noise spikes.

FIGURE 15. TTL INTERFACE WITH HIGH-LEVEL LOGIC

TYPICAL APPLICATION DATA

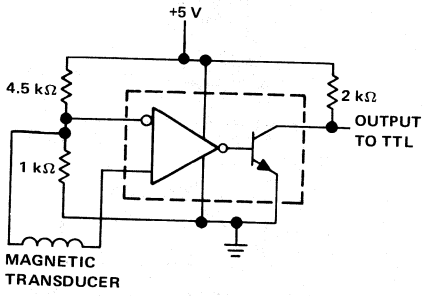


FIGURE 16. DETECTOR FOR MAGNETIC TRANSDUCER

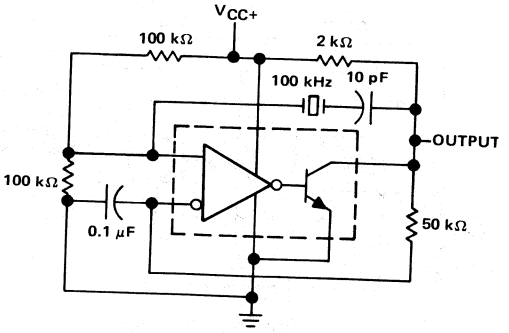


FIGURE 17. 100 kHz CRYSTAL OSCILLATOR

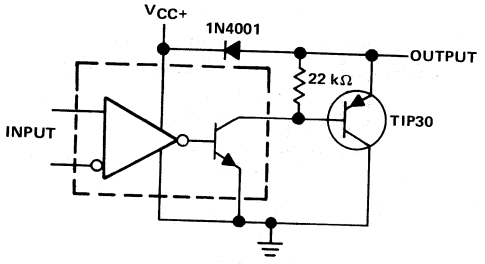
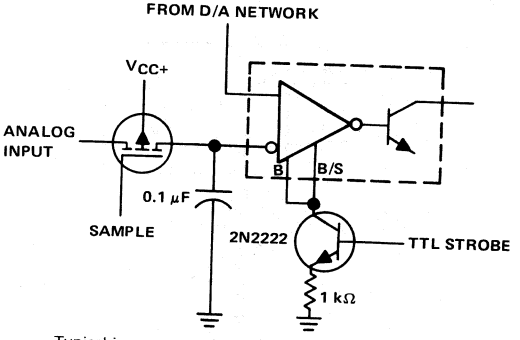


FIGURE 18. COMPARATOR AND SOLENOID DRIVER



Typical input current is 50 pA with inputs strobed off.

FIGURE 19. STROBING BOTH INPUT AND OUTPUT STAGES SIMULTANEOUSLY

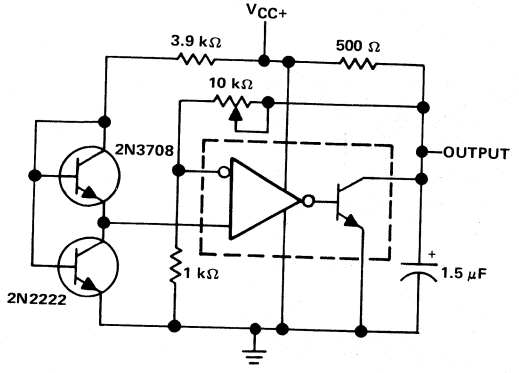


FIGURE 20. LOW-VOLTAGE ADJUSTABLE REFERENCE SUPPLY

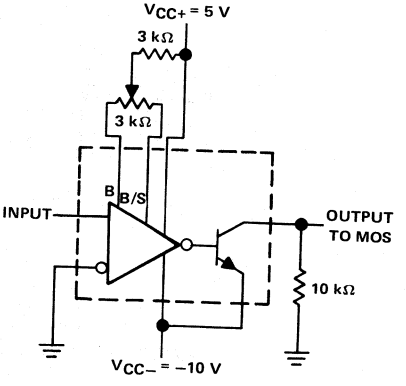


FIGURE 21. ZERO-CROSSING DETECTOR DRIVING MOS LOGIC

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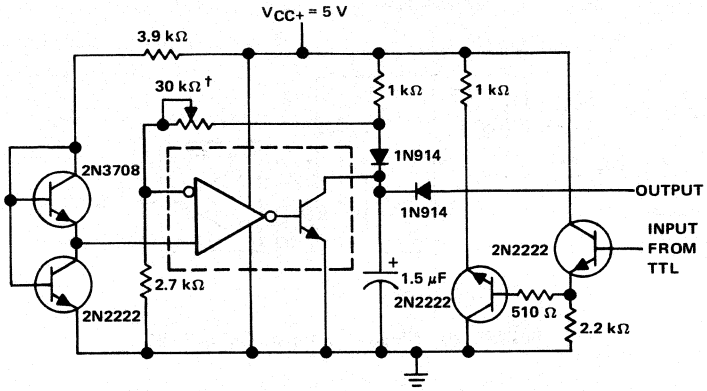
TYPICAL APPLICATION DATA



†Adjust to set clamp level.

FIGURE 22. PRECISION SQUARER

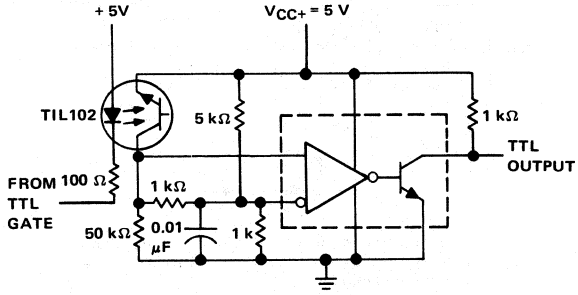


FIGURE 23. DIGITAL TRANSMISSION ISOLATOR

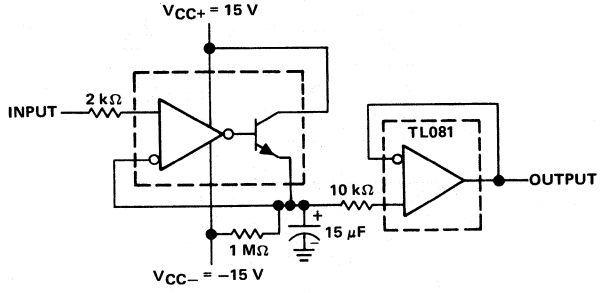


FIGURE 24. POSITIVE-PEAK DETECTOR

TYPICAL APPLICATION DATA

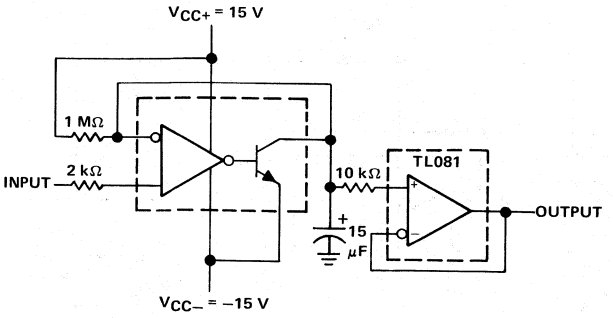
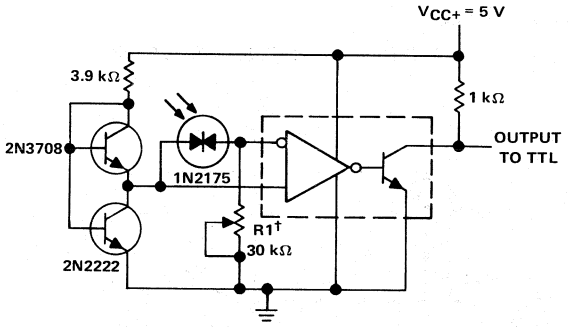
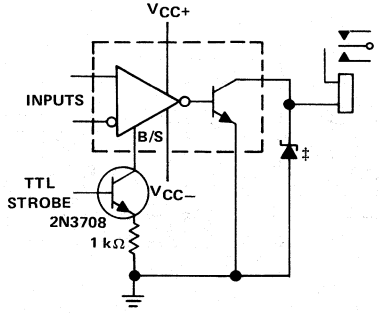


FIGURE 25. NEGATIVE-PEAK DETECTOR



†R1 sets the comparison level. At comparison, the photodiode has less than 5 mV across it decreasing dark current by an order of magnitude.

FIGURE 26. PRECISION PHOTODIODE COMPARATOR



‡Transient voltage and inductive kickback protection

FIGURE 27. RELAY DRIVER WITH STROBE

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

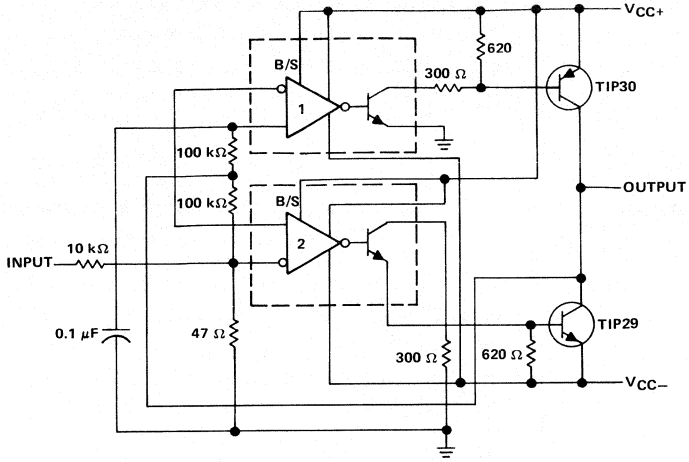


FIGURE 28. SWITCHING POWER AMPLIFIER

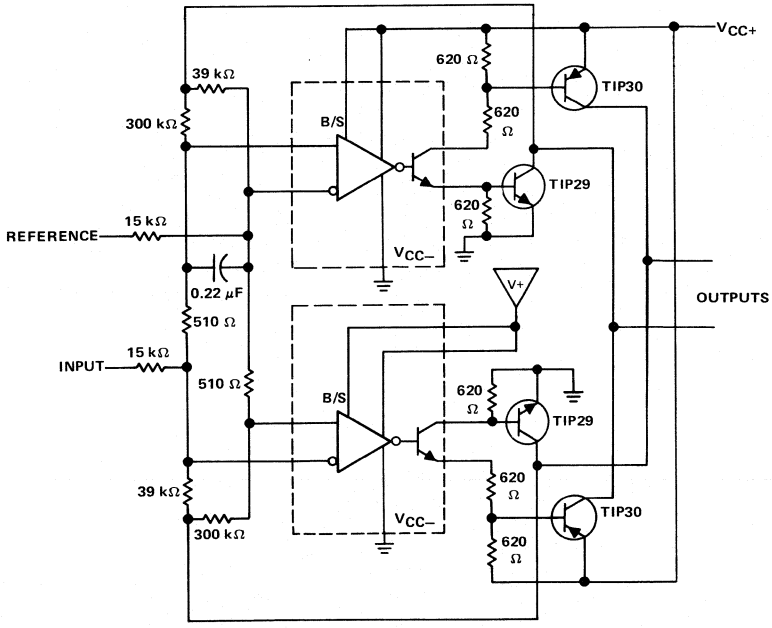


FIGURE 29. SWITCHING POWER AMPLIFIERS

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM139)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

description

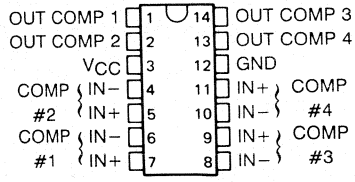
These devices consist of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 3 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

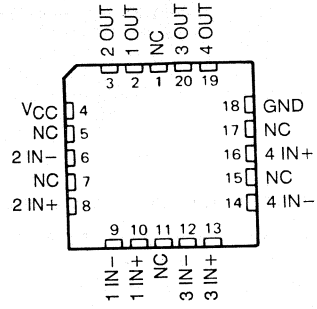
T_A	V_{IO} MAX at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	LM339D	—	LM339J	LM339N
	2 mV	LM339AD	—	LM339AJ	LM339AN
−25°C to 85°C	5 mV	LM239D	—	LM239J	LM239N
	2 mV	LM239AD	—	LM239AJ	LM239AN
−40°C to 125°C	7 mV	LM2901ID	—	LM2901IJ	LM2091IN
−55°C to 125°C	5 mV	—	LM139FK	LM139J	—
	2 mV	—	LM139AFK	LM139AJ	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., LM339DR)

LM139, LM139A . . . J PACKAGE
ALL OTHERS . . . D, J, OR N PACKAGE
(TOP VIEW)

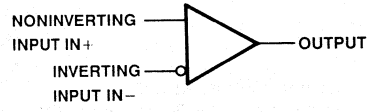


LM139, LM139A
FK CHIP CARRIER PACKAGE
(TOP VIEW)

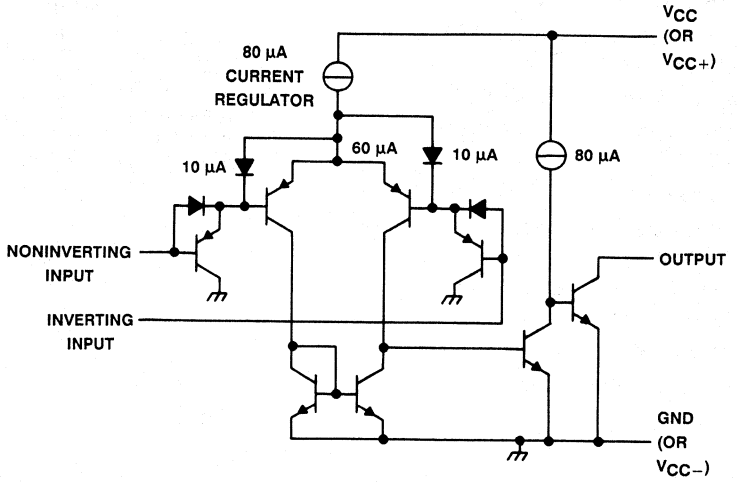


NC—No internal connection

symbol (each comparator)



schematic (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 36 V
Differential input voltage (see Note 3) . . . . . ±36 V
Input voltage range (either input) . . . . . −0.3 V to 36 V
Output voltage . . . . . 36 V
Output current . . . . . 20 mA
Duration of output short-circuit to ground (see Note 4) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: LM139 . . . . . −55°C to 125°C
LM239, LM239A . . . . . −25°C to 85°C
LM339, LM339A . . . . . 0°C to 70°C
LM2901 . . . . . −40°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 2. All voltage values, except differential voltages, are with respect to the network ground terminal.
3. Differential voltages are at the noninverting input terminal with respect to the inverting input.
4. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	900 mW	7.6 mW/°C	31°C	608 mW	494 mW	–
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (LM139, LM139A)	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
J (All others)	900 mW	8.2 mW/°C	40°C	656 mW	533 mW	–
N	900 mW	9.2 mW/°C	52°C	736 mW	598 mW	–

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM139			LM139A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V		25°C		2	5		1	2	mV
				−55°C to 125°C			9			4	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		3	25	nA
				−55°C to 125°C			100			100	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−100		−25	−100	nA
				−55°C to 125°C			−300			−300	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				−55°C to 125°C	0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm}$ = ±7.5 V, V_O = −5 V to 5 V		25°C		200		50	200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	−55°C to 125°C			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				−55°C to 125°C			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load		25°C		0.8	2		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM239, LM339			LM239A, LM339A			LM2901			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V		25°C		2	5		1	2		2	7	mV
				Full range			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50		5	50		5	50	nA
				Full range			150			150			200	
I_{IB}	Input bias current			25°C		−25	−250		−25	−250		−25	−250	nA
		V_O = 1.4 V		Full range			−400			−400			−500	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to V_{CC}		25°C	50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1	50		0.1	50		0.1	50	nA
			V_{OH} = 30 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	500	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V, No load		25°C		0.8	2		0.8	2		0.8	2	mA
		V_{CC} = 30 V, V_O = 15 V, No load										1	2.5	

† Full range (MIN to MAX) for LM239 and LM239A is −25°C to 85°C, for LM339 and LM339A is 0°C to 70°C, and for LM2901 is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 5	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

‡ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

D2232, JUNE 1976—REVISED NOVEMBER 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . . 3 nA Typ (LM139)
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

description

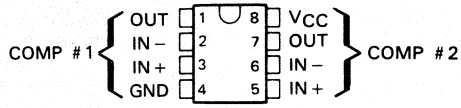
These devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible as long as the difference between the two supplies is 2 V to 36 V and pin 8 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

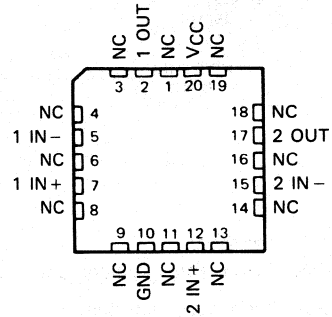
SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX AT T_A = 25°C
DEVICE	PACKAGE SUFFIX		
LM193	L, FK, JG	−55°C to 125°C	5 mV
LM293	D, JG, P	−25°C to 85°C	5 mV
LM293A	D, JG, P	−25°C to 85°C	2 mV
LM393	D, JG, P	0°C to 70°C	5 mV
LM393A	D, JG, P	0°C to 70°C	2 mV
LM2903	D, JG, P	−40°C to 125°C	7 mV

The D package is available in tape and reel. Add an R suffix when ordering. (e.g., LM393DR)

LM193 . . . JG PACKAGE
ALL OTHERS . . . D, JG, OR P PACKAGE
(TOP VIEW)

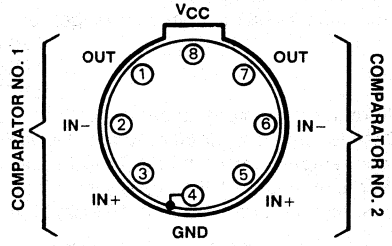


LM193 . . . FK PACKAGE
(TOP VIEW)



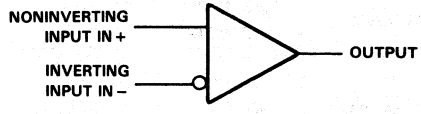
NC—No internal connection

LM193 . . . L
PLUG-IN PACKAGE
(TOP VIEW)

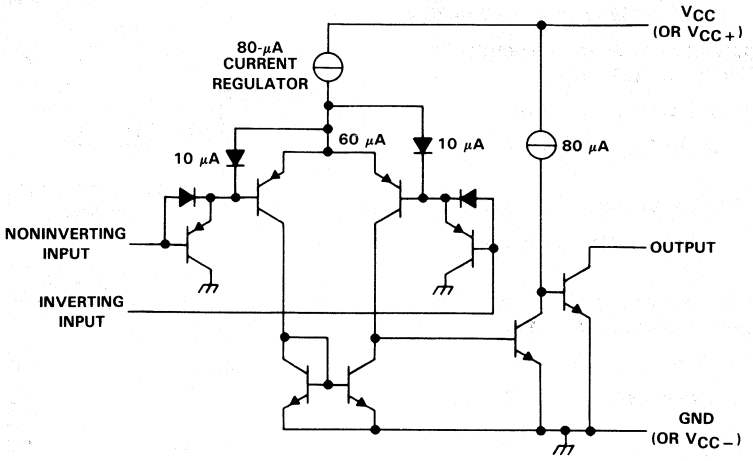


PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE.

symbol (each comparator)



schematic (each comparator)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Output voltage	36 V
Output current	20 mA
Duration of output short-circuit to ground (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range: LM193	−55°C to 125°C
LM293, LM293A	−25°C to 85°C
LM393, LM393A	0°C to 70°C
LM2903	−40°C to 125°C
Storage temperature range	−65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	25°C	464 mW	377 mW	–
FK	900 mW	11.0 mW/°C	68°C	880 mW	715 mW	275 mW
JG (LM193)	900 mW	8.4 mW/°C	43°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	–
L	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	165 mW
P	900 mW	8.0 mW/°C	37°C	640 mW	520 mW	–

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			LM193			LM293, LM393			LM293A, LM393A			LM2903			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, $V_{IC} = V_{ICR}$, V_O = 1.4 V		25°C		2	5		2	5		1	2		2	7	mV
				Full range			9			9			4			15	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50		5	50		5	50	nA
				Full range			100			150			150			200	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		25	100		25	250		25	250		25	250	nA
				Full range			300			400			400			500	
V_{ICR}	Common-mode input voltage range‡			25°C	0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			0 to $V_{CC}-1.5$			V
				Full range	0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			0 to $V_{CC}-2$			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15\ k\Omega$ to VCC		25°C	50	200		50	200		50	200		25	100		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V	V_{ID} = 1 V	25°C		0.1			0.1	50		0.1	50		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	Full range			1			1			1			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V,	25°C		150	400		150	400		150	400		150	400	mV
				Full range			700			700			700			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = −1 V	25°C	6			6			6			6			mA
I_{CC}	Supply current	$R_L = \infty$	V_{CC} = 5 V	25°C		0.8	1		0.8	1		0.8	1		0.8	1	mA
			V_{CC} = 30 V	Full range			2.5			2.5			2.5			2.5	

† Full range (MIN to MAX) for LM193 is −55°C to 125°C, for LM293 and LM293A is 25°C to 85°C, for the LM393 and LM393A is 0°C to 70°C, and for LM2903 is −40°C to 125°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} −1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,§ See Note 4	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

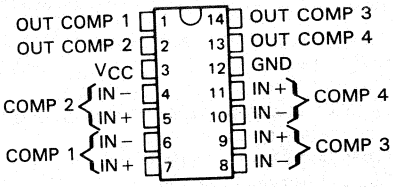
NOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

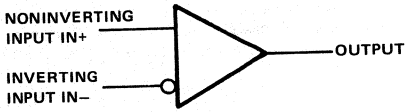
D2402, OCTOBER 1977 – REVISED APRIL 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage . . . 2 to 28 Volts
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current . . .3 nA Typ
- Low Input Offset Voltage . . . 3 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±28 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

D, J, OR N PACKAGE
(TOP VIEW)



symbol (each comparator)



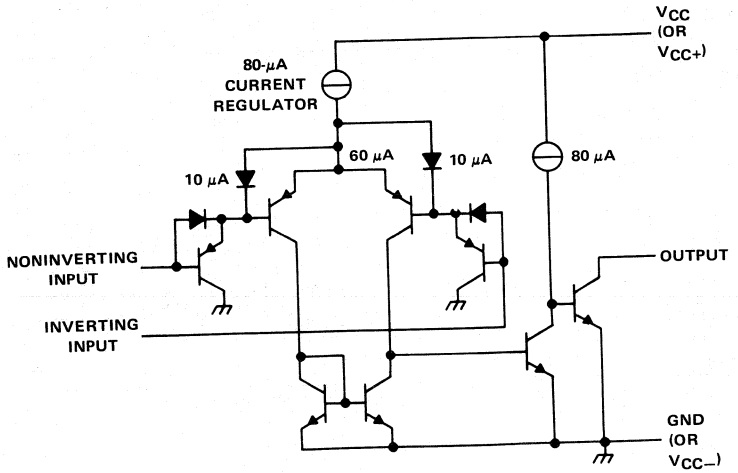
description

This device consists of four independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 28 V and pin 3 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The outputs can be connected to other open-collector outputs to achieve wired-AND relationships.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_{IO} MAX at 25°C
DEVICE	PACKAGE SUFFIX		
LM3302	D, J, N	−40°C to 85°C	20 mV

The D packages are available taped and reeled. Add the suffix R to the device type, when ordering. (i.e., LM3302DR)



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) 28
Differential input voltage (see Note 2) 28
Input voltage range (either input) . . . . . ±28
Output voltage . . . . . −0.3 V to 28
Output current 28
Duration of output short-circuit to ground (see Note 3) . . . . . 20 m
Continuous total dissipation . . . . . unlimite
Operating free-air temperature range . . . . . See Dissipation Rating Tab
Storage temperature range . . . . . −40°C to 85°
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . −65°C to 150°
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 300°
. . . . . 260°

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 28 V, $V_{IC} = V_{ICR}$ min, V_O = 1.4 V		25°C		3	20	mV
				−40°C to 85°C			40	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	100	nA
				−40°C to 85°C			300	
I_{IB}	Input bias current			25°C		−25	−500	nA
				−40°C to 85°C			−1000	
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{CC}−1.5			V
				−40°C to 85°C	0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = 15 kΩ to V_{CC}		25°C	2	30		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V,	V_{OH} = 5 V	25°C		0.1		nA
				−40°C to 85°C			1	µA
V_{OL}	Low-level output voltage	V_{ID} = 1 V,	I_{OL} = 4 mA	25°C		150	500	mV
				40°C to 85°C			700	
I_{OL}	Low-level output current	V_{ID} = 1 V,	V_{OL} = 1.5 V	25°C	6	16		mA
I_{CC}	Supply current (four comparators)	V_O = 2.5 V,	No load	25°C		0.8	2	mA

† All characteristics are measured with zero common-mode input voltage unless otherwise specified.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

¡witching characteristics, V_{CC} = 5 V, T_A = 25°C

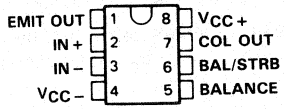
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ to 5 V,	100-mV input step with 5-mV overdrive		1.3		µs
	C_L = 15 pF‡, See Note 4	TTL-level input step		0.3		

C_L includes probe and jig capacitance.
IOTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

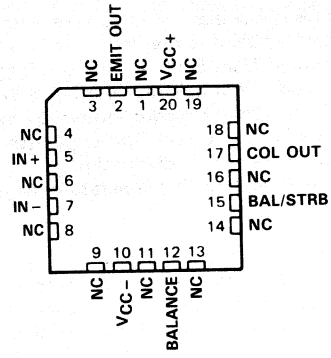
D3019, JUNE 1987—REVISED MAY 1988

- Low Power Drain — 900 μW Typical with 5-V Supply
- Operates from ±15 V or from a Single Supply as Low as 3 V
- Output Drive Capability of 25 mA
- Emitter Output Can Swing Below Negative Supply
- Response Time — 1.2 μs Typ
- Low Input Currents:
  Offset Current . . . 2 nA Typ
  Bias Current . . . 15 nA Typ
- Wide Common-Mode Input Range:
  −14.5 V to 13.5 V with ±15-V Supply
- Same Pinout as LM111, LM211, LM311
- Designed to be Interchangeable with National Semiconductor LP311

LP111 . . . JG DUAL-IN-LINE PACKAGE
LP211, LP311 . . . D, JG, OR P PACKAGE
(TOP VIEW)



LP111 . . . FK CHIP CARRIER PACKAGE
(TOP VIEW)

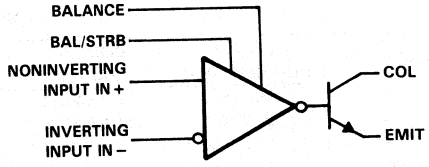


NC—No internal connection

description

The LP111, LP211, and LP311 are a low-power versions of the industry-standard LM111, LM211, and LM311. They take advantage of stable, high-value, ion-implanted resistors to perform the same function as the LM311 series, with a 30:1 reduction in power consumption but only a 6:1 slowdown in response time. Thus, they are well-suited for battery-powered applications and all other applications where fast response times are not needed. They operate over a wide range of supply voltages, from ±18 V down to a single 3-V supply with less than 300 μA current drain, but are still capable

functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	7.5 mV	LP311D	—	LP311JG	LP311P
−25°C to 85°C	7.5 mV	LP211D	—	LP211JG	LP211P
−55°C to 125°C	7.5 mV	—	LP111FK	LP111JG	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering, (e.g., LP311DR)

description (continued)

of driving a 25-mA load. The LP111, LP211, and LP311 are quite easy to apply free of oscillation if ordina precautions are taken to minimize stray coupling from the output to either input or to the trim pins.

The LP111 is characterized for operation over the full military temperature range of −55°C to 125°C The LP211 is characterized for operation from −25°C to 85°C, and the LP311 is characterized for operatic from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −18 V
Differential input voltage (see Note 2) . . . . . ±30 V
Input voltage (either input, see Notes 1 and 3) . . . . . ±15 V
Voltage from emitter output to V_{CC-} . . . . . 30 V
Voltage from collector output to V_{CC-} . . . . . 40 V
Voltage from collector output to emitter output . . . . . 40 V
Duration of output short-circuit (see Note 4) . . . . . 40 V
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: LP111 . . . . . −55°C to 125°C
LP211 . . . . . −25°C to 85°C
LP311 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential input voltages are at the noninverting input terminal with respect to the inverting terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage of ±15 V, whichever is less.
4. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	—
FK	1375 mW	11.0 mW/°C	25°C	880 mW	715 mW	275 mW
JG (LP111)	1050 mW	8.4 mW/°C	25°C	672 mW	546 mW	210 mW
JG (LP_11)	825 mW	6.6 mW/°C	25°C	528 mW	429 mW	—
P	500 mW	8.0 mW/°C	88°C	500 mW	500 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNITS
Input voltage ($\lvert V_{CC\pm} \rvert \leq 15$ V)	V_{CC-} +0.5		V_{CC+} −1.5	V
Supply voltage, $V_{CC+} - V_{CC-}$	3.5		30	V

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

lectrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
$/_{ID}$	Input offset voltage	RS < 100 kΩ, See Note 5	25°C			2	7.5	mV
			Full Range				10	
IO	Input offset current	See Note 5	25°C			2	25	nA
			Full Range				35	
IB	Input bias current		25°C			15	100	nA
			Full Range				150	
V_{OL}	Low-level output voltage	V_{ID} > 10 mV, I_{OL} = 25 mA, See Note 6	25°C			0.4	1.5	V
		V_{CC} = 4.5 V, V_{CC-} = 0, V_{ID} < −10 mV, I_{OL} = 1.6 mA, See Note 6	Full Range	LP111		0.1	0.7	
				LP211 LP311		0.1	0.4	
	Low-level strobe current	$V_{(strobe)}$ = 0.3 V, V_{ID} < −10 mV, See Note 7	25°C			100	300	μA
$I_{O(off)}$	Output off-state current	V_{ID} > 10 mV, V_{CE} = 35 V	25°C			0.2	100	nA
A_{VD}	Large signal differential voltage amplification	R_L = 5 kΩ	25°C		40	100		V/mV
I_{CC+}	Supply current from V_{CC+}	V_{ID} = −50 mV, R_L = ∞	Full Range			150	300	μA
I_{CC-}	Supply current from V_{CC-}	V_{ID} = 50 mV, R_L = ∞	Full Range			−80	−180	μA

†All typical values are at $V_{CC\pm}$ = ±15 V, T_A = 25°C.

NOTES: 5. The offset voltages and offset currents given are the maximum values required to drive the output within 1 V of either supply with a 1-mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
6. Voltages are with respect to EMIT OUT and V_{CC-} tied together.
7. The strobe should not be shorted to ground; it should be current driven at 100 μA to 300 μA.

switching characteristics at $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

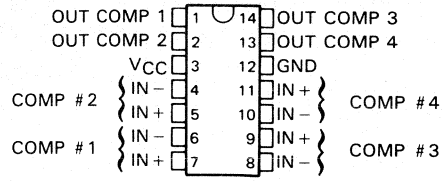
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	See Note 8		1.2		μs

NOTE 8: The response time is specified for a 100-mV input step with 5-mV overdrive.

D3044, OCTOBER 1987—REVISED MAY 1988

- **Ultralow Power Supply Current Drain . . . Typically 60 μA**
- **Low Input Biasing Current . . . 3 nA**
- **Low Input Offset Current . . . ±0.5 nA**
- **Low Input Offset Voltage . . . ±2 mV**
- **Common-Mode Input Voltage Includes Ground**
- **Output Voltage Compatible with MOS and CMOS Logic**
- **High Output Sink-Current Capability (30 mA at V_O = 2 V)**
- **Power Supply Input Reverse-Voltage Protected**
- **Single-Power-Supply Operation**
- **Pin-for-Pin Compatible with LM239, LM339, LM2901**

D, J, OR N PACKAGE
(TOP VIEW)



description

The LP239, LP339, and LP2901 are low-power quadruple differential comparators. Each device consists of four independent voltage comparators designed specifically to operate from a single power supply and typically to draw 60-μA drain current over a wide range of voltages. Operation from split power supplies is also possible and the ultralow power supply drain current is independent of the power supply voltage.

Applications include limit comparators, simple analog-to-digital converters, pulse generators, squarewave generators, time delay generators, voltage controlled oscillators, multivibrators, and high-voltage logic gates. The LP239, LP339, and LP2901 were specifically designed to interface with the CMOS logic family. The ultralow power supply current makes these products desirable in battery-powered applications.

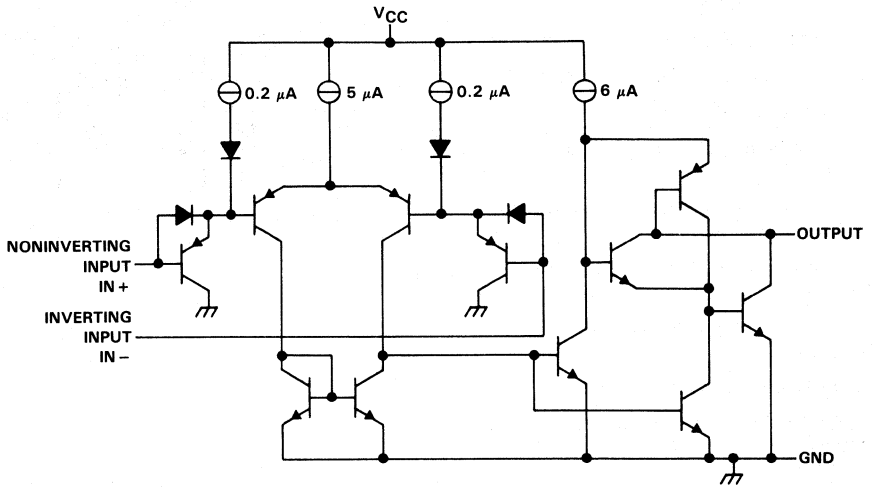
The LP239 is characterized for operation from −25°C to 85°C. The LP339 is characterized for operation from 0°C to 70°C. The LP2901 is characterized for operation from −40°C to 85°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE		
		SMALL-OUTLINE (D)	PLASTIC DIP (N)	CERAMIC DIP (J)
0°C to 70°C	±5 mV	LP339D	LP339N	LP339J
−25°C to 85°C	±5 mV	LP239D	LP239N	LP239J
−40°C to 85°C	±5 mV	LP2901D	LP2901N	LP2901J

D packages are available taped-and-reeled. Add "R" suffix to device type when ordering (e.g., LP339DR).

schematic diagram (each comparator)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	36 V
Differential input voltage, V_{ID} (see Note 2)	±36 V
Input voltage range (either input)	−0.3 V to 36 V
Input current, $V_I \leq -0.3$ V (see Note 3)	−50 mA
Duration of output short-circuit to ground (see Note 4)	unlimited
Continuous total dissipation (see Note 5)	See Dissipation Rating Table
Operating free-air temperature range: LP239	−25°C to 85°C
LP339	0°C to 70°C
LP2901	−40°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. This input current only exists when the voltage at any of the inputs is driven negative. The current flows through the collector-base junction of the input clamping device. In addition to the clamping device action, there is lateral n-p-n parasitic transistor action. This action is not destructive and normal output states are re-established when the input voltage returns to a value more positive than −0.3 V at T_A = 25°C.
4. Short circuits between outputs to V_{CC} can cause excessive heating and eventual destruction.
5. If the output transistors are allowed to saturate, the low bias dissipation and the on-off characteristics of the outputs keep the dissipation very small (usually less than 100 mW).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
J	1025 mW	8.2 mW/°C	656 mW	533 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

		LP2901			LP239			LP339			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		5		30	5		30	5		30	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0		3	0		3	0		3	V
	V_{CC} = 30 V	0		28	0		28	0		28	V
Input voltage, V_I	V_{CC} = 5 V	0		3	0		3	0		3	V
	V_{CC} = 30 V	0		28	0		28	0		28	V
Operating free-air temperature, T_A		−40		85	−25		85	0		70	°C

electrical characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, RS = 0,	V_O = 2 V, See Note 6	25°C		±2	±5	mV
				Full range			±9	
I_{IO}	Input offset current			25°C		±0.5	±5	nA
				Full range		±1	±15	
I_{IB}	Input bias current	See Note 7		25°C		−2.5	−25	nA
				Full range		−4	−40	
V_{ICR}	Common-mode input voltage range	Single supply		25°C	0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V,	R_L = 15 kΩ			500		V/mV
	Output sink current	V_{I-} = 1 V, V_{I+} = 0	V_O = 2 V (see Note 8)	25°C	20	30		mA
				Full range	15			
			V_O = 0.4 V	25°C	0.2	0.7		
	Output leakage current	V_{I+} = 1 V, V_{I-} = 0	V_O = 5 V	25°C		0.1		nA
			V_O = 30 V	Full range			1	μA
V_{ID}	Differential input voltage	V_I ≤ 0 (or V_{CC-} on split supplies)					36	V
I_{CC}	Supply current	R_L = ∞ all comparators				60	100	μA

NOTES: 6. V_{IO} is measured over the full common-mode input voltage range.
7. Because of the p-n-p input stage, the direction of the current is out of the device. This current is essentially constant (i.e., independent of the output state). Therefore, no loading change exists on the reference or input lines as long as the common-mode input voltage range is not exceeded.
8. The output sink current is a function of the output voltage. These devices have a bimodal output section that allows them to sink (via a Darlington connection) large currents at output voltages greater than 1.5 V, and smaller currents at output voltages less than 1.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L connected to 5 V through 5.1 kΩ

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Large-signal response time	TTL logic swing, V_{ref} = 1.4 V		1.3		μs
Response time			8		μs

TYPICAL APPLICATION DATA

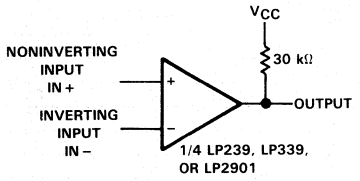


FIGURE 1. BASIC COMPARATOR

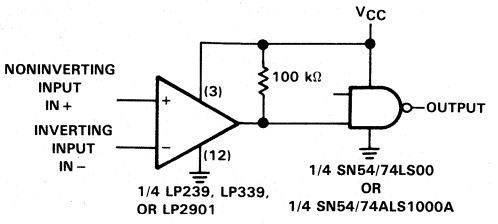


FIGURE 2. CMOS DRIVER

All pins of any unused comparators should be grounded. The bias network of the LP239, LP339, and LP2901 establishes a drain current that is independent of the magnitude of the power supply voltage over the range of 2 V to 30 V. It is usually necessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V_{CC} without damaging the device. Protection should be provided to prevent the input voltages from going negative by more than −0.3 V. The output section has two distinct modes of operation: a Darlington mode and a grounded-emitter mode. This unique drive circuit permits the device to sink 30 mA at V_O = 2 V in the Darlington mode and 700 μA at V_O = 0.4 V in the ground-emitter mode. Figure 3 is a simplified schematic diagram of the output section. The output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough (above 1 V), Q1 is not saturated and the output current is limited only by the product of the h_{FE} of Q1, the h_{FE} of Q2, and I1 and by the 60-Ω saturation resistance of Q2. The devices are capable of driving LEDs, relays, etc., in this mode while maintaining an ultralow power supply current of 60 μA typically.

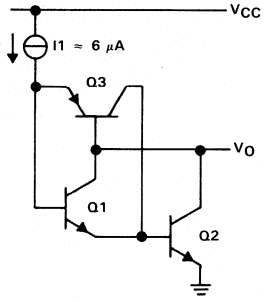


FIGURE 3. OUTPUT SECTION SCHEMATIC DIAGRAM

Without transistor Q3, if the output voltage were allowed to drop below 0.8 V, transistor Q1 would saturate and the output current would drop to zero. The circuit would be unable to pull low current loads down to ground or the negative supply, if used. Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the h_{FE} of Q2 (700 μA at V_O = 0.4 V). The output of the devices exhibit a bimodal characteristic with a smooth transition between modes.

In both cases, the output is an uncommitted collector. Therefore several outputs can be tied together to provide a dot logic function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range, and there is no restriction on this voltage based on the magnitude of the voltage that is applied to the V_{CC} terminal of the package.

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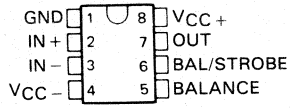
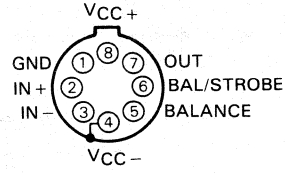
D3179, JANUARY 1989

- **Low Input Offset Voltage . . . 1.5 or 0.5 mV Max**
- **Maximum Input Bias Current . . . 50 or 25 nA**
- **Low Input Offset Current . . . 4 or 3 nA Max**
- **Output Response Time . . . 250 ns Max**
- **Voltage Gain . . . 200 V/mV Min**
- **Output Current . . . 50 mA Source or Sink**
- **Differential Input Voltage . . . ±30 V**
- **Can Operate from Single 5-V Supply**
- **Pin-Compatible with LM111 Series**
- **Designed to be Interchangeable with Linear Technology LT1011 and LT1011A**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)

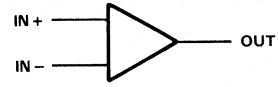


Pin 4 (L package) is in electrical contact with the case.

description

The LT1011 and LT1011A are general-purpose comparators that are pin-compatible with the LM111. The LT1011A offers significantly better input characteristics than the LM111: four times lower bias current, six times lower offset voltage, and five times higher voltage gain. Additionally, the supply current is considerably lower than that of the LM111 with no loss in speed. The offset voltage temperature coefficient of the LT1011A is 15 µV/°C. The LT1011 and LT1011A are fully specified for dc parameters and output response time when operating from a single 5-V supply.

symbol



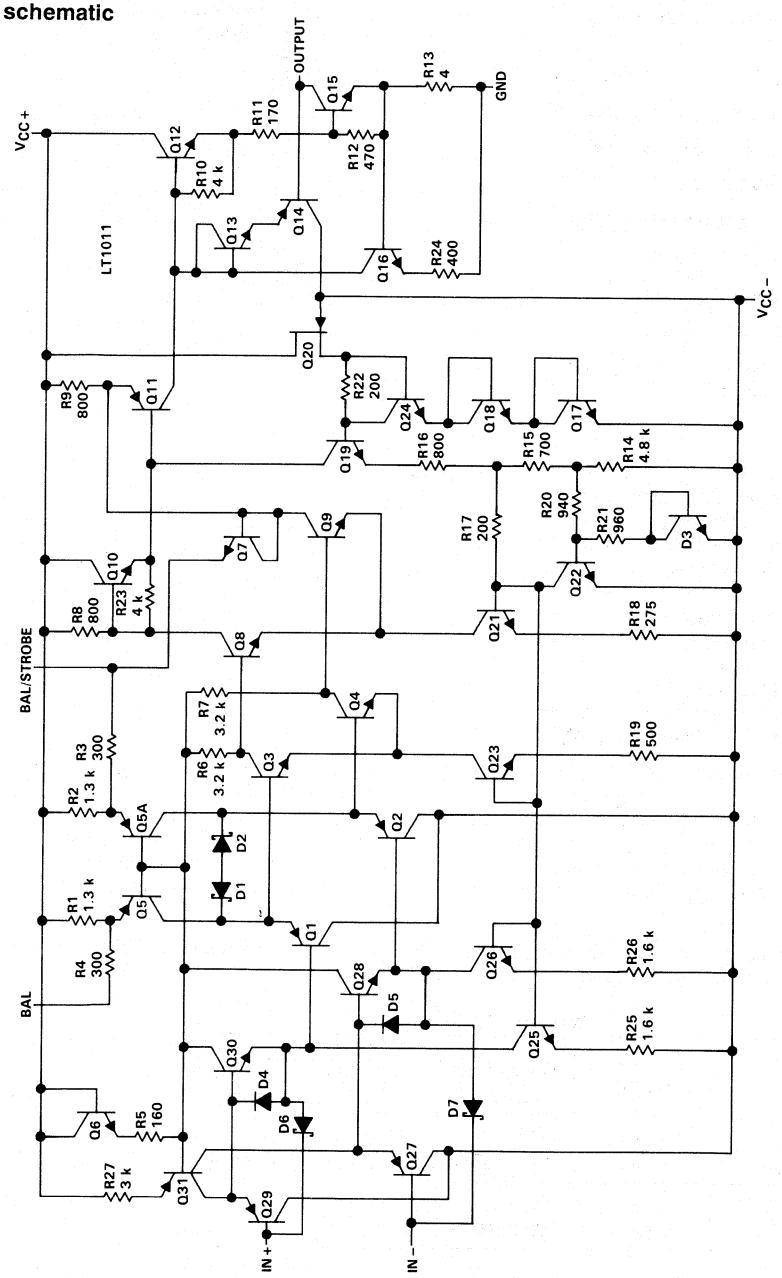
The LT1011 and LT1011A can be used in high-accuracy (≥ 12-bit) systems without trimming. The devices retain all the versatile features of the LM111 including single-supply operation (3 V to 36 V) or dual-supply operation (±1.5 V to ±18 V) and a floating transistor output with 50-mA source or sink capability. The devices can drive loads that are referenced to ground, the negative supply, or the positive supply, and are specified up to 50 V between V_{CC-} and the collector output. A differential input voltage up to the full supply voltage is allowed, even with ±18-V supplies, enabling the inputs to be clamped to the supplies with simple diode clamps.

M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. C-suffix devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	1.5 mV	LT1011CJG	LT1011CL	LT1011CP
	0.5 mV	LT1011ACJG	LT1011ACL	LT1011ACP
−55°C to 125°C	1.5 mV	LT1011MJG	LT1011ML	
	0.5 mV	LT1011AMJG	LT1011AML	

schematic



Resistor values shown are nominal and in ohms.

ıbsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+}	18 V
Supply voltage, V_{CC-}	−18 V
Voltage from output to V_{CC-}: M-suffix	50 V
C-suffix	40 V
Voltage from GND to V_{CC-}	30 V
Voltage from strobe to V_{CC+}	5 V
Differential input voltage (see Note 1)	±36 V
Input voltage (either input, see Note 2)	$V_{CC\pm}$
Duration of output short circuit (see Note 3)	10 s
Continuous power dissipation	See Dissipation Rating Table
Operating free-air temperature range: M-suffix	−55°C to 125°C
C-suffix	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package	260°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. Inputs may be clamped to supplies with diodes so that the maximum input voltage actually exceeds the supply voltage by one diode drop (refer to "input protection" in the applications section).
3. The output may be shorted to ground or to either power supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG (M-suffix)	1050 mW	8.4 mW/°C	672 mW	210 mW
JG (C-suffix)	825 mW	6.6 mW/°C	528 mW	N/A
L (M-suffix)	825 mW	6.6 mW/°C	528 mW	165 mW
L (C-suffix)	650 mW	5.2 mW/°C	416 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	N/A

recommended operating conditions

		M-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}				15			15	V
Supply voltage, V_{CC-}				−15			−15	V
Input voltage, V_I, (see Note 4)	$V_{CC\pm}$ = ±15 V	−14.5		13	−14.5		13	V
	V_{CC} = single 5-V	0.5		3	0.5		3	
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 4: See "Input Signal Range" under "Typical Application Data."

electrical characteristics, $V_{CC\pm}$ = ±15 V, V_{IC} = 0, R_S = 0, pin 1 at V_{CC-}, output at pin 7 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1011			LT1011A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	I_O = 1.5 mA, V_O = 0	25°C		0.6	1.5		0.3	0.5	mV
			Full range			3			1	
		R_S ≤ 50 kΩ, See Note 5	25°C			2			0.75	
			Full range			3			1.5	
αV_{IO}	Average temperature coefficient of input offset voltage	See Note 6	Full range		4	25		4	15	µV/°C
I_{IO}	Input offset current	See Note 5	25°C		0.2	4		0.2	3	nA
			Full range			6			5	
I_{IB}	Input bias current	I_O = 1.5 mA, V_O = 0	25°C		−20	±50		−15	±25	nA
		See Note 5	25°C		−25	±65		−20	±35	
			Full range			±80			±50	
$I_{IL(S)}$	Low-level strobe current (See Note 7)		25°C			−500			−500	µA
V_{ICR}	Common-mode input voltage range		Full range	−14.5 to 13			−14.5 to 13			V
A_{VD}	Large-signal differential voltage amplification	R_L = 1 kΩ to V_{CC+}, V_O = −10 V to 14.5 V	25°C	200	500		200	500		V/mV
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 8 mA, Pin 1 at 0 V	Full range			0.4			0.4	V
		V_{ID} = −5 mV, I_{OL} = 50 mA, Pin 1 at 0 V	Full range			1.5			1.5	
$I_{O(lkg)}$	Output leakage current	V_{ID} = 5 mV, Pin 1 at −15 V, V_O = 35 V (25 V for LT1011C)	25°C		0.2	10		0.2	10	nA
			Full range			500			500	
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR\ min}$, R_S ≤ 50 kΩ	25°C	90	115		94	115		dB
I_{CC+}	Supply current from V_{CC+}		25°C		3.2	4		3.2	4	mA
I_{CC-}	Supply current from V_{CC-}		25°C		−1.7	−2.5		−1.7	−2.5	mA
C_i	Input capacitance		25°C		6			6		pF

† Full range is −55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

NOTES: 5. These specifications apply for single supply voltages from 5 V to 30 V and dual supply voltages from ±2.5 V to ±15 V for the entire input voltage range, and for both high and low output states. The high state is I_{OH} ≥ 100 µA and V_O ≥ (V_{CC+} − 1 V). The low state is I_{OL} ≤ 8 mA and V_O ≤ 0.8 V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

6. Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.

7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.

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electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0, V_{IC} = 0, R_S = 0, pin 1 at 0 V, output at pin 7 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LT1011			LT1011A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$R_S \le 50\ k\Omega$, See Note 5	25°C			2			0.75	mV
			Full range			3			1.5	
I_{IO}	Input offset current	See Note 8	25°C		0.2	4		0.2	3	nA
			Full range			6			5	
I_{IB}	Input bias current	See Note 8	25°C		25	65		20	35	nA
			Full range			80			50	
$I_{IL(S)}$	Low-level strobe current (See Note 7)		25°C			−500			−500	µA
V_{ICR}	Common-mode input voltage range		Full range	0.5 to 3			0.5 to 3			V
A_{VD}	Large-signal differential voltage amplification	R_L = 0.5 kΩ to V_{CC+}, V_O = 0.5 V to 4.5 V	25°C	50	300		50	300		V/mV
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 8 mA	Full range			0.4			0.4	V
		V_{ID} = −5 mV, I_{OL} = 50 mA	Full range			1.5			1.5	
I_O	Output leakage current	V_{ID} = 5 mV, V_O = 50 V (40 V for LT1011C)	25°C		0.2	10		0.2	10	nA
			Full range			500			500	
I_{CC+}	Supply current from V_{CC+}		25°C		3.2	4		3.2	4	mA
I_{CC-}	Supply current from V_{CC-}		25°C		−1.7	−2.5		−1.7	−2.5	mA

† Full range is −55°C to 125°C for the LT1011M and LT1011AM. Full range is 0°C to 70°C for the LT1011C and LT1011AC.

NOTES: 6. Average temperature coefficient is calculated by dividing the offset voltage difference measured at minimum and maximum temperatures by the temperature difference.

7. This is the minimum current that must be drawn from the strobe to ensure that the output is off regardless of differential input voltage.

8. These specifications apply for all single-supply voltages from 5 V to 30 V for the entire input voltage range, and for both high and low output states. The high state is $I_{OH} \ge 100\ \mu A$ and $V_O \ge (V_{CC+} - 1\ V)$. The low state is $I_{OL} \le 8$ mA and $V_O \le 0.8$ V. Therefore, this specification defines a worst-case error band that includes effects due to common-mode signals, voltage gain, and output load.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 0, pin 1 at 0 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	LT1011			LT1011A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Output response time	R_C = 500 Ω to 5 V, C_L = 5 pF, See Note 9		150	250		150	250	ns

NOTE 9: The response time specified is for a 100-mV input step with 5-mV overdrive and is the interval between the input step function and the instant when the output crosses 1.4 V.

TYPICAL CHARACTERISTICS†

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

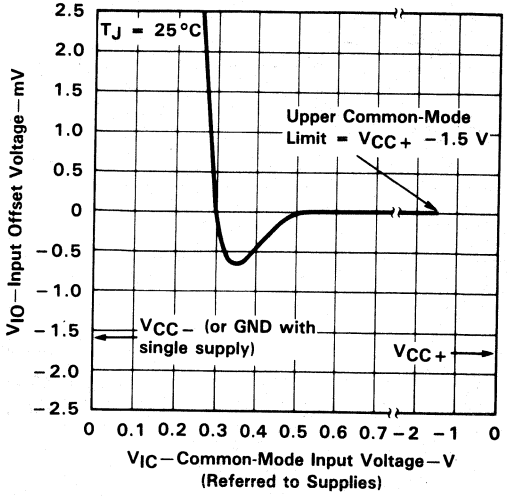

FIGURE 1

OFFSET ADJUSTMENT CHARACTERISTICS

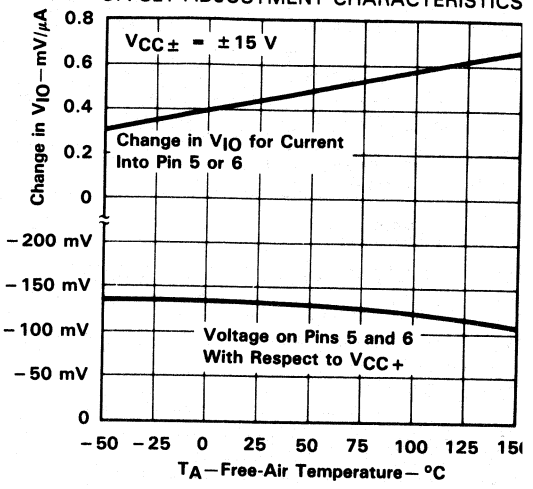

FIGURE 2

INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

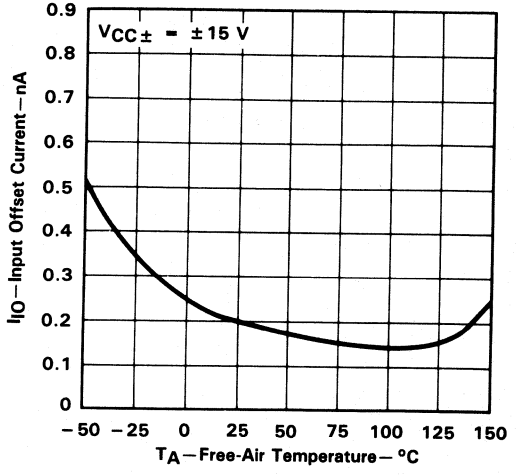

FIGURE 3

LT1011
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

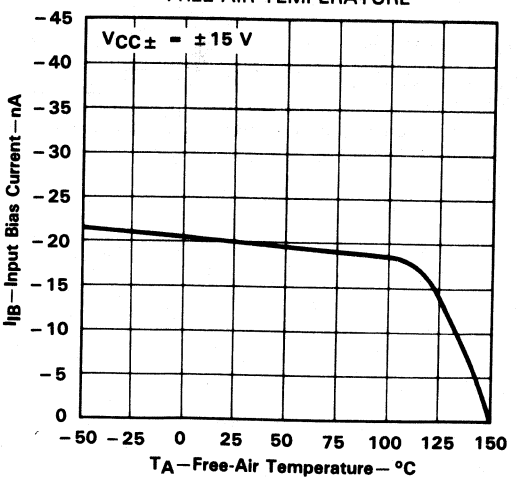

FIGURE 4

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

INPUT VOLTAGE LIMITS
vs
FREE-AIR TEMPERATURE

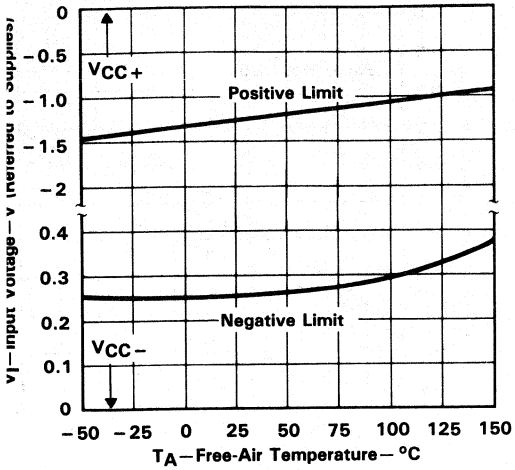

FIGURE 5

LT1011
INPUT CHARACTERISTICS
(EITHER INPUT WITH OTHER
INPUT GROUNDED)

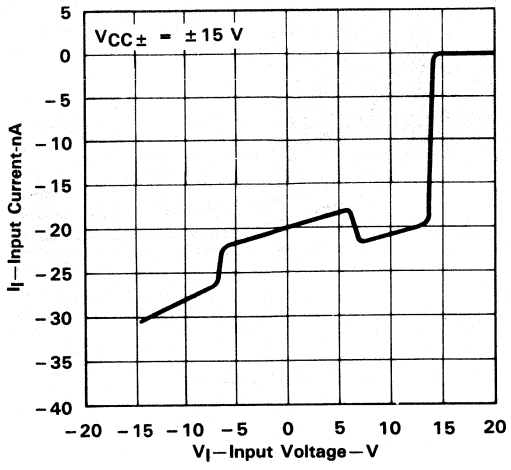

FIGURE 6

EQUIVALENT OFFSET VOLTAGE
vs
SOURCE RESISTANCE

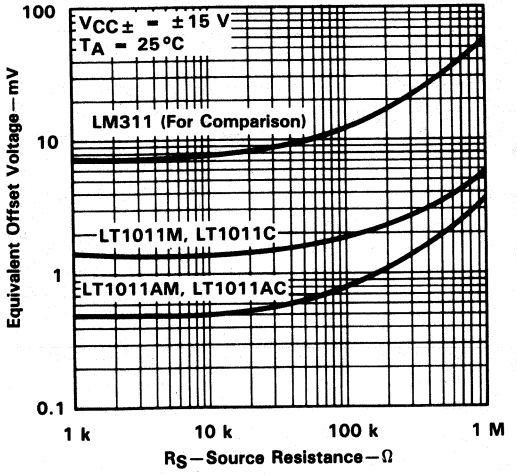

FIGURE 7

VOLTAGE TRANSFER CHARACTERISTICS

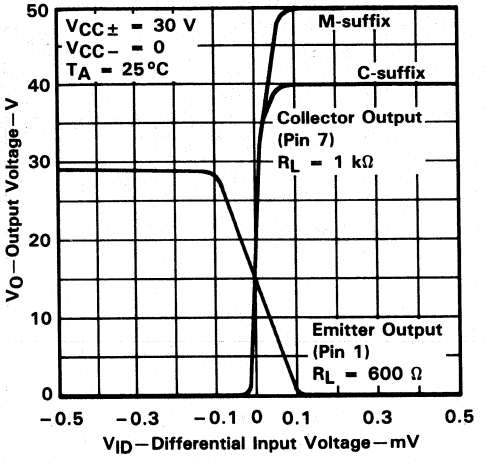

FIGURE 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
INPUT OVERDRIVE

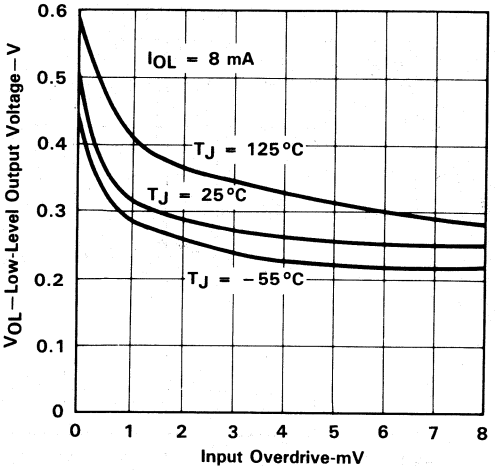

FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

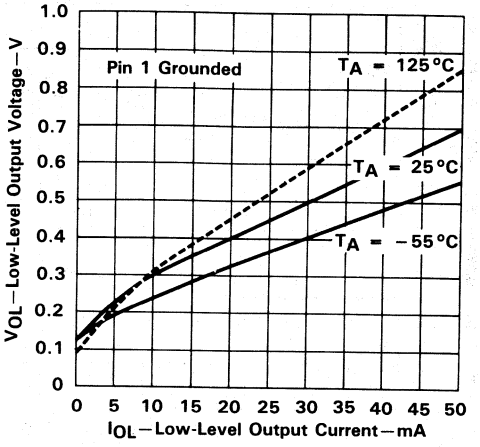

FIGURE 10

OUTPUT LEAKAGE CURRENT
vs
FREE-AIR TEMPERATURE

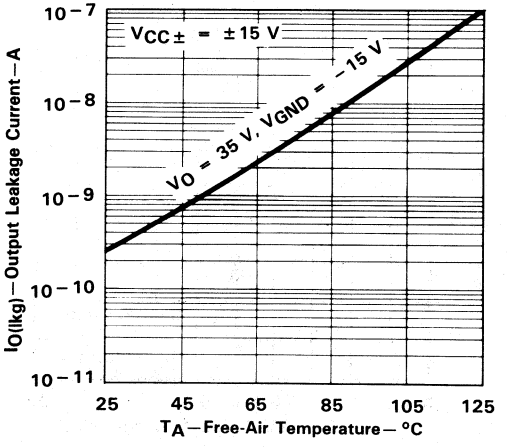

FIGURE 11

SHORT-CIRCUIT OUTPUT CURRENT
AND DISSIPATION
(3 MINUTES AFTER SHORT)
vs
OUTPUT VOLTAGE

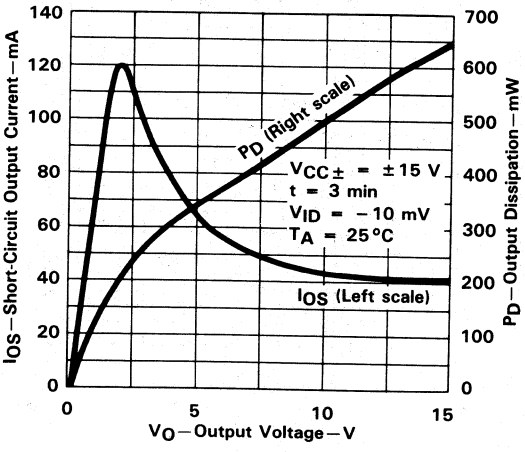

FIGURE 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

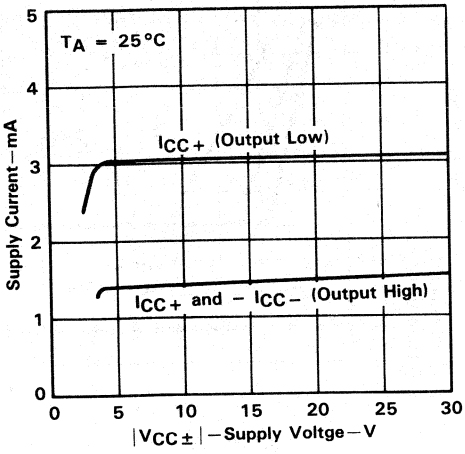

FIGURE 13

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

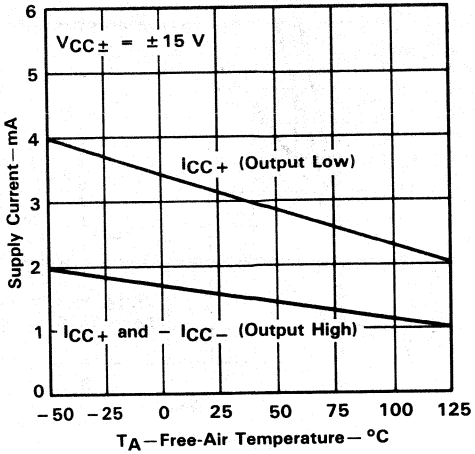

FIGURE 14

OUTPUT SATURATION VOLTAGE
(GROUND INPUT)
vs
OUTPUT CURRENT

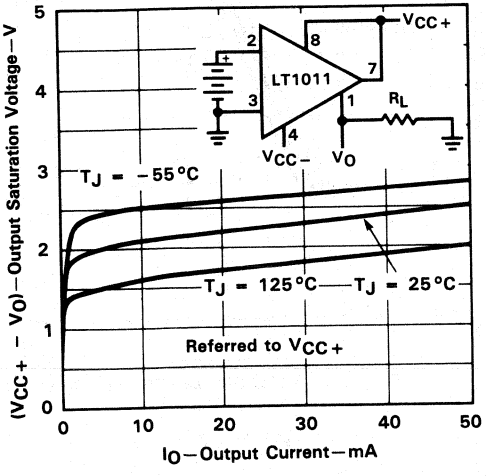

FIGURE 15

OUTPUT RESPONSE TIME
vs
INPUT STEP SIZE

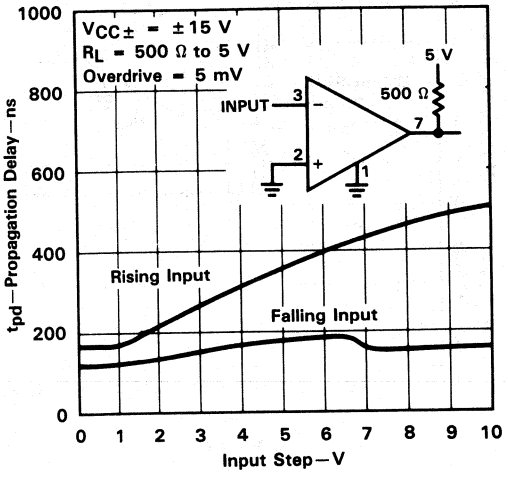

FIGURE 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

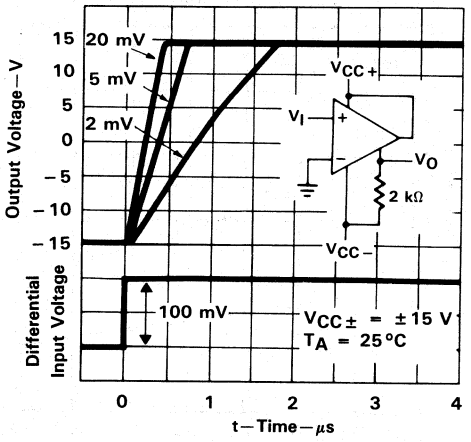

FIGURE 17

OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

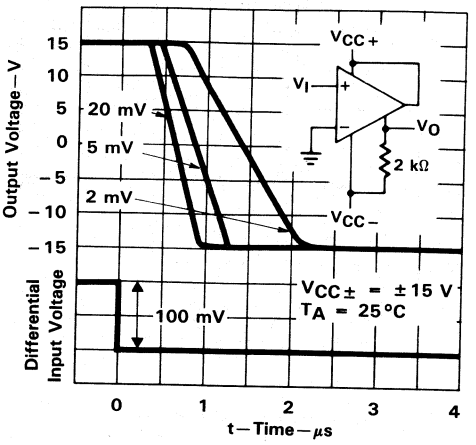

FIGURE 18

HIGH- TO LOW-LEVEL
OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

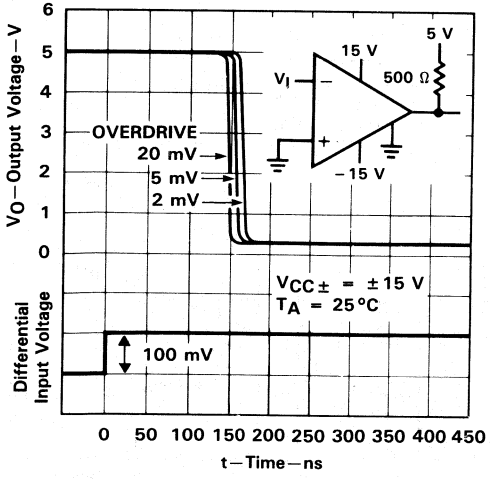

FIGURE 19

LOW- TO HIGH-LEVEL
OUTPUT RESPONSE
FOR VARIOUS INPUT OVERDRIVES

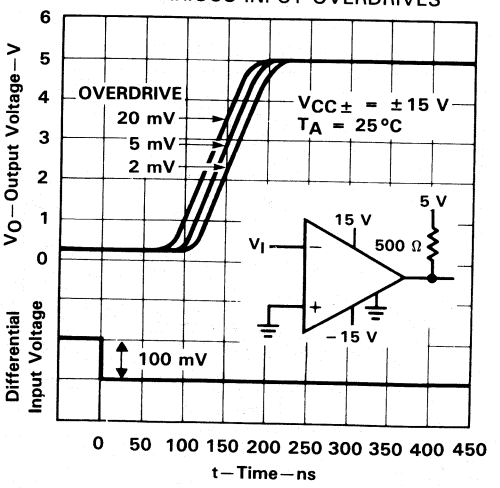

FIGURE 20

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TYPICAL APPLICATION DATA

eventing oscillation problems

Oscillation problems in comparators are often caused by stray capacitance between the output and inputs or between the output and other sensitive pins on the comparator. This is especially true for comparators with high gain and wide bandwidth, like the LT1011 (GBW ≥ 10 GHz), that are designed for fast switching with millivolt input signal levels. Because oscillation problems tend to occur at frequencies around 5 MHz, where the LT1011 has a gain of approximately 2 V/mV, attenuation of output signals must be at least 2000:1 at 5 MHz as measured at the inputs. If the source impedance is 1 kΩ, the effective stray capacitance between output and input must have a reactance of more than (2000)(1 kΩ) = 2 MΩ, or less than 2 pF. The actual inter-lead capacitance between input and output pins on the LT1011 is less than 0.002 pF when cut to mounting length for printed circuit boards. Additional stray capacitance due to printed circuit traces must be minimized by routing the output trace directly away from input lines and, if possible, running ground traces next to input traces to provide shielding.

Additional steps to prevent oscillation problems are:

1. Bypass the strobe/balance pins with a 0.01-μF capacitor connected from pin 5 to pin 6 to eliminate stray capacitive feedback from the output to the balance pins. The balance pins are nearly as sensitive to stray capacitive feedback as the inputs.
2. Bypass the negative supply (pin 4) with a 0.1-μF ceramic capacitor close to the comparator. A 0.1-μF capacitor can also be used for the positive supply (pin 8) if the pull-up load is tied to a separate supply. When the pull-up load is tied directly to pin 8, use a 2-μF solid tantalum bypass capacitor.
3. Bypass any slow-moving or dc input with a capacitor (≥ 0.01 μF) close to the comparator to reduce high-frequency source impedance.
4. Keep resistive source impedance as low as possible. If a resistor is added in series with one input, bypass it with a capacitor to balance source impedances for dc accuracy. The low input bias current of the LT1011 usually eliminates any need for source resistance balancing. A 5-kΩ imbalance, for example, creates only 0.25-mV offset.
5. Use hysteresis, which consists of shifting the input offset voltage of the comparator when the output changes state. Hysteresis forces the comparator to move quickly through its linear region, eliminating oscillations by "overdriving" the comparator under all input conditions. Hysteresis may be either ac or dc. An ac hysteresis technique does not shift the apparent offset voltage of the comparator but requires a minimum input signal slew rate to be effective. A dc hysteresis technique works for all input slew rates but creates a shift in offset voltage dependent on the previous condition of the input signal.

   The circuit shown in Figure 21 is an excellent compromise between ac and dc hysteresis. The 0.003-μF capacitor from pin 6 to pin 8 generates ac hysteresis by slightly shifting the voltage on the balance pins; both pins move about 4 mV depending on the state of the output. If pin 6 is bypassed, a level of ac hysteresis is created that is sufficient to switch the output at a speed near the comparator's maximum speed.

A small amount of dc hysteresis is also used to prevent problems due to low values of input slew rate. The sensitivity of the balance pins to current is about 0.5-mV input referred offset for each microampere of balance pin current. The 15-MΩ resistor tied from output to pin 5 generates 0.5-mV dc hysteresis.

The circuit is especially useful for general-purpose comparator applications because it does not force any signals directly back onto the input signal source. Instead, it takes advantage of the unique properties of the balance pins to provide extremely fast, clean output switching even with low-frequency input signals in the millivolt range. The combination of ac and dc hysteresis creates clean oscillation-free switching with very small input errors. The curve in Figure 22 plots input referred error versus switching frequency for the circuit shown in Figure 21. Note that at low frequencies, the error is simply the dc hysteresis, while at high frequencies, an additional error is created by the ac hysteresis. The high-frequency error can be reduced by reducing C_H, but lower values may not provide clean switching with very low slew-rate input signals.

TYPICAL APPLICATION DATA

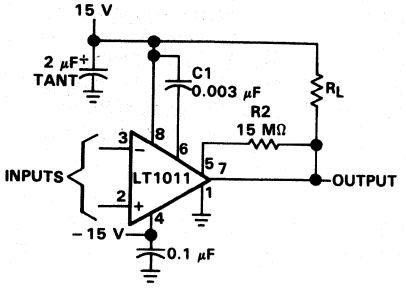


FIGURE 21. COMPARATOR WITH HYSTERESIS

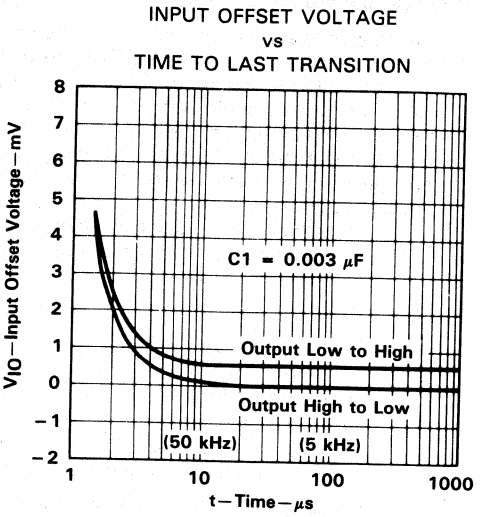
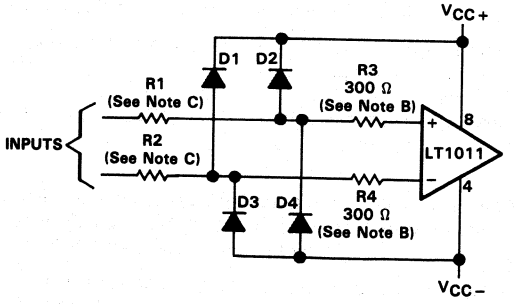


FIGURE 22

input protection

The inputs to the LT1011 are particularly suited to general-purpose comparator applications because large differential and/or common-mode voltages can be tolerated without damage to the comparator. Either or both inputs can be raised 40 V above the negative supply, independent of the positive supply voltage. Internal forward biased diodes conduct when the inputs are taken below the negative supply. In this condition, input current must be limited to 1 mA. If very large (fault) input voltages must be accommodated, series resistors and clamp diodes should be used, as shown in Figure 23.



NOTES: A. D1-D4 1N4148.
B. May be eliminated for fault current ≤ 1 mA.
C. Select according to allowable fault current and power dissipation.

FIGURE 23. LIMITING FAULT INPUT CURRENTS

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TYPICAL APPLICATION DATA

The input resistors should limit fault current to a value between 0.1 mA and 20 mA. Power dissipation in the resistors must be considered for continuous faults, especially when the LT1011 supplies are off. Lightly loaded supplies may be forced to higher voltages by large fault currents flowing through D1-D4.

R3 and R4 limit input current to the LT1011 to less than 1 mA when the input signals are held below $V_{CC}-$. They may be eliminated if R1 and R2 are large enough to limit fault current to less than 1 mA.

ıput slew rate limitations

In the LT1011, step size is important because the slew rate of internal nodes increases response time for input step sizes larger than 1 V. For example, at 5-V step size, response time increases from 150 ns to 360 ns (see Figure 16). If response time is critical and large input signals are expected, clamp diodes across the inputs are recommended. The slew rate limitation can also affect performance when differential input voltage is low, but both inputs must slew quickly. The maximum suggested common-mode slew rate is 10 V/μs.

trobing

The LT1011 can be strobed by pulling current out of the strobe pin. The output transistor is forced to an off state, giving a high output at the collector (pin 7). Currents as low as −250 μA may cause strobing, but when the strobe current is low, strobe delay increases to between 200 ns and 300 ns. If strobe current is increased to −3 mA, strobe delay drops to about 60 ns. When the strobe current is 0, the voltage at the strobe pin is approximately 150 mV below $V_{CC}+$; when the strobe current is increased to −3 mA, the strobe pin voltage is approximately 2 V below $V_{CC}+$. Do not ground the strobe pin; it must be current driven.

Figure 24 shows a typical strobe circuit. Note that there is no bypass capacitor between pins 5 and 6, which maximizes strobe speed but leaves the comparator more sensitive to oscillation problems for slow, low-level inputs. A 1-pF capacitor between the output and pin 5 greatly reduces oscillation problems without reducing strobe speed.

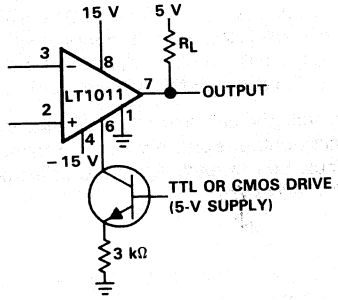

FIGURE 24. TYPICAL STROBE CIRCUIT

Placing a resistor from the output to pin 5 adds dc hysteresis. See step number 5 under "preventing oscillation problems."

The pin that is used for strobing (pin 6) is also one of the offset adjustment pins. Current into or out of pin 6 must be kept very low (<0.2 μA) when not strobing to prevent input offset voltage shifts.

output transistor

When the LT1011 output transistor is in the off state, negligible current flows into or out of the collector or emitter. The equivalent circuit is shown in Figure 25.

TYPICAL APPLICATION DATA

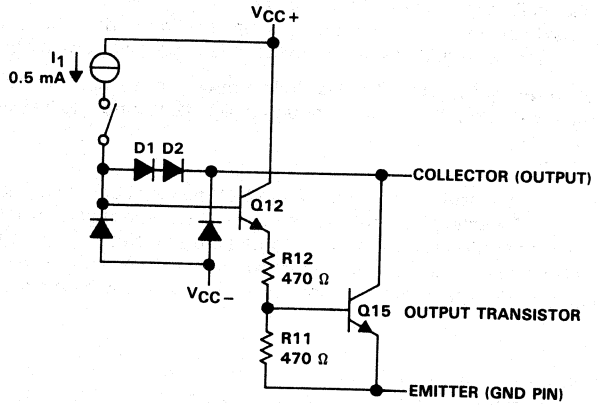

FIGURE 25. OUTPUT TRANSISTOR CIRCUITRY

output transistor (continued)

In the off state, I_1 is switched off and both Q12 and Q15 turn off. The collector of Q15 can then be held above V_{CC-} without conducting current. The maximum voltage above V_{CC-} is 50 V for the LT1011 and 40 V for the LT1011C (these maximum voltages may exceed V_{CC+}). The emitter can be held at any voltage between V_{CC-} and V_{CC+} as long as the voltage is negative with respect to the collector.

In the on state, I_1 is connected, which turns on both Q12 and Q15. Diodes D1 and D2 prevent deep saturation of Q15 to improve speed and also limit the drive current of Q12. The R11/R12 divider sets the saturation voltage of Q15 and provides turn-off drive. Either the collector or emitter pin can be held at a voltage between V_{CC-} and V_{CC+}, which allows the remaining pin to drive the load. In typical applications, the emitter is connected to V_{CC-} or ground, and the collector drives a load tied to V_{CC+} or a separate positive supply.

When the emitter is used as the output, the collector is typically tied to V_{CC+}, and the load is connected to ground or V_{CC-}. Note that the emitter output is phase reversed with respect to the collector output so that the "+" and "−" input designations must be reversed. When the collector is tied to V_{CC+}, the voltage at the emitter in the one state is about 2 V below V_{CC+}.

input signal range

The input voltage range of the LT1011 is typically 300 mV above the negative supply and 1.5 V below the positive supply, independent of the actual supply voltages. This is the input voltage range over which the output will respond correctly when a voltage within the range is applied to one input and a higher or lower signal is applied to the other input. If one input is inside the range and one is outside, the output will be correct. If both inputs are outside the range, in opposite directions, the output will still be correct. If, however, both inputs are outside the range in the same direction, the output will not respond to the differential input; it will remain unconditionally off.

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TYPICAL APPLICATIONS

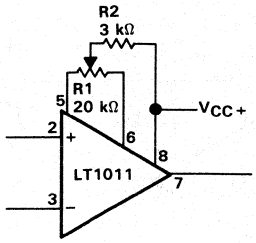
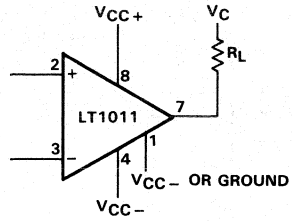
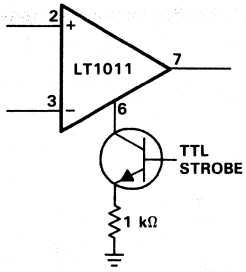


FIGURE 26. OFFSET BALANCING



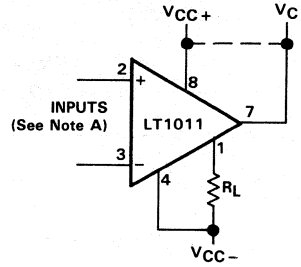
NOTE: V_C can be greater or less than V_{CC+}.

FIGURE 28. DRIVING LOAD REFERENCED TO POSITIVE SUPPLY



NOTE: Do not ground strobe pin.

FIGURE 27. STROBING



NOTE A: Input polarity is reversed when using Pin 1 for output.

FIGURE 29. DRIVING LOAD REFERENCED TO NEGATIVE SUPPLY

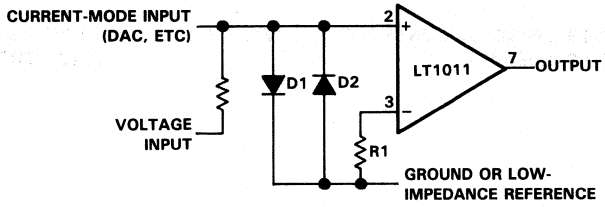
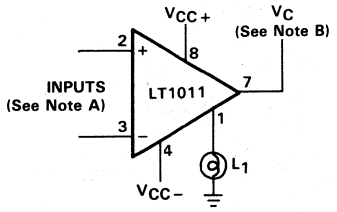


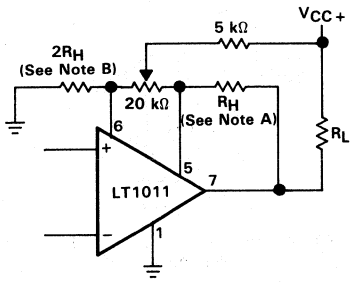
FIGURE 30. USING CLAMP DIODES TO IMPROVE FREQUENCY RESPONSE (See Figure 16)

TYPICAL APPLICATIONS



NOTES: A. Input polarity is reversed when using Pin 1 for output.
B. V_C may be any voltage above V_{CC-}. Pin 1 swings to within approximately 2 V of V_{CC+}.

FIGURE 31. DRIVING LOAD REFERENCED TO GROUND



NOTES: A. Hysteresis is approximately 0.45 mV/μA change in current in R_H.
B. This resistor causes hysteresis to be centered around V_{IO}.

FIGURE 32. COMBINING OFFSET ADJUSTMENT AND HYSTERESIS

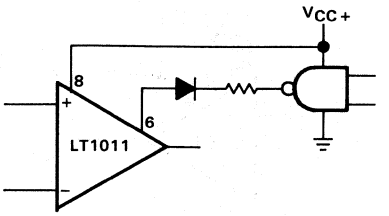


FIGURE 33. DIRECT STROBE DRIVE WHEN CMOS LOGIC USES SAME V_{CC+} SUPPLY AS LT1011
(Not applicable for TTL logic)

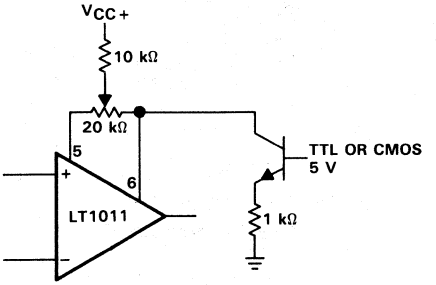
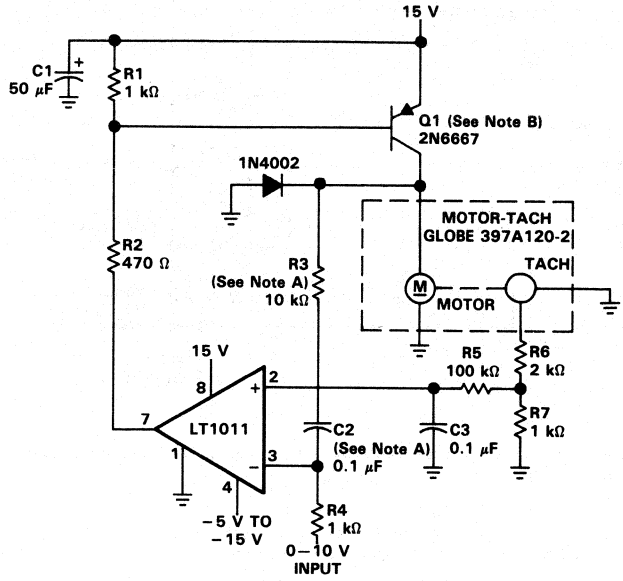


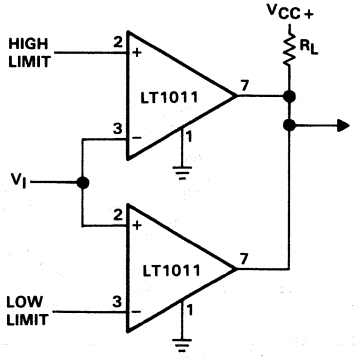
FIGURE 34. COMBINING OFFSET ADJUSTMENT AND STROBE

TYPICAL APPLICATIONS



NOTES: A. R3/C2 determines oscillation frequency of controller.
B. Q1 operates in switch mode.

FIGURE 35. HIGH-EFFICIENCY MOTOR SPEED CONTROLLER



NOTE: Output is high inside "window" and low above high limit or below low limit.

FIGURE 36. WINDOW DETECTOR

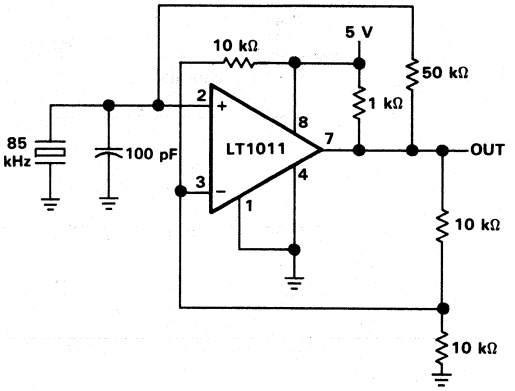
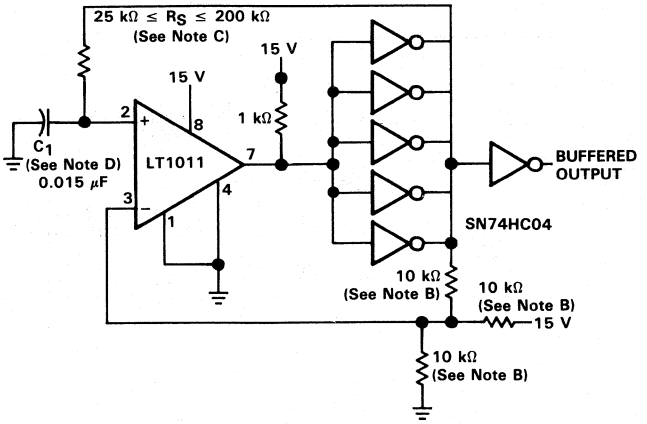


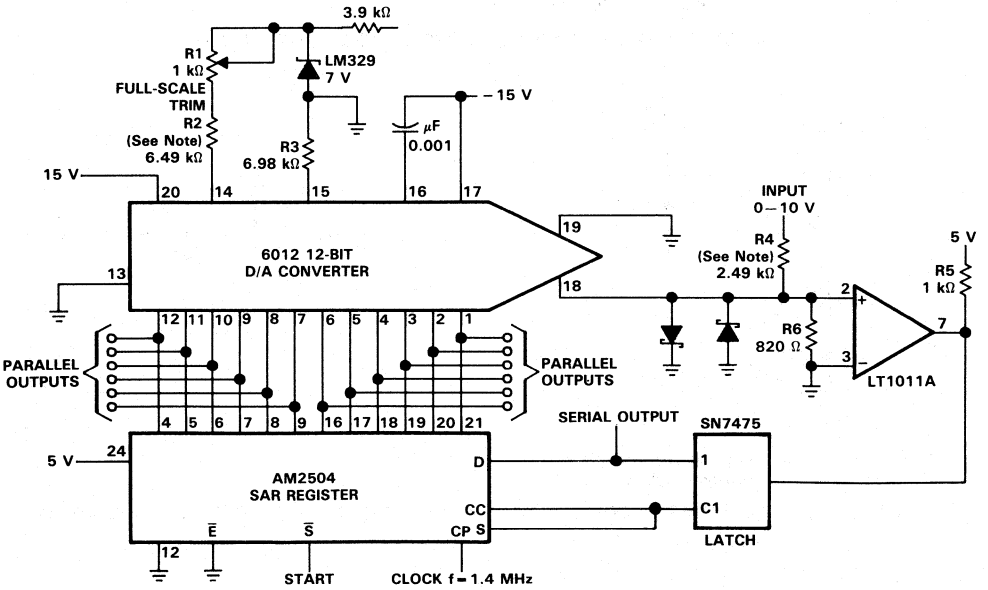
FIGURE 37. CRYSTAL OSCILLATOR

TYPICAL APPLICATIONS



NOTES: A. Low drift and accurate frequency are obtained because this configuration rejects effects due to input offset voltage and inpu bias current of the comparator.
B. 1% metal film.
C. R_S = TRW type MTR-5/ + 120 ppm/°C.
D. C_1 = 0.015 μF = polystyrene : 120 ppm/°C ±30 ppm WESCO type 32-P.
E. Comparator contributes ≤ 10 ppm/°C drift for frequencies below 10 kHz.

FIGURE 38. LOW-DRIFT R/C OSCILLATOR



NOTE: R2 and R4 should TC track.

FIGURE 39. 10-μs 12-BIT A-D CONVERTER

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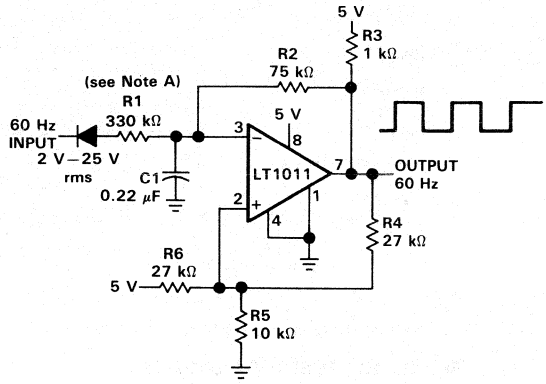
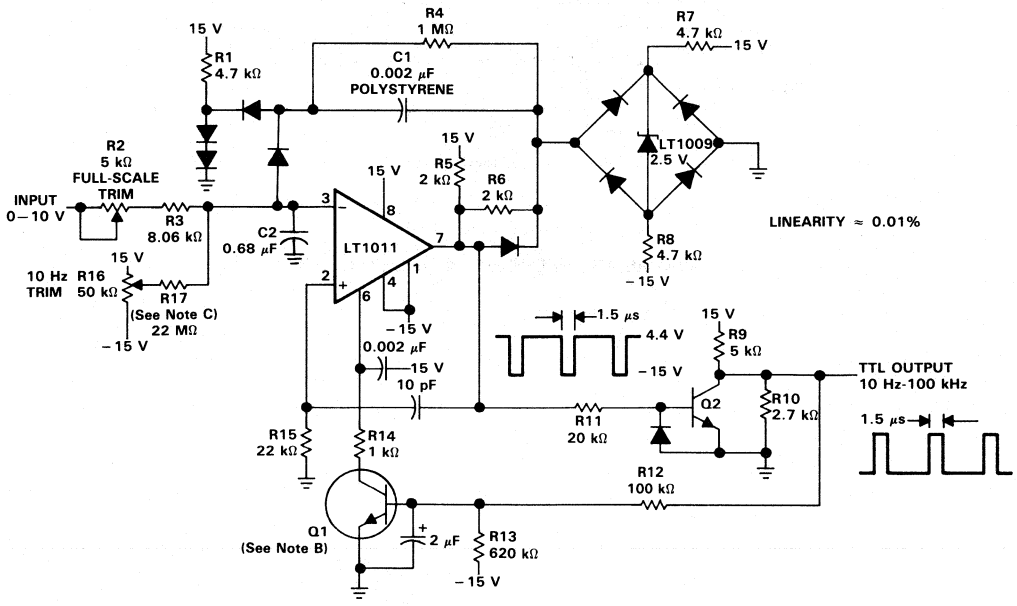
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATIONS



NOTES: A. Increase R1 for larger input voltages.
B. LT1011 self-oscillates at approximately 60 Hz, thereby "locking" onto incoming line signal.

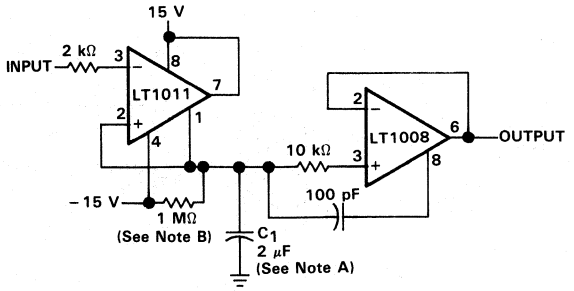
FIGURE 40. NOISE-IMMUNE 60-Hz LINE SYNCHRONIZATION



NOTES: A. All diodes 1N4148, transistors 2N3904.
B. Used only to guarantee start-up.
C. R17 may be increased for better 10-Hz trim resolution.

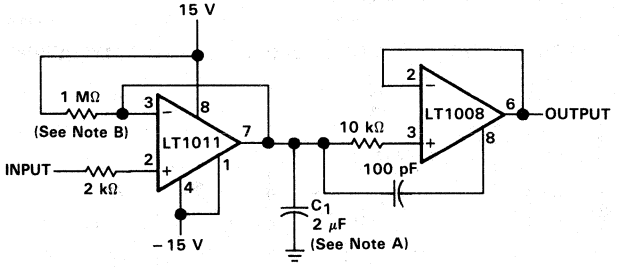
FIGURE 41. 10-Hz TO 100-kHz VOLTAGE-TO-FREQUENCY CONVERTER

TYPICAL APPLICATIONS



NOTES: A. Mylar
B. Set for required reset time constant.

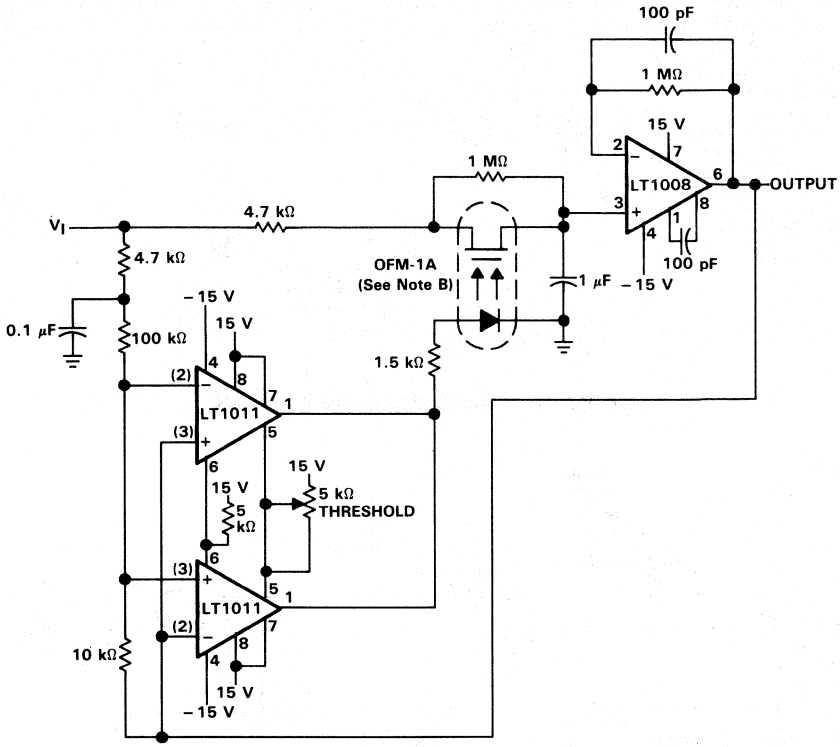
FIGURE 42. POSITIVE PEAK DETECTOR



NOTES: A. Mylar
B. Select for required reset time constant.

FIGURE 43. NEGATIVE PEAK DETECTOR

TYPICAL APPLICATIONS



NOTES: A. The comparators drive the opto-coupled FET "on" when the difference between the output and the input exceeds threshold. When the output approaches the input, the FET turns "off" and low-pass filtering occurs.
B. From Theta-J Corporation, Woburn, Massachusetts.

FIGURE 44. FAST-SETTLING FILTER

TYPICAL APPLICATIONS

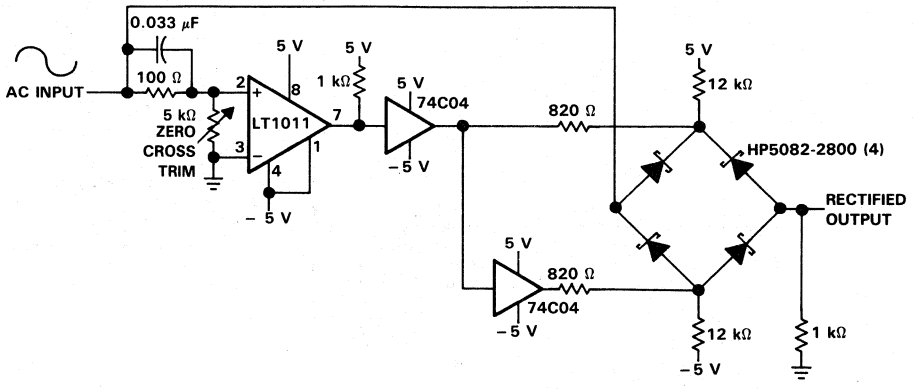
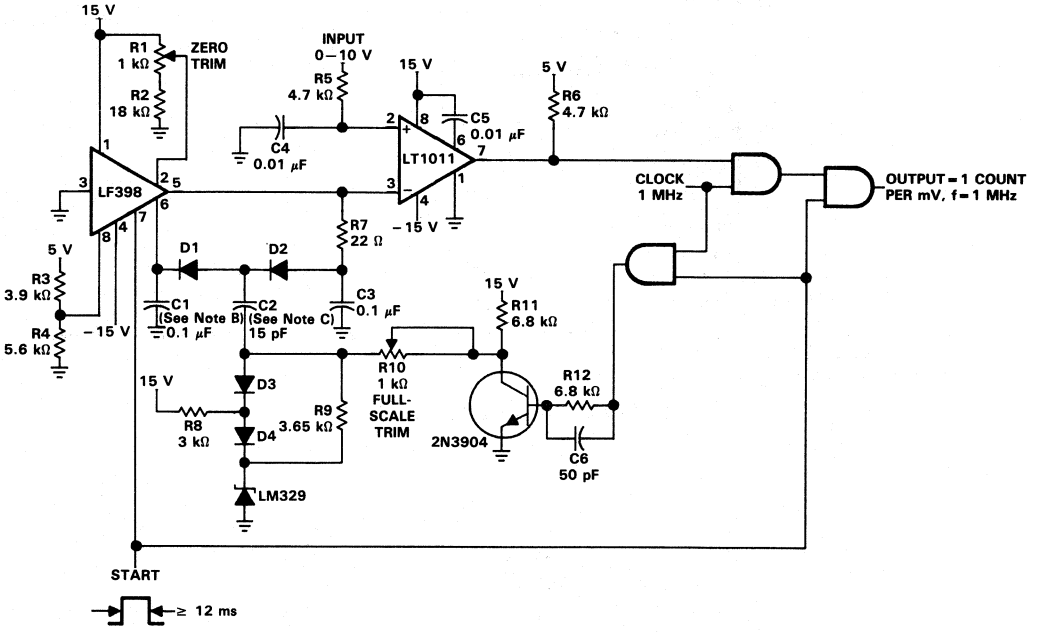


FIGURE 45. 100-kHz PRECISION RECTIFIER



NOTES: A. All diodes 1N4148
B. Polystyrene
C. NPO

FIGURE 46. 4-DIGIT (10,000-COUNT) A-D CONVERTER

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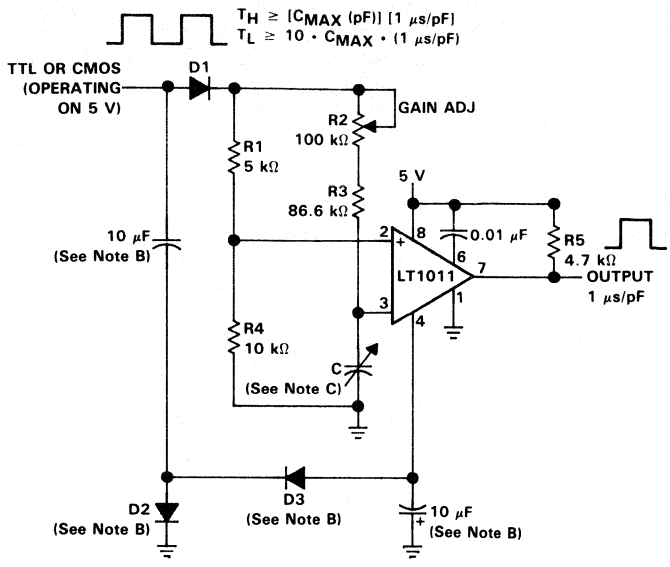
TYPICAL APPLICATIONS



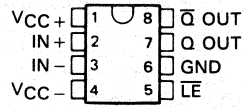
NOTES: A. PW = (R2 + R3) • (C) • [(R1 + R4)/R1]. The input capacitance of the LT1011 is approximately 6 pF. This is an offset term.
B. These components may be eliminated if negative supply is available (−1 V to −15 V).
C. Typical two sections of 365-pF variable capacitor when used as shaft-angle indication.

FIGURE 47. CAPACITANCE-TO-PULSE-WIDTH CONVERTER

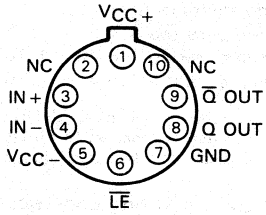
D3242, MAY 1988—REVISED MARCH 1989

- **Ultra-Fast . . . 10 ns Typ t_{pd}**
- **Operates from Single 5-V or Dual ±5-V Supply**
- **Complementary TTL Outputs**
- **Low Input Offset Voltage . . . 0.8 mV or 1 mV Typ**
- **No Minimum Input Slew Rate Requirement**
- **No Supply Current Spiking**
- **Output Latch**

D, JG, OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



NC—No internal connection.

All leads of the L package are electrically insulated from the case.

Description

The LT1016 is an ultra-fast comparator specifically designed to interface directly to TTL logic while operating from either a dual ±5-V supply or a single 5-V supply. The LT1016 offers tight offset voltage specifications and high gain for precision applications. Matched complementary outputs further extend the versatility of the LT1016.

The LT1016 features a unique output stage that provides active drive in both directions for maximum speed into TTL-logic or passive loads yet does not exhibit the large current spikes normally found in totem-pole output stages. This eliminates the need for a minimum input slew rate typical of other fast comparators. The LT1016's ability to remain stable with the outputs in the active region greatly reduces the problem of output "glitching" when the input signal is slow moving or is at a low level.

The LT1016 has a true latch for retaining input data at the outputs. The outputs remain latched as long as the latch enable input $\overline{LE}$ is high. Quiescent negative supply current is only 3 mA, about ten times lower than competitive units. This feature reduces die temperature and allows the negative supply pin to be driven from virtually any supply voltage with a simple resistive divider. Device performance is not affected by variations in negative supply voltage.

The LT1016M is characterized for operation over the full military temperature range of −55°C to 125°C. The LT1016C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	LT1016CD	LT1016CJG	LT1016CL	LT1016CP
−55°C to 125°C		LT1016MJG	LT1016ML	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LT1016CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC-} . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±5 V
Input voltage (either input) . . . . . $V_{CC\pm}$
Latch enable input voltage . . . . . $V_{CC\pm}$
Output current, I_O . . . . . ±20 mA
Operating free-air temperature range: LT1016M . . . . . −55°C to 125°C
LT1016C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: L package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The output may be shorted to ground or to either power supply.

recommended operating conditions

		LT1016M			LT1016C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}				5			5	V
Supply voltage, V_{CC-}				−5			−5	V
Input voltage, V_I	$V_{CC\pm}$ = ±15 V	−3.75		3.5	−3.75		3.5	V
	V_{CC+} = 5 V, V_{CC-} = 0	1.25		3.5	1.25		1.25	
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $V_{O(Q)}$ = 1.4 V, $\overline{LE}$ at 0 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A†	LT1016M			LT1016C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage (see Note 4)	$R_S \leq 100\ \Omega$	25°C		0.8	2		1	3	mV
			Full range			3			3.5	
αV_{IO}	Average temperature coefficient of input offset voltage		Full range		4			4		μV/°C
I_{IO}	Input offset current (see Note 4)		25°C		0.3	1		0.3	1	μA
			Full range			1.3			1.3	
I_{IB}	Input bias current (see Note 5)	V_O = 1.4 V	25°C		5	10		5	10	μA
			Full range			13			13	
V_{ICR}	Common-mode input voltage range	Dual supply	Full range	−3.75 to 3.5			−3.75 to 3.5			V
		Single supply	Full range	1.25 to 3.5			1.25 to 3.5			
V_I	Input voltage	$\overline{LE}$ high	Full range	2			2			V
		$\overline{LE}$ low	Full range			0.8			0.8	
V_{OH}	High-level output voltage	$V_{CC+} \leq 4.6$ V, I_O = 1 mA	Full range	2.7			2.7			V
		$V_{CC+} \leq 4.6$ V, I_O = 10 mA		2.4			2.4			
V_{OL}	Low-level output voltage	I_O = 4 mA	Full range			0.5			0.5	V
		I_O = 10 mA	25°C		0.4			0.4		
A_{VD}	Small-signal differential voltage amplification	V_O = 1 V to 2 V	25°C	1400	3000		1400	3000		V/V
CMRR	Common-mode rejection ratio	V_{IC} = −3.75 V to 3.5 V	Full range	80			80			dB
k_{SVR}	Supply voltage rejection ratio	Positive supply, V_{CC+} = 4.6 V to 5.4 V	Full range	60			60			dB
		Negative supply, V_{CC-} = 2 V to 7 V		80			80			
I_{CC+}	Supply current from V_{CC+}		Full range			35			35	mA
I_{CC-}	Supply current from V_{CC-}		Full range			5			5	mA
I_I	Latch pin input current		Full range			500			500	μA

Full range is −55°C to 125°C for the LT1016M. Full range is 0°C to 70°C for the LT1016C.

NOTES: 4. Input offset voltage is defined as the average of the two voltages measured by forcing first one output and then the other to 1.4 V. Input offset current is defined in an analogous way.

5. Input bias current is defined as the average of the two input currents.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, $\overline{LE}$ at 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time	ΔV_I = 100 mV, 5-mV overdrive, See Note 6	25°C		10	14	ns
			Full range			16	
		ΔV_I = 100 mV, 20-mV overdrive, See Note 6	25°C		10	14	
			Full range			16	
Δt_{pd}	Differential propagation delay	ΔV_I = 100 mV, 5-mV overdrive, See Note 6	25°C			3	ns
	Latch minimum setup time		25°C		2		ns

†Full range is −55°C to 125°C for the LT1016M. Full range is 0°C to 70°C for the LT1016C.

NOTE 6: t_{pd} and Δt_{pd} cannot be measured in automatic-handling test equipment with low values of overdrive. The LT1016 is teste with a 1-V step and 500-mV overdrive. Correlation testing indicates that t_{pd} and Δt_{pd} limits shown can be met with this test For low overdrive conditions, V_{IO} is added to the overdrive.

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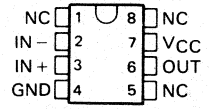
D2344, APRIL 1977—REVISED OCTOBER 1988

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage 2 to 36 V
- Low Supply Current Drain Independent of Supply Voltage . . . 0.8 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Current 3 to 5 nA Typ
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible with TTL, MOS, and CMOS

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE		
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TL331CD	TL331CJG	TL331CP
−25°C to 85°C	5 mV	TL331ID	TL331IJG	TL331IP

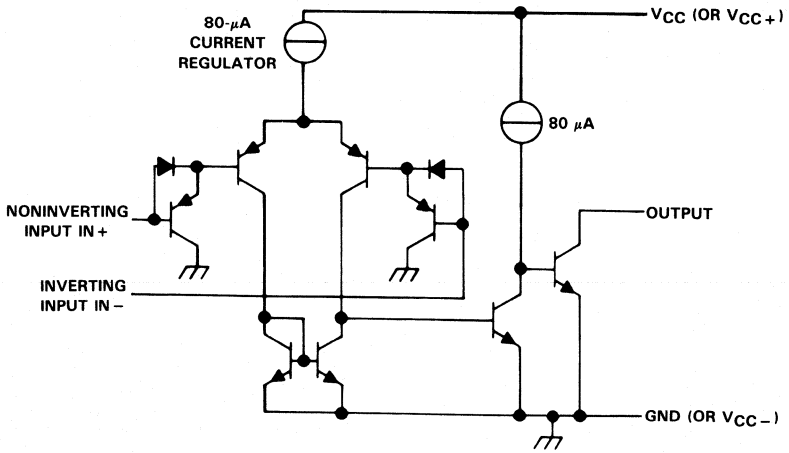
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL331CDR)

escription

The TL331 is a voltage comparator that is designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 V to 36 V and pin 7 is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage.

The TL331I is characterized for operation from −25°C to 85°C. The TL331C is characterized for operation from 0°C to 70°C.

:hematic



Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 36 V
Differential input voltage (see Note 2) . . . . . ±36 V
Input voltage range (either input) . . . . . −0.3 V to 36 V
Output voltage . . . . . 36 V
Output current . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TL331I . . . . . −25°C to 85°C
TL331C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	680 mW	5.8 mW/°C	464 mW	377 mW
JG	680 mW	6.6 mW/°C	528 mW	429 mW
P	680 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		TL331I		TL331C		UNIT
		MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		5	30	5	30	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	3	0	3	V
	V_{CC} = 30 V	0	28	0	28	
Operating free-air temperature, T_A		−25	85	0	70	°C

TEXAS INSTRUMENTS
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lectrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TL331I			TL331C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_{IC} = V_{ICR} min, V_O = 1.4 V		25°C		2	5		2	5	mV
				Full range			9			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		3	25		5	50	nA
				Full range			100			150	
I_{IB}	Input bias current			25°C		−25	−100		−25	−250	nA
				Full range			−300			−400	
V_{ICR}	Common-mode input voltage range	V_{CC} = 5 V to 30 V		25°C	0 to V_{CC}−1.5			0 to V_{CC}−1.5			V
				Full range	0 to V_{CC}−2			0 to V_{CC}−2			
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L = 15 kΩ to V_{CC}		25°C		200			200		V/mV
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1		nA
			V_{OH} = 30 V	Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400	mV
				Full range			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6			6			mA
I_{CC}	Supply current	V_O = 2.5 V,	No load	25°C		0.5	0.8		0.5	0.8	mA

Full range (MIN to MAX) for the TL331I is −25°C to 85°C and for the TL331C is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage unless otherwise specified.

witching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF,‡ See Note 4	100-mV input step with 5-mV overdrive		1.3		μs
		TTL-level input step		0.3		

C_L includes probe and jig capacitance.
OTE 4: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

D999, OCTOBER 1977—REVISED MARCH 1988

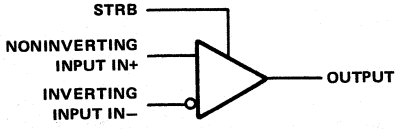
- **Fast Response Times**
- **High Differential Voltage Amplification**
- **Low Offset Characteristics**
- **Outputs Compatible with Most TTL Circuits**

lescription

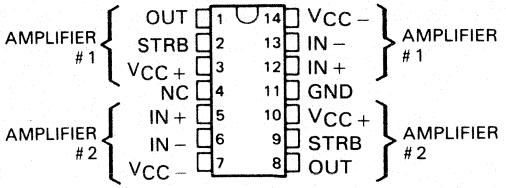
The TL514 is an improved version of the TL720 dual high-speed voltage comparator. When compared with the TL720, these circuits feature higher amplification (typically 33,000) due to an extra amplification stage, increased accuracy because of lower offset characteristics, and greater flexibility with the addition of a strobe to each comparator. Since the output cannot be more positive than the strobe, a low-level input at the strobe will cause the output to go low regardless of the differential input.

These circuits are especially useful in applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed limit detector. The TL514M is characterized for operation over the full military temperature range of −55°C to 125°C.

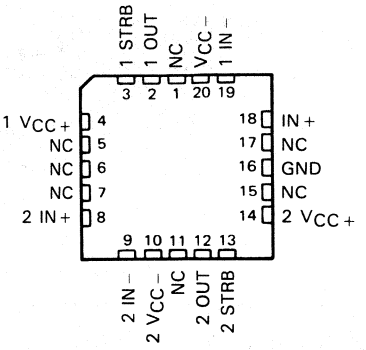
ymbol (each comparator)



J OR W PACKAGE
(TOP VIEW)



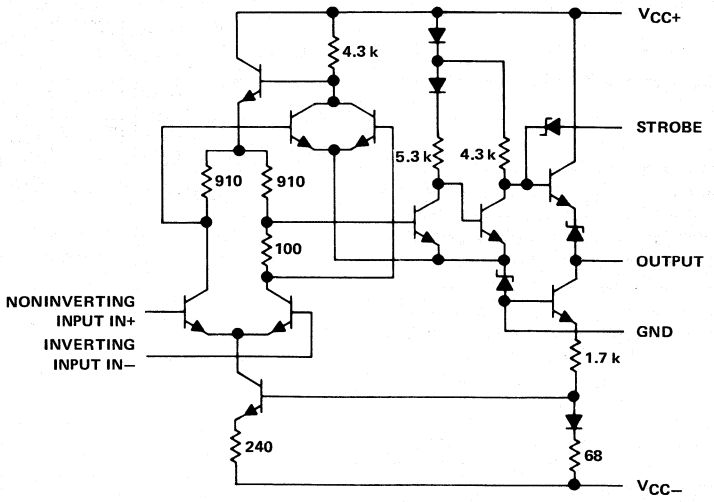
FK CHIP CARRIER
(TOP VIEW)



NC – No internal connection

3 Voltage Comparators

schematic (each comparator)



Resistor values shown are nominal in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 14 V
Supply voltage V_{CC-} (see Note 1) . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±5 V
Input voltage (any input, see Note 1) . . . . . ±7 V
Strobe voltage (see Note 1) . . . . . 6 V
Peak output current ($t_W \leq 1$ s) . . . . . 10 mA
Continuous total dissipation (either comparator or both together) . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 125°C$ POWER RATING
FK	600 mW	11.0 mW/°C	95°C	275 mW
J	600 mW	11.0 mW/°C	95°C	275 mW
W	600 mW	8.0 mW/°C	75°C	200 mW

TEXAS INSTRUMENTS
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lectrical characteristics at specified free-air temperature, V_{CC+} = 12 V, V_{CC-} = −6 V

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$R_S \le 20\ \Omega$, See Note 4	25°C		0.6	2	mV
			−55°C to 125°C			3	
α_{VIO}	Average temperature coefficient of input offset voltage	$R_S = 50\ \Omega$, See Note 4	−55°C to 25°C		3	10	μV/°C
			25°C to 125°C		3	10	
I_{IO}	Input offset current	See Note 4	25°C		0.75	3	μA
			−55°C		1.8	7	
			125°C		0.25	3	
α_{IIO}	Average temperature coefficient of input offset current	See Note 4	−55°C to 25°C		15	75	nA/°C
			25°C to 125°C		5	25	
I_{IB}	Input bias current	See Note 4	25°C		7	15	μA
			−55°C		12	25	
$I_{IH(S)}$	High-level strobe current	$V_{(strobe)}$ = 5 V, V_{ID} = −5 mV	25°C			±100	μA
$I_{IL(S)}$	Low-level strobe current	$V_{(strobe)}$ = −100 mV, V_{ID} = 5 mV	25°C		−1	−2.5	mA
V_{ICR}	Common-mode input voltage range	V_{CC} = −7 V	−55°C to 125°C	±5			V
V_{ID}	Differential input voltage range		−55°C to 125°C	±5			V
A_{VD}	Large-signal differential voltage amplification	No load, V_O = 0 to 2.5 V	25°C	12.5	33		V/mV
			−55°C to 125°C	10			
V_{OH}	High-level output voltage	V_{ID} = 5 mV, I_{OH} = 0	−55°C to 125°C		4§	5	V
		V_{ID} = 5 mV, I_{OH} = −5 mA	−55°C to 125°C	2.5	3.6§		
V_{OL}	Low-level output voltage	V_{ID} = −5 mV, I_{OL} = 0	−55°C to 125°C	−1	−0.5§	0‡	V
		$V_{(strobe)}$ = 0.3 V, V_{ID} = 5 mV, I_{OL} = 0	−55°C to 125°C	−1		0‡	V
I_{OL}	Low-level output current	V_{ID} = −5 mV, V_O = 0	25°C	2	2.4		mA
			−55°C	1	2.3		
			125°C	0.5	2.3		
r_o	Output resistance	V_O = 1.4 V	25°C		200		Ω
CMRR	Common-mode rejection ratio	$R_S \le 200\ \Omega$	−55°C to 125°C	80	100§		dB
I_{CC+}	Supply current from V_{CC+} ¶	V_{ID} = −5 mV, No load	−55°C to 125°C		11§	18	mA
I_{CC-}	Supply current from V_{CC-} ¶		−55°C to 125°C		−7§	−14	mA
P_D	Total power dissipation¶		−55°C to 125°C		180§	300	mW

Unless otherwise noted, all characteristics are measured with the strobe open.
The algebraic convention, where the most-positive (least-negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., when 0 V is the maximum, the minimum limit is a more-negative voltage.
These typical values are at T_A = 25°C.
Supply current and power dissipation limits apply for both comparators operating simultaneously.
OTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits this comparator is intended to drive.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time	R_L = ∞ C_L = 5 pF, See Note 5		30	80	ns
Strobe release time	R_L = ∞ C_L = 5 pF, See Note 6		5	25	ns

NOTES: 5. The response time specified is for a 100-mV input step with 5-mV overdrive.
6. For testing purposes, the input bias conditions are selected to produce an output voltage of 1.4 V. A 5-mV overdrive is then added to the input bias voltage to produce an output voltage which rises above 1.4 V. The time interval is measured from the 50% point of the strobe voltage curve to the point where the overdriven output voltage crosses the 1.4-V level.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

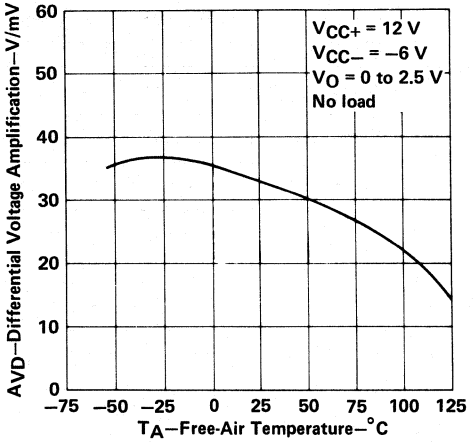

FIGURE 1

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

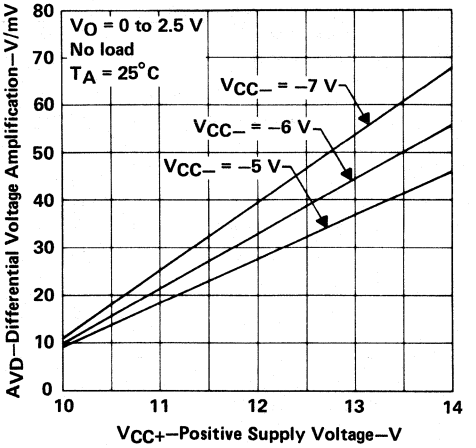

FIGURE 2

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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE LEVELS
vs
FREE-AIR TEMPERATURE

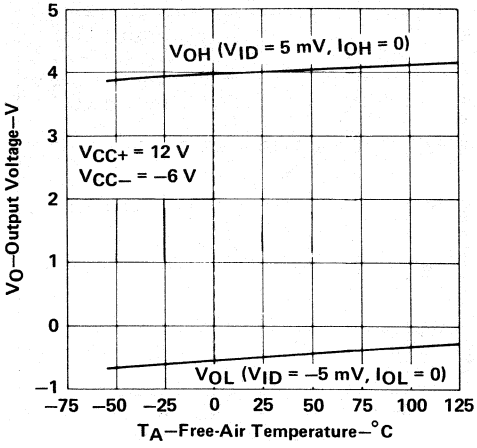

FIGURE 3

LOW-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

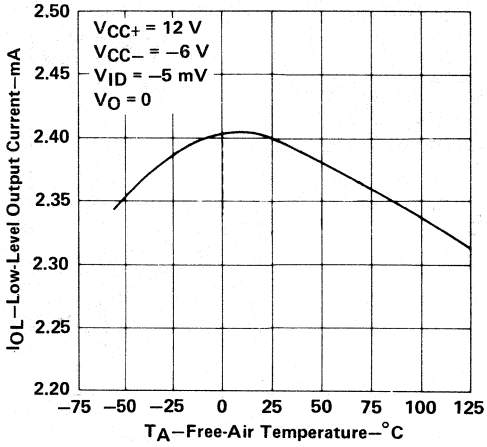

FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

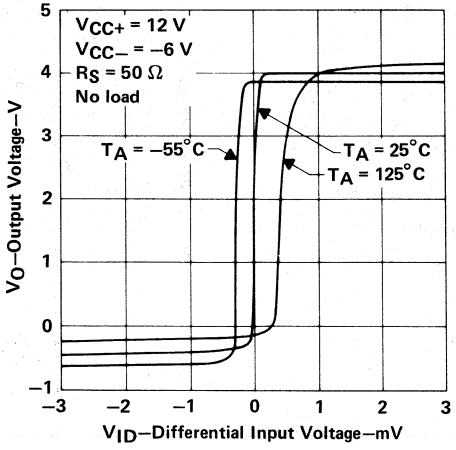

FIGURE 5

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

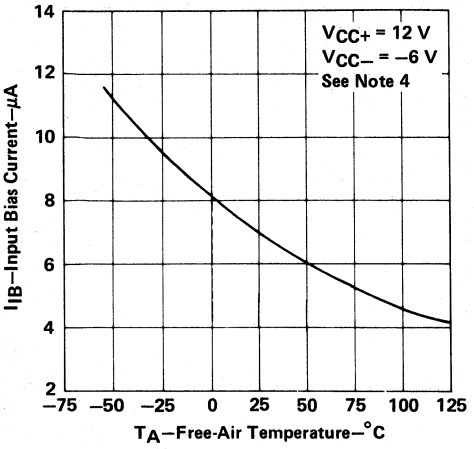

FIGURE 6

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

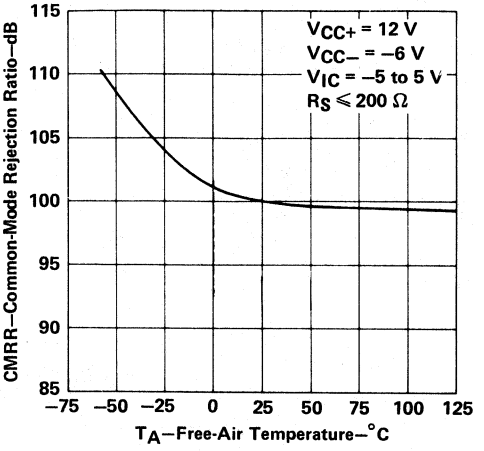

FIGURE 7

OUTPUT RESPONSE FOR
VARIOUS INPUT OVERDRIVES

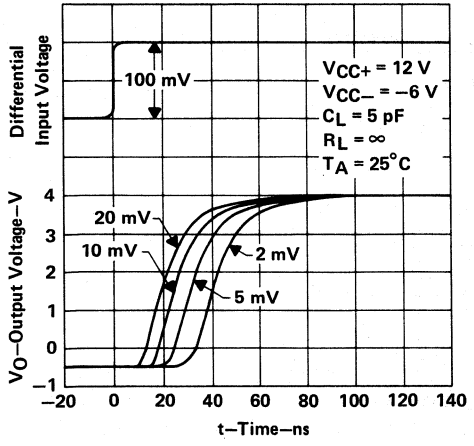

FIGURE 8

STROBE RELEASE TIME
FOR VARIOUS INPUT OVERDRIVES

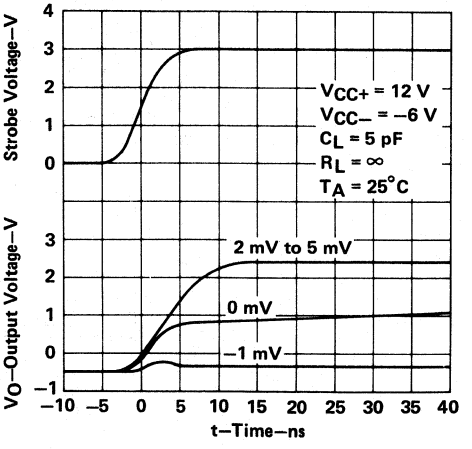

FIGURE 9

NOTE 4: These characteristics are verified by measurements at the following temperatures and output voltage levels: V_O = 1.8 V at T_A = −55°C, V_O = 1.4 V at T_A = 25°C, and V_O = 1 V at T_A = 125°C. These output voltage levels were selected to approximate the logic threshold voltages of the types of digital logic circuits this comparator is intended to drive.

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TYPICAL CHARACTERISTICS

COMMON-MODE PULSE RESPONSE

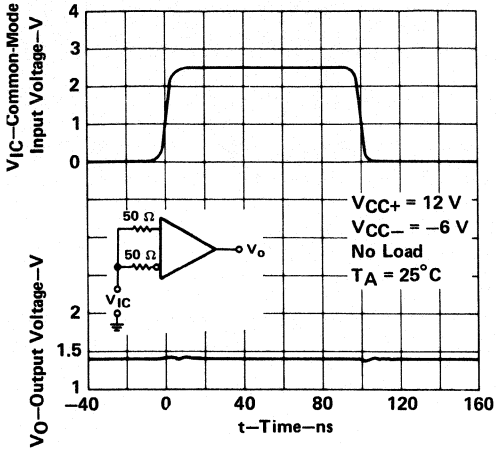


FIGURE 10

TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

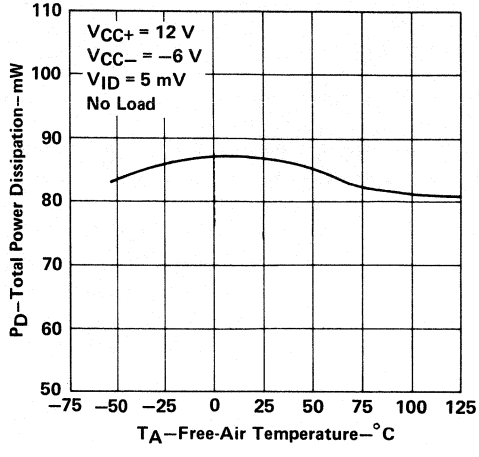
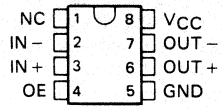


FIGURE 11

D2741, JUNE 1983—REVISED MARCH 1988

- **Operates from a 5-V Supply**
- **0 to 5 V Common-Mode Input Voltage Range**
- **Self-Biased Inputs**
- **Complementary 3-State Outputs**
- **Enable Capability**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 25 ns Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



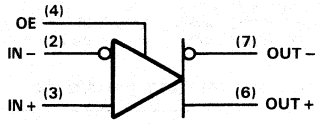
NC—No internal connection

description

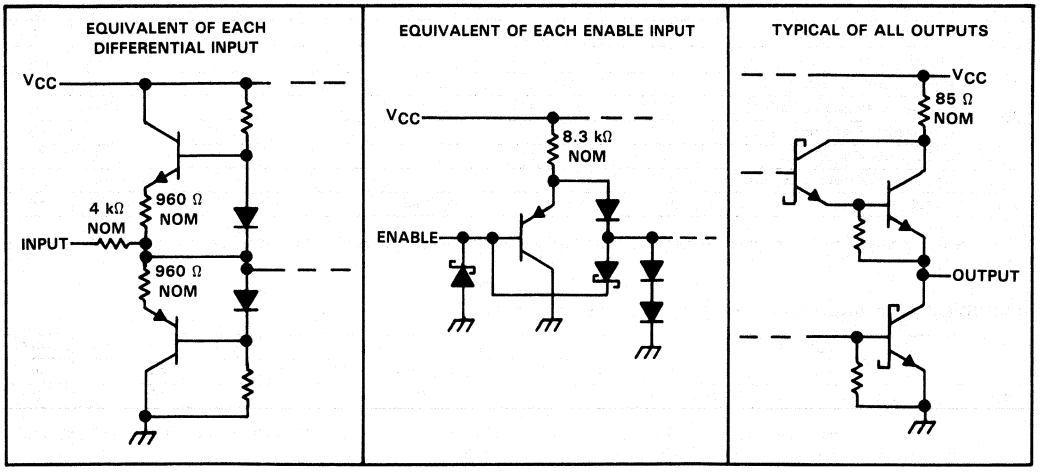
The TL712 is a high-speed comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable, OE, is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

The TL712 is characterized for operation from 0°C to 70°C.

symbol (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±15	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_T+ and V_T-)	V_{ICR} = 0 to 5 V	−100†		100	mV
V_{hys}	Hysteresis ($V_T+ - V_T-$)			5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV, I_{OH} = −1 mA	2.7	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 16 mA		0.4	0.5	V
I_{OZ}	Off-state output current	V_O = 2.4 V			−20	μA
I_I	Enable current	V_I = 5.5 V			100	μA
I_{IH}	High-level enable current	V_{IH} = 2.7 V			20	μA
I_{IL}	Low-level enable current	V_{IL} = 0.4 V			−360	μA
r_i	Differential input resistance		4			kΩ
r_o	Output resistance				100	Ω
I_{OS}	Short-circuit output current		−15		−85	mA
I_{CC}	Supply current	V_{ID} = 0, No load		17	20	mA

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	TTL load (see Figure 1),		25		ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Note 3		25		ns

NOTE 3: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total), and is the interval between the input step function and the instant when the output crosses 2.5 V.

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PARAMETER MEASUREMENT INFORMATION

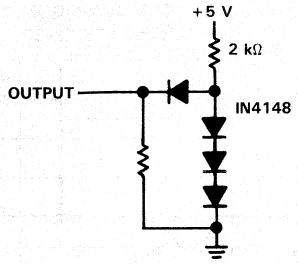

FIGURE 1. TTL OUTPUT LOAD CIRCUIT

TYPICAL CHARACTERISTICS

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

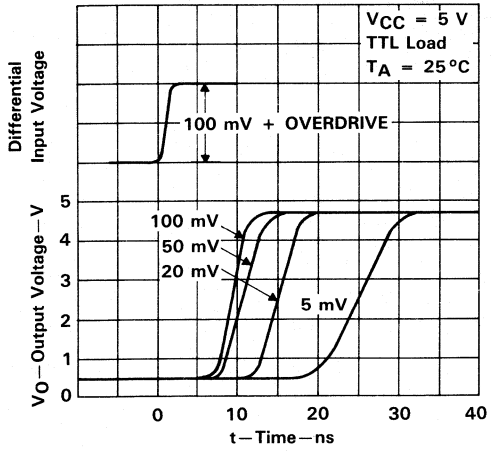

FIGURE 2

OUTPUT RESPONSE FOR VARIOUS
INPUT OVERDRIVES

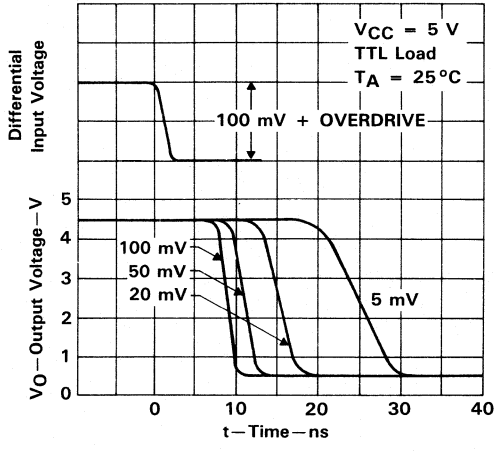

FIGURE 3

TYPICAL CHARACTERISTICS

COMMON-MODE
PULSE RESPONSE

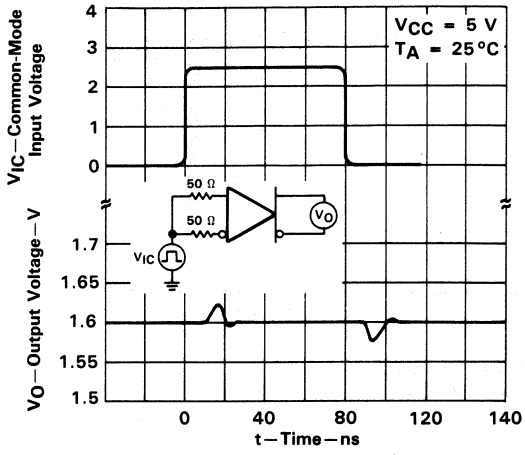

FIGURE 4

TEXAS INSTRUMENTS
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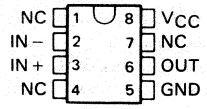
D3131, DECEMBER 1988

- **Operates from a 5-V Supply**
- **Self-Biasing Inputs**
- **Hysteresis . . . 10 mV Typical**
- **Response Time . . . 7 ns Typical**
- **Maximum Operating Frequency . . . 50 MHz Typical**

D OR P PACKAGE
(TOP VIEW)



NC—No internal connection

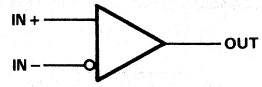
description

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

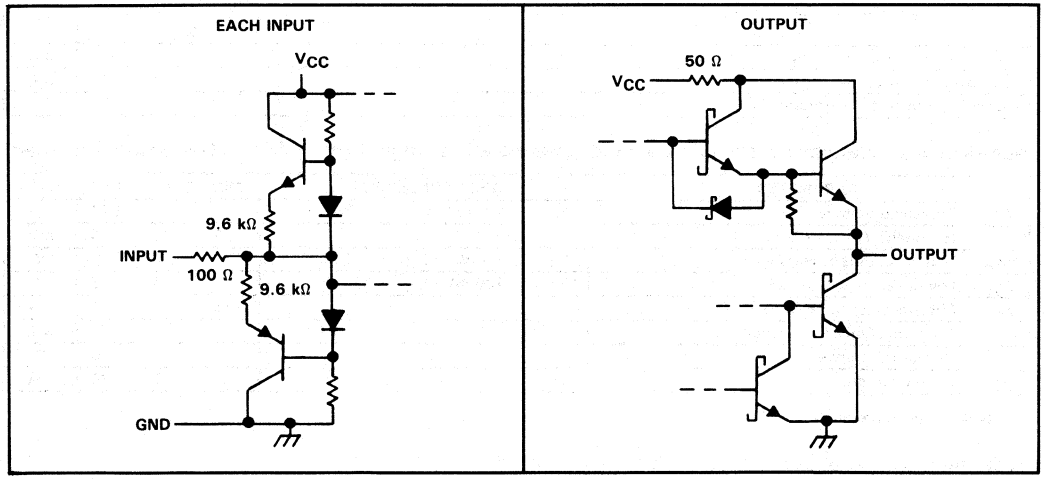
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

The TL714C is characterized for operation from 0°C to 70°C.

symbol



schematic of inputs and output



All resistor values shown are nominal.

absolute maximum ratings over oprating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Input voltage range . . . . . V_{CC} to GND
Low-level output current, I_{OL} . . . . . 40 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values, except for differential voltage, are with respect to the network ground.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW
P	500 mW	N/A	N/A	500 mW

recommended operating conditions

PARAMETER	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.75	5.25	V
Common-mode input voltage, V_{IC}	1.4 to V_{CC} −1.4		V
High-level output current, I_{OH}		−1	mA
Low-level output current, I_{OL}		16	mA
Operating free-air temperature, T_A	0	70	°C

electrical characteristics over free-air operating temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_T	Threshold voltage	V_{IC} = 1.4 V to 3.6 V			±20	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)		2	10	20	mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV, I_{OH} = −1 mA	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 16 mA		0.4	0.5	V
I_{OS}	Short-circuit output current		−15		−85	mA
r_i	Differential input resistance		2.9			kΩ
r_o	Output resistance				100	Ω
I_{CC}	Supply current	V_{ID} = 0, I_O = 0		7	20	mA

†All typical values are at T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum operating frequency	V_{ID} = ±250 mV, $t_r = t_f$ = 4 ns, C_L = 25 pF, Input duty cycle = 50%		50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = ±100 mV, C_L = 25 pF, See Figures 1 and 2		7	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			7	25	ns
t_r	Rise time	V_{ID} = ±100 mV, C_L = 25 pF, See Figure 3		4	8	ns
t_f	Fall time			4	8	ns

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PARAMETER MEASUREMENT INFORMATION

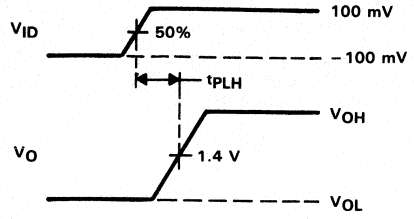


FIGURE 1. PROPAGATION DELAY TIME, LOW TO HIGH (t_{PLH})

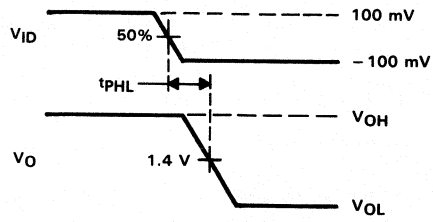


FIGURE 2. PROPAGATION DELAY TIME, HIGH TO LOW (t_{PHL})

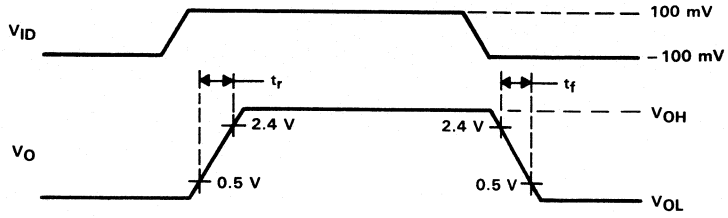
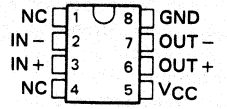


FIGURE 3. RISE AND FALL TIMES (t_r, t_f)

D2781, FEBRUARY 1984—REVISED OCTOBER 1988

- **Operates from a −5.2-V Power Supply**
- **Self-Biased Inputs**
- **Common-Mode Input Voltage Range 0 V to −5.2 V**
- **MECL III and MECL 10 000 Compatible**
- **Complementary ECL-Compatible Outputs**
- **Hysteresis . . . 5 mV Typ**
- **Response Times . . . 10 ns Typ**

D, JG, OR P PACKAGE
(TOP VIEW)



NC—No internal connection

symbol

description

The TL721 is a high-speed voltage comparator fabricated with bipolar Schottky† process technology. The circuit has differential analog inputs and complementary ECL-compatible logic outputs with symmetrical switching characteristics. The device operates from a single −5.2-volt supply and is useful as a disk memory read-chain data comparator.

The TL721 is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . −7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Low-level output current . . . . . 50 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		−5.2		V
Common-mode input voltage, V_{IC}			±7	V
High-level output current, I_{OH}			−1	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

3 Voltage Comparators

electrical characteristics at T_A = 25°C, V_{CC} = −5.2 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Threshold voltage (V_T+ and V_T-)	V_{IC} = V_{ICR} min		−100†		100	mV
V_{hys}	Hysteresis ($V_T+ - V_T-$)				5		mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	R_L = 50 Ω to −2 V	−0.96†		−0.81	V
V_{OL}	Low-level output voltage	V_{ID} = −100 mV,	R_L = 50 Ω to −2 V	−1.85†		−1.65	V
V_{ICR}	Common-mode input voltage range			0 to −5.2			V
r_{in}	Input resistance			4			kΩ
I_{CC}	Supply current	V_{ID} = 0,	No load		−13	−17	mA

† The algebraic convention, in which the more negative limit is designated as minimum, is used in this data sheet for input threshold and output voltage levels only.

switching characteristics at T_A = 25°C, V_{CC} = −5.2 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_{ID} = +200 mV to −200 mV or −200 mV to +200 mV, R_L = 50 Ω to −2 V		18		ns
t_{PHL}	Propagation delay time, high-to-low-level output			18		ns

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TYPICAL CHARACTERISTICS

OUTPUT RESPONSES FOR VARIOUS
INPUT OVERDRIVES

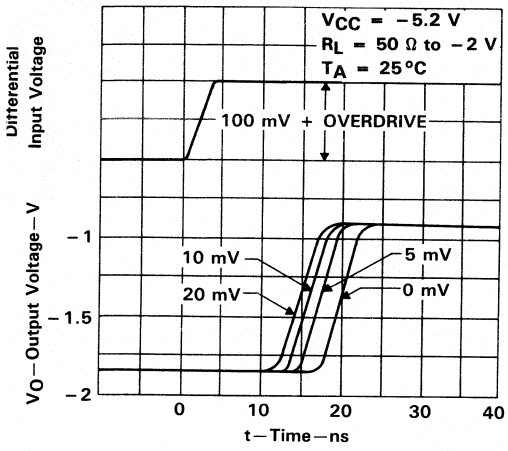


FIGURE 1

OUTPUT RESPONSES FOR VARIOUS
INPUT OVERDRIVES

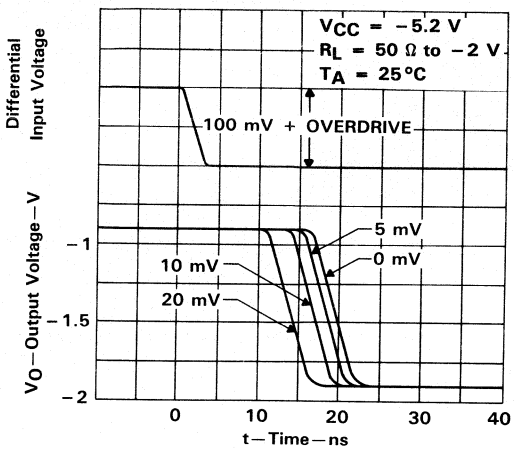


FIGURE 2

COMMON-MODE
PULSE RESPONSE

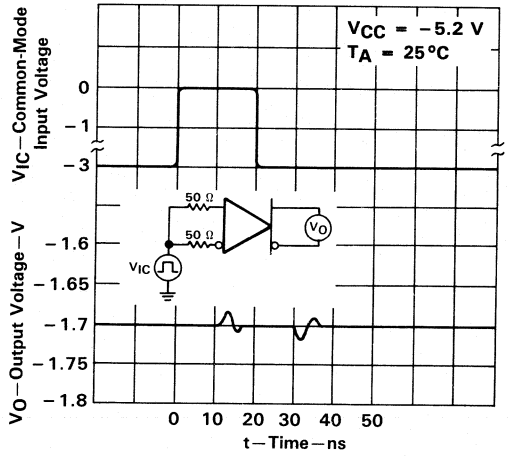
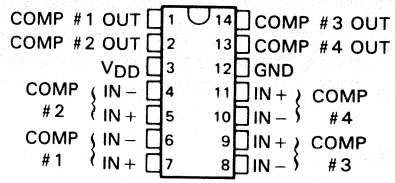


FIGURE 3

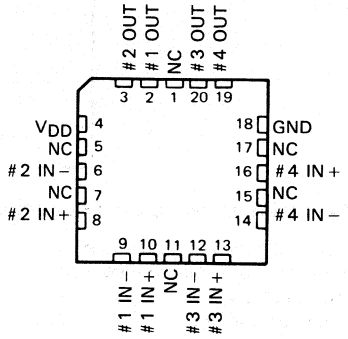
D3135, DECEMBER 1986—REVISED FEBRUARY 1989

- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive**
- **Single Supply Operation:**
  TLC339M . . . 4 V to 16 V
  TLC339I . . . 3 V to 16 V
  TLC339C . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

TLC339M . . . J PACKAGE
TLC339I, TLC339C . . . D, J, OR N PACKAGE
(TOP VIEW)



TLC339M . . . FK PACKAGE
(TOP VIEW)



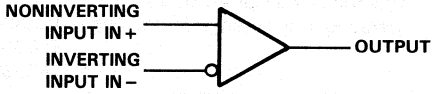
NC—No internal connection

description

The TLC339 consists of four independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3704 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC339CD	—	TLC339CJ	TLC339CN
−40°C to 85°C	5 mV	TLC339ID	—	TLC339IJ	TLC339IN
−55°C to 125°C	5 mV	—	TLC339MFK	TLC339MJ	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., TLC339CDR)

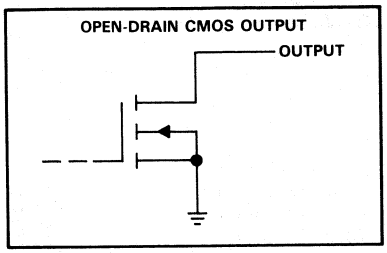
inCMOS is a trademark of Texas Instruments Incorporated.

description (continued)

currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC339M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC339I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC339C is characterized for operation over the commercial temperature range of 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . −0.3 V to V_{DD}
Output voltage, V_O . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . 20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 60 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC339M . . . . . −55°C to 125°C
TLC339I . . . . . −40°C to 85°C
TLC339C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC339M)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC339I & C)	1025 mW	8.2 mW/°C	656 mW	533 mW	–
N	1150 mW	9.2 mW/°C	736 mW	598 mW	–

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ecommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

lectrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise oted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			−55°C to 125°C			175	

All characteristics are measured with zero common-mode voltage unless otherwise noted.

OTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD}−1.5	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}−1			V
			−40°C to 85°C	0 to V_{DD}−1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			−40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			−40°C to 85°C			125	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}		8	20	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	µA
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		44	80	µA
			0°C to 70°C			100	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

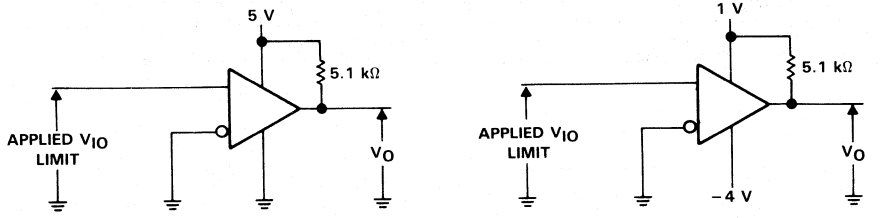
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.5		
			Overdrive = 10 mV		1.7		
			Overdrive = 20 mV		1.2		
			Overdrive = 40 mV		1.0		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{PHL}	Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
			Overdrive = 5 mV		2.1		
			Overdrive = 10 mV		1.3		
			Overdrive = 20 mV		0.85		
			Overdrive = 40 mV		0.55		
		V_I = 1.4 V step at IN+ pin			0.10		
t_{THL}	Transition time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

PARAMETER MEASUREMENT INFORMATION

The TLC339 contains a digital output stage that, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} with V_{IC} = 0 V (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching mode servo loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

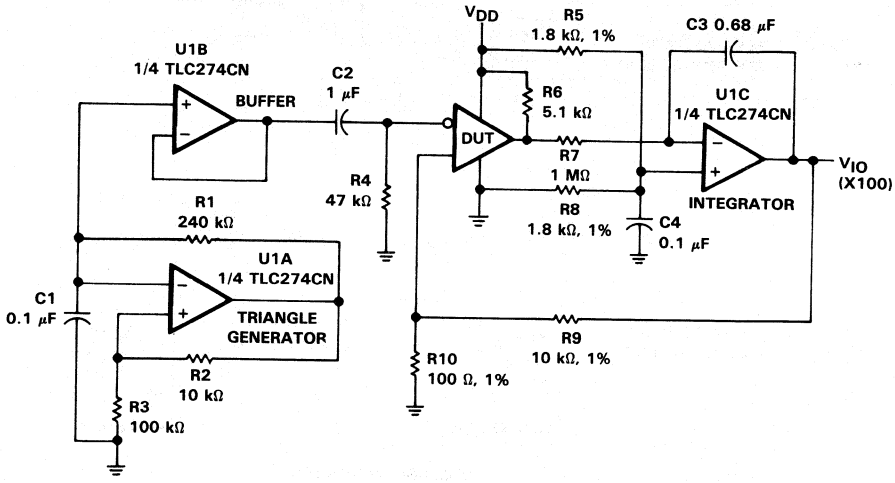
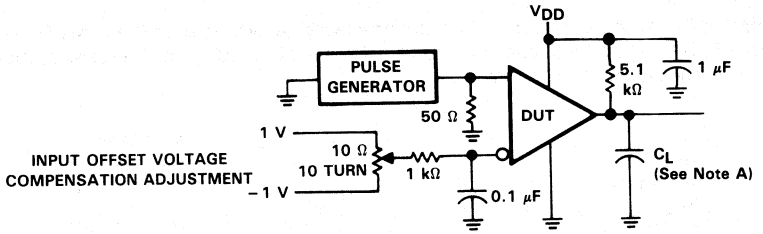


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

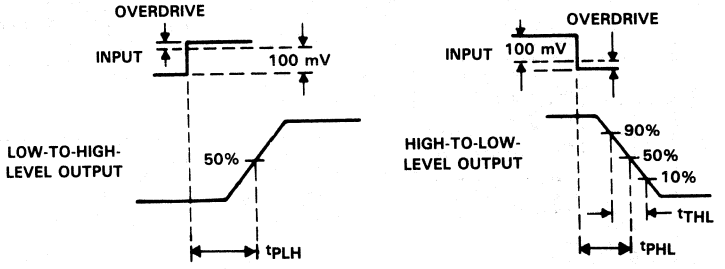
Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. PROPAGATION DELAY, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

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TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

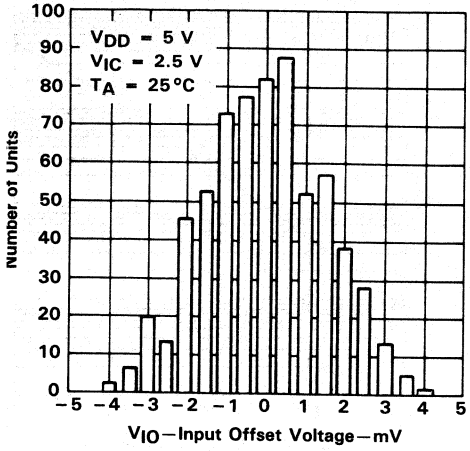

FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

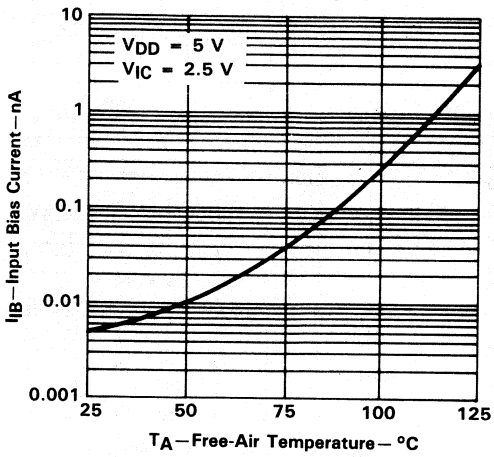

FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

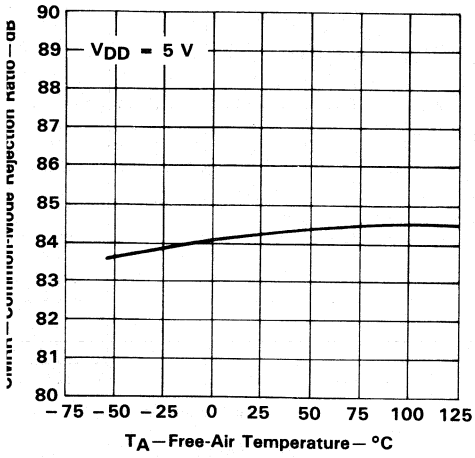

FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

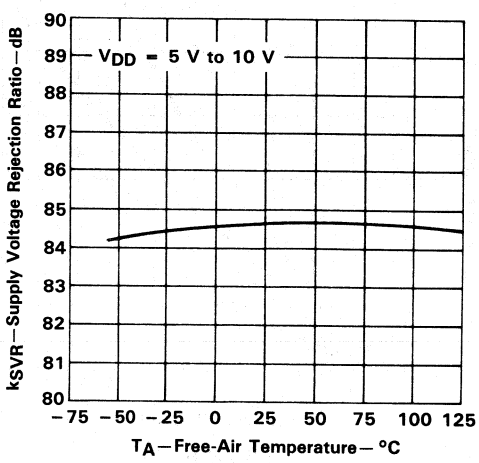

FIGURE 7

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

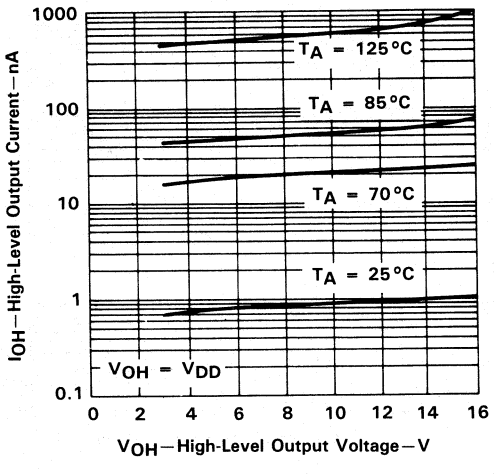

FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

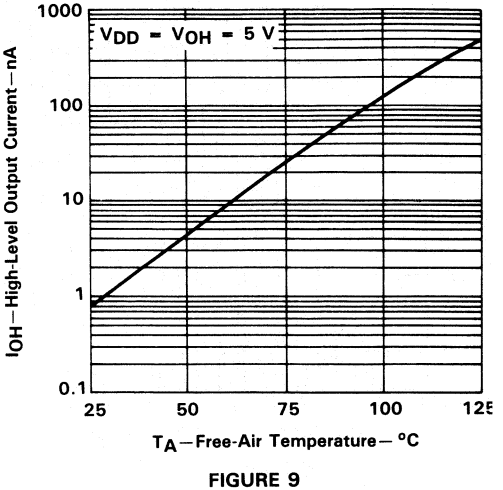

FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

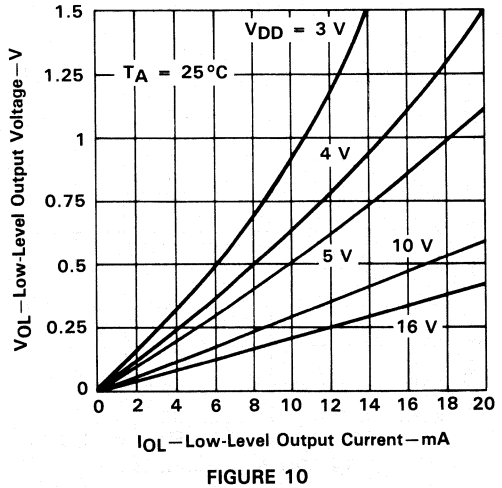

FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

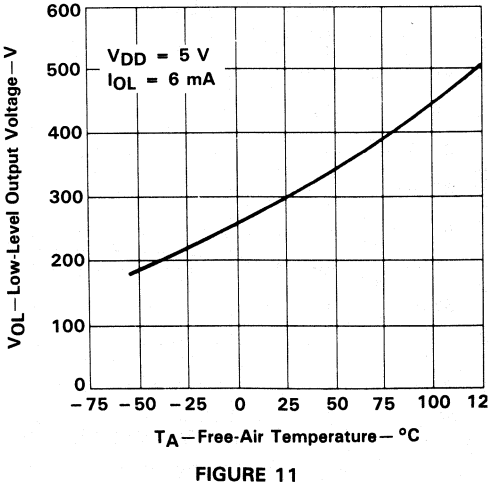

FIGURE 11

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

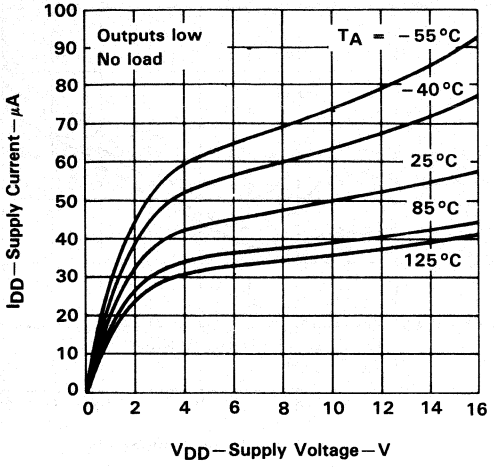

FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

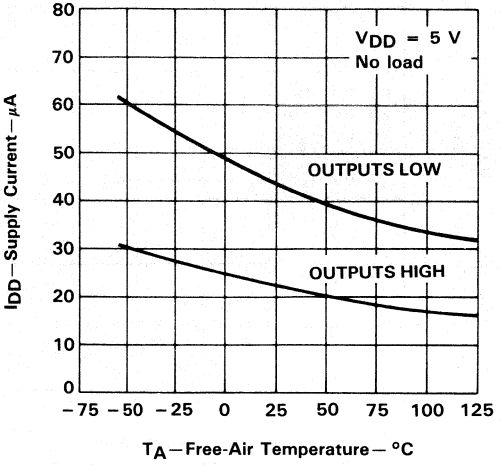

FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

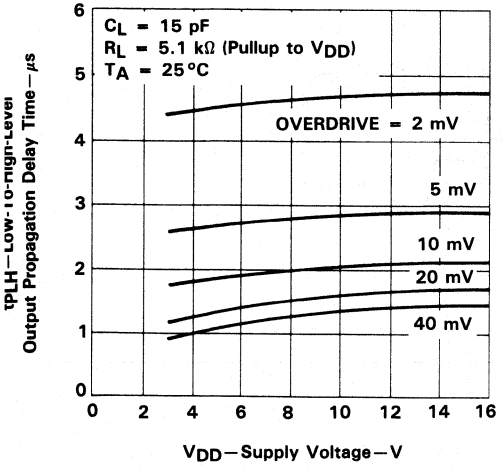

FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

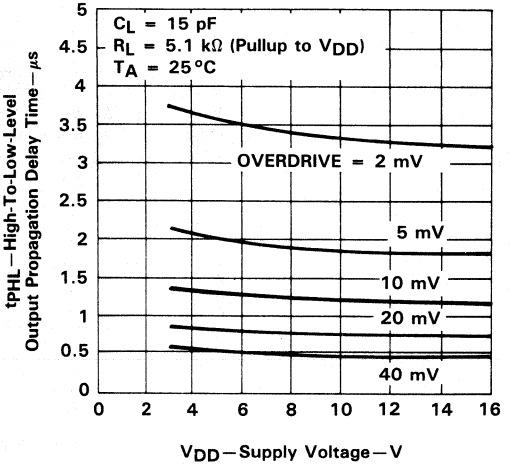

FIGURE 15

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

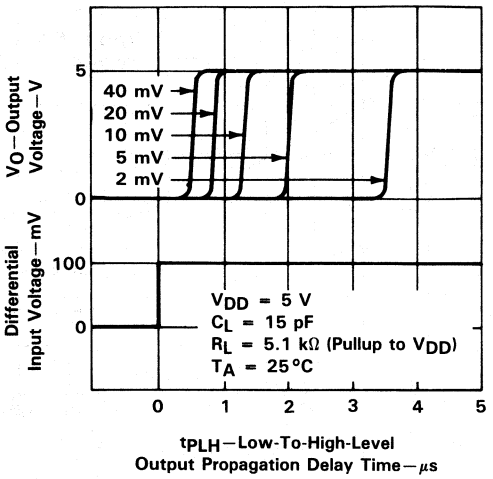

FIGURE 16

OUTPUT FALL TIME
vs
SUPPLY VOLTAGE

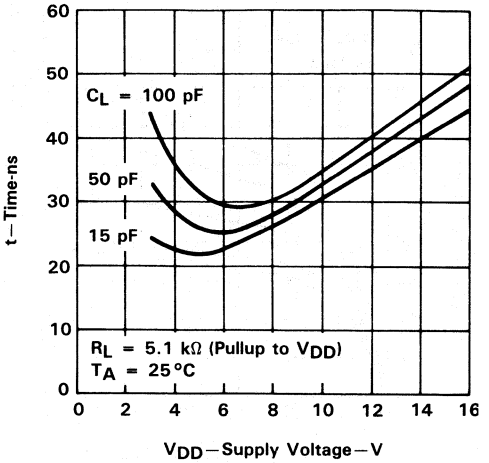

FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

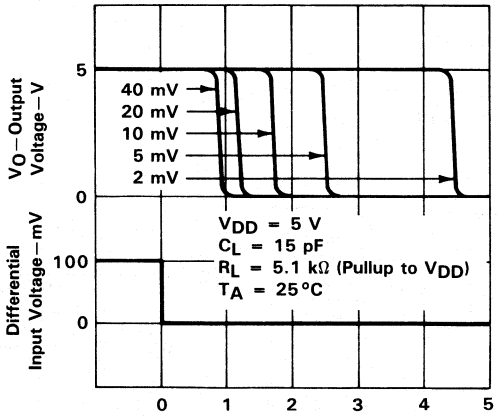

FIGURE 18

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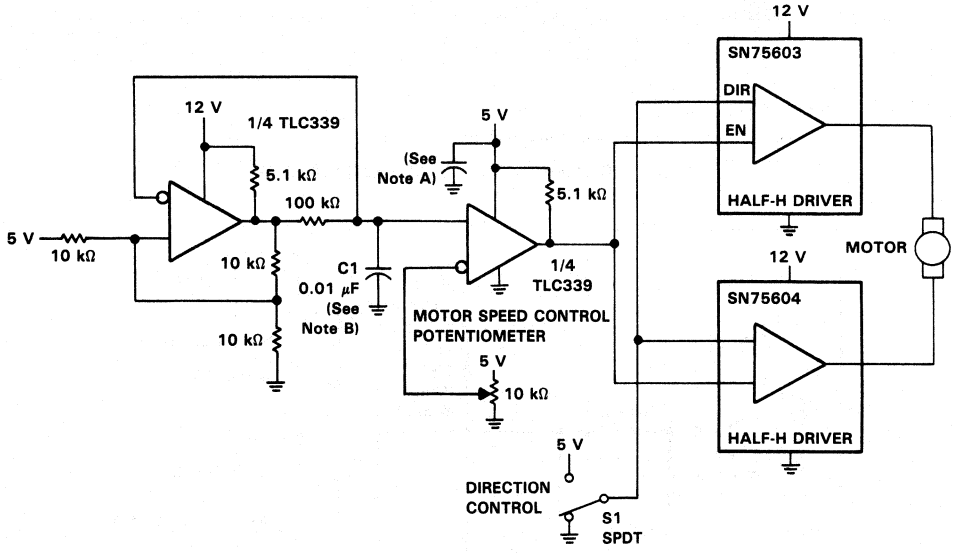
TYPICAL APPLICATION DATA

The inputs should always remain within the supply rails in order to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not be damaged as long as the input current is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with V_{DD} = 5 V, both inputs must remain between −0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close to the device as possible.

Be careful to note the output and supply current limitations since the TLC339 does not provide current protection. For example, each output can source or sink a maximum of 20 mA; however, the total current to ground can only be an absolute maximum of 60 mA. This prohibits sinking 20 mA from each of the four outputs simultaneously since the total current to ground would be 80 mA.

The TLC339 has internal ESD protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

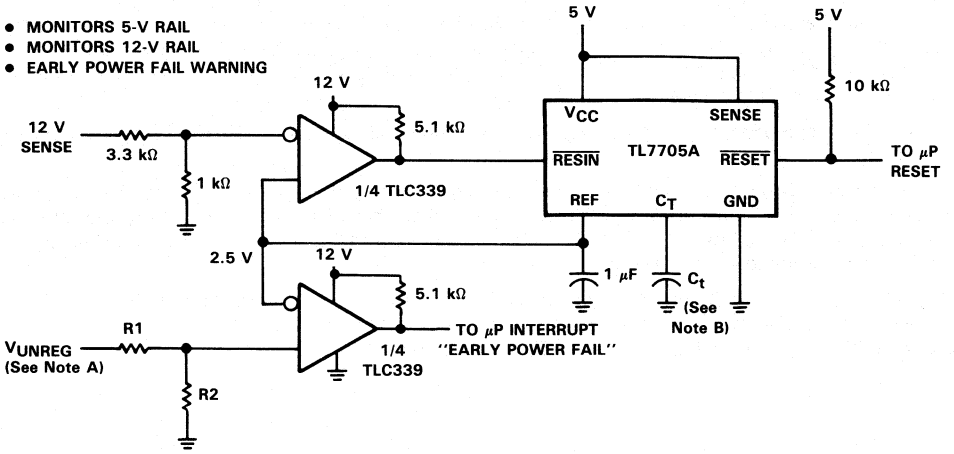


NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA

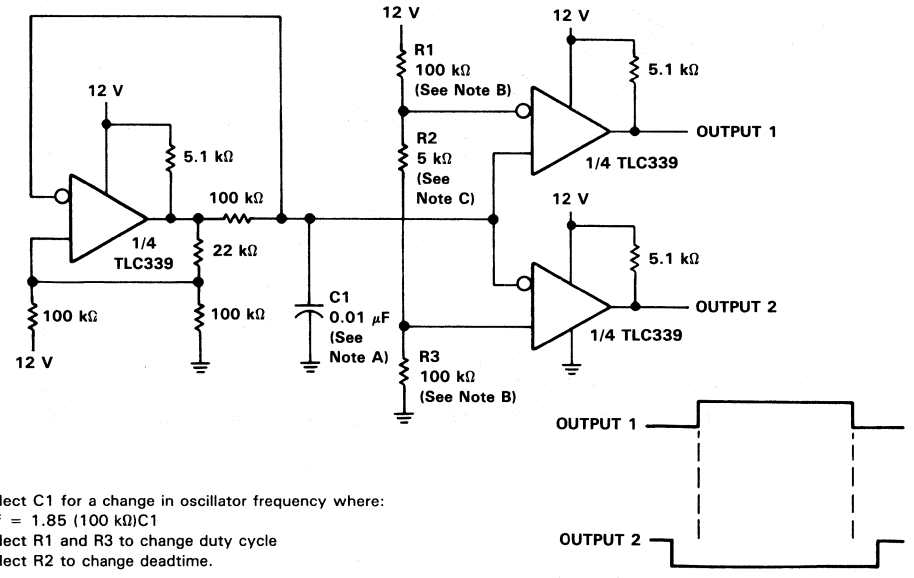
- MONITORS 5-V RAIL
- MONITORS 12-V RAIL
- EARLY POWER FAIL WARNING



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 20. ENHANCED SUPPLY SUPERVISOR



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$

B. Select R1 and R3 to change duty cycle

C. Select R2 to change deadtime.

FIGURE 21. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

TEXAS INSTRUMENTS
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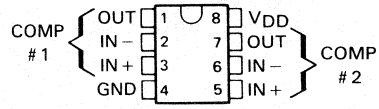
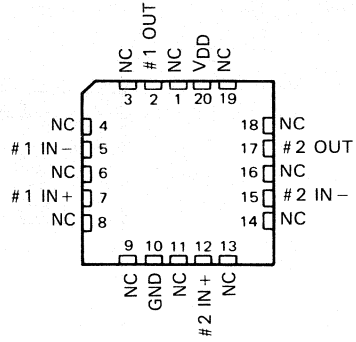
D2901, SEPTEMBER 1985—REVISED FEBRUARY 1989

- **Single- or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 1.4 V to 18 V**
- **Very Low Supply Current Drain**
  150 μA Typ at 5 V
  65 μA Typ at 1.4 V
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM393**

TLC352M . . . JG PACKAGE
TLC352I, TLC352C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TLC352M . . . FK PACKAGE
(TOP VIEW)

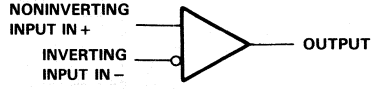


NC—No internal connection

description

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC352 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

symbol (each comparator)

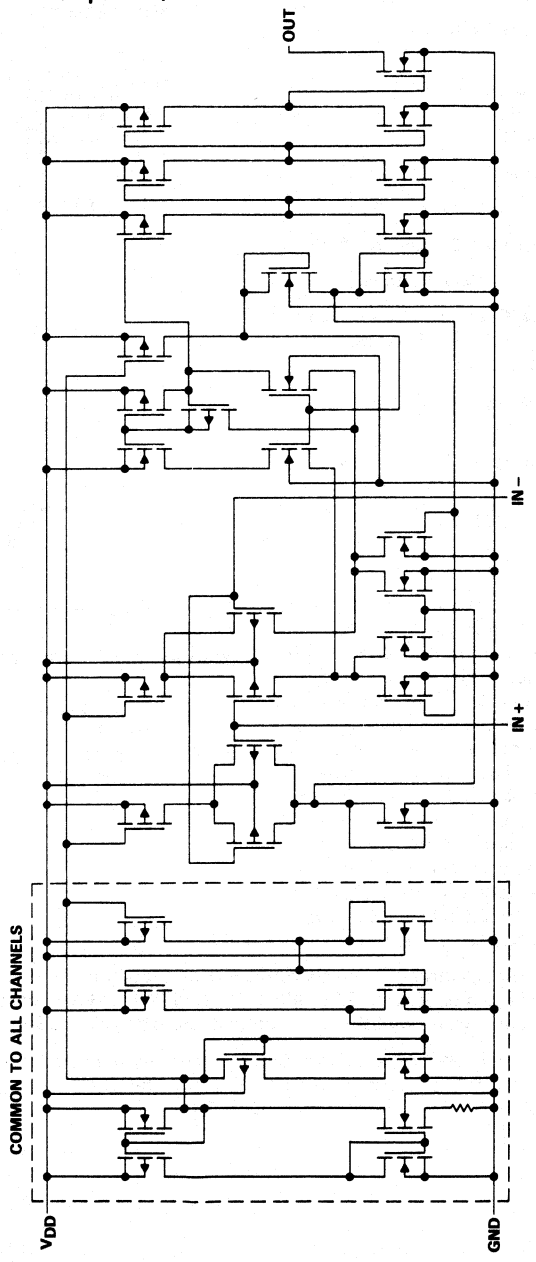


The TLC352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC352M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC352I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC352C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC352CD	–	TLC352CJG	TLC352CP
−40°C to 85°C	5 mV	TLC352ID	–	TLC352IJG	TLC352IP
−55°C to 125°C	5 mV	–	TLC352MFK	TLC352MJG	–

D packages are availabe taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC352CDR).

ıbsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC352M . . . . . −55°C to 125°C
TLC352I . . . . . −40°C to 85°C
TLC352C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

ıOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG (TLC352M)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (TLC352I, TLC352C)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TLC352M			TLC352I			TLC352C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4	25°C		2	5		2	5		2	5	mV
			Full range			10			7			6.5	
I_{IO}	Input offset current		25°C		1			1			1		pA
			MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current		25°C		5			5			5		pA
			MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range		Full range	0 to 0.2			0 to 0.2			0 to 0.2			V
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V, I_{OL} = 0.6 mA	25°C		100	200		100	200		100	200	mV
			Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5 V, V_{OL} = 0.3 V	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (two comparators)	V_{DD} = 0.5 V, No load	25°C		65	150		65	150		65	150	μA
			Full range			200			200			200	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC352M, 0°C to 70°C for TLC352C, and −40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC352M			TLC352I			TLC352C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 5		25°C		1	5		1	5		1	5	mV
				Full range			10			7			6.5	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{DD} = 1 V,	No load	25°C		0.15	0.3		0.15	0.3		0.15	0.3	μA
				Full range			0.4			0.4			0.4	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC352M, 0°C to 70°C for TLC352C, and −40°C to 85°C for TLC352I. IMPORTANT: See Parameter Measurement Information.

NOTE 5: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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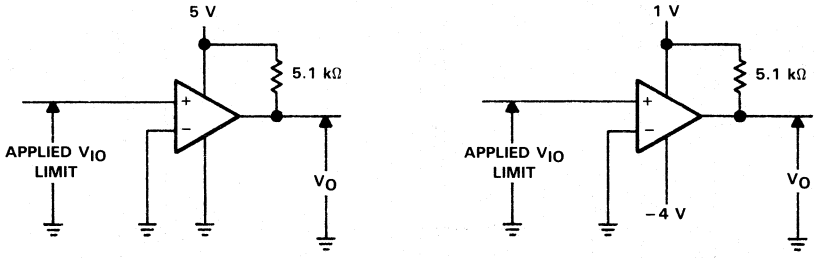
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC352 can be damaged if it is held in the linear region of the transfe curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that i designed to force the device output to a level within this linear region. Since the servo-loop method o testing cannot be used, the following alternative for measuring parameters such as input offset voltage common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the inpu as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the outpu should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The suppl voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method t vary the differential input voltage while monitoring the output state. When the applied input voltag differential is equal, but opposite in polarity, to the input offset voltage, the output will change states



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

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PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

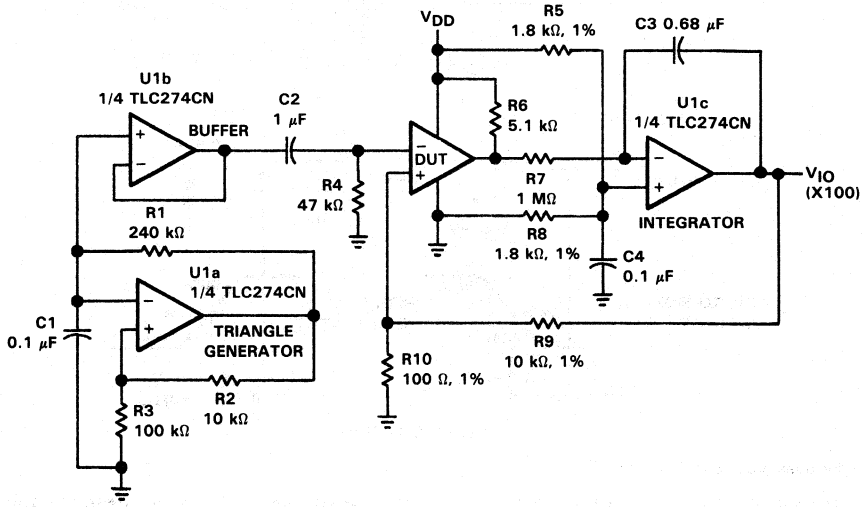
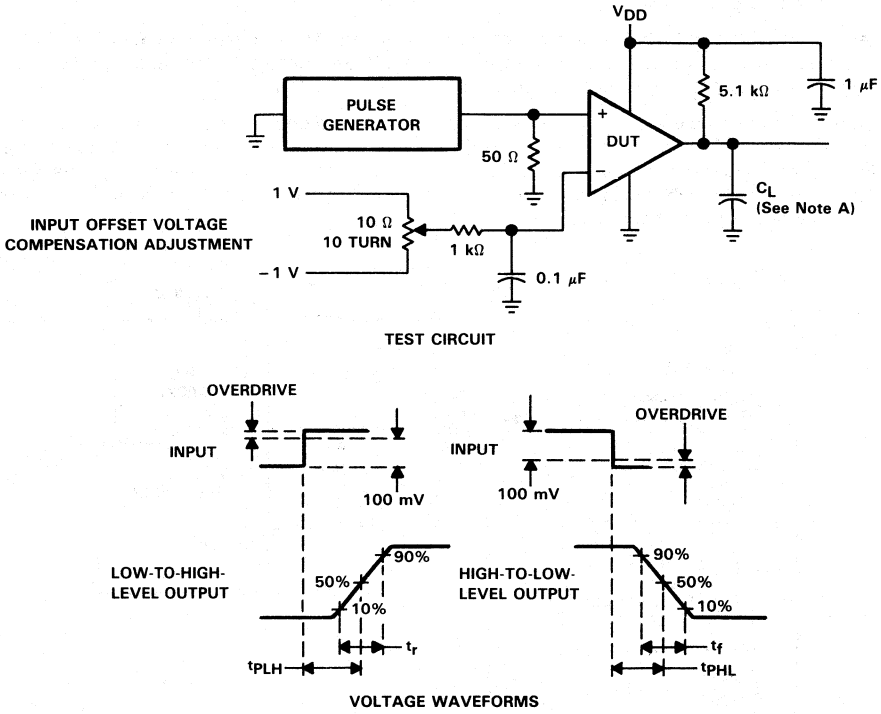


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instar when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measure from the leading edge of the input pulse, while response time, high-to-low-level output, is measured fror the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatl affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the invertin input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for exampl 105-mV or 5-mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

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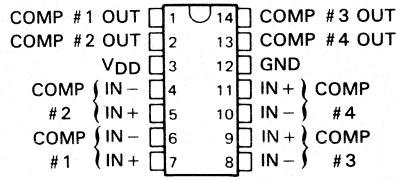
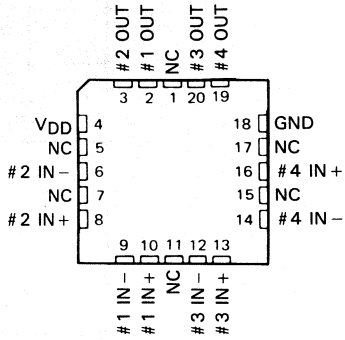
- Single- or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 1.4 V to 18 V
- Very Low Supply Current Drain
  300 μA Typ at 5 V
  130 μA Typ at 1.4 V
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM339

TLC354M . . . J PACKAGE
TLC354I, TLC354C . . . D OR N PACKAGE
(TOP VIEW)

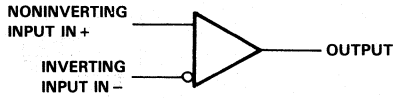


TLC354M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each comparator)



description

This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators; each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 1.4 V to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interface to high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships. The capability of the TLC354 to operate from a 1.4-V supply makes this device ideal for low-voltage battery applications.

The TLC354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

The TLC354M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC354I is characterized for operation over the industrial temperature range of −40°C to 85°C. The TLC354C is characterized for operation from 0°C to 70°C.

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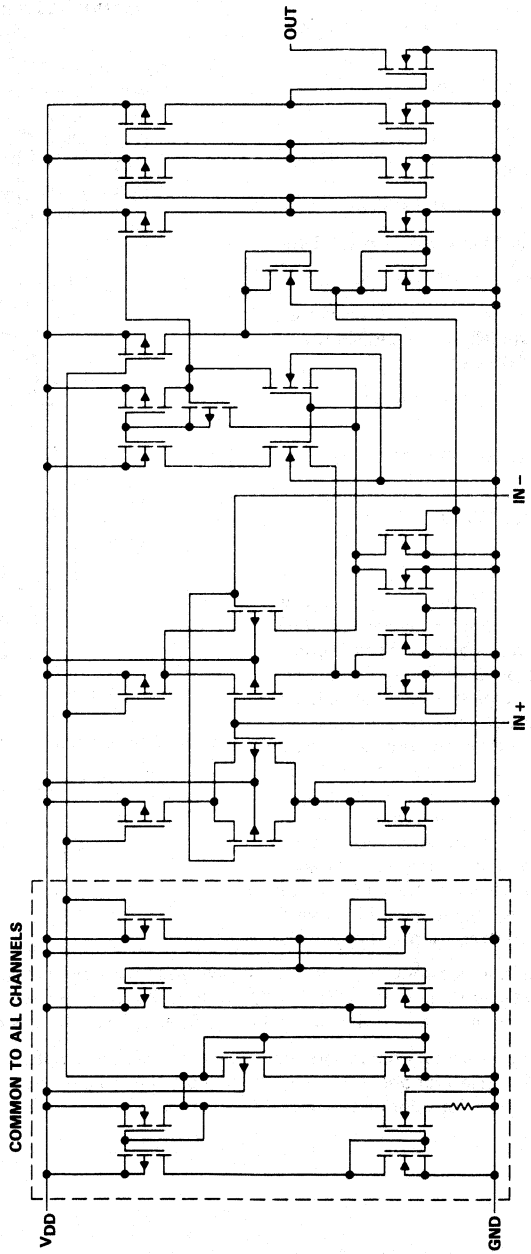
equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC354CD	–	TLC354CJ	TLC354CN
−40°C to 85°C	5 mV	TLC354ID	–	TLC354IJ	TLC354IN
−55°C to 125°C	5 mV	–	TLC354MFK	TLC354MJ	–

D packages are availabe taped and reeled. Add "R" suffix to device type when ordering (e.g., TLC354CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC354M . . . . . −55°C to 125°C
TLC354I . . . . . −40°C to 85°C
TLC354C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	500 mW	494 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC354M)	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC354I, TLC354C)	500 mW	N/A	N/A	500 mW	500 mW	N/A
N	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		1.4		16	1.4		16	1.4		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 1.4 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC354M			TLC354I			TLC354C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		2	5		2	5		2	5	mV
				Full range			10			7			6.5	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to 0.2			0 to 0.2			0 to 0.2			V
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −0.5 V,	I_{OL} = 0.6 mA	25°C		100	200		100	200		100	200	mV
				Full range			200			200			200	
I_{OL}	Low-level output current	V_{ID} = −0.5 V,	V_{OL} = 300 mV	25°C	1	1.6		1	1.6		1	1.6		mA
I_{DD}	Supply current (four comparators)	V_{DD} = 0.5 V,	No load	25°C		130	300		130	300		130	300	μA
				Full range			400			400			400	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC354M, −40°C to 85°C for TLC354I, and 0°C to 70°C for TLC354C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 1.25 V or below 150 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

...temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC354M			TLC354I			TLC354C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 4		25°C		2	10		2	10		2	10	mV
				Full range			12			13			12	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to $V_{DD}-1$			0 to $V_{DD}-1$			0 to $V_{DD}-1$			V
				Full range	0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			0 to $V_{DD}-1.5$			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{DD} = 1 V,	No load	25°C		0.3	0.6		0.3	0.6		0.3	0.6	μA
				Full range			0.8			0.8			0.8	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC354M, −40°C to 85°C for TLC354I, and 0°C to 70°C for TLC354C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC354 can be damaged if it is held in the linear region of the transfe curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that i designed to force the device output to a level within this linear region. Since the servo-loop method o testing cannot be used, the following alternative for measuring parameters such as input offset voltage common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the inpu as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the outpu should be high. With the input polarity reversed, the output should be low.

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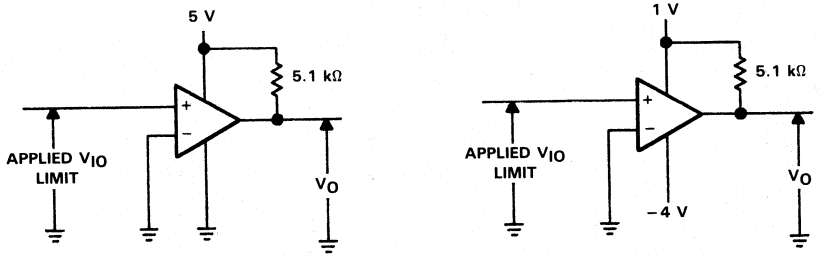

(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

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PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

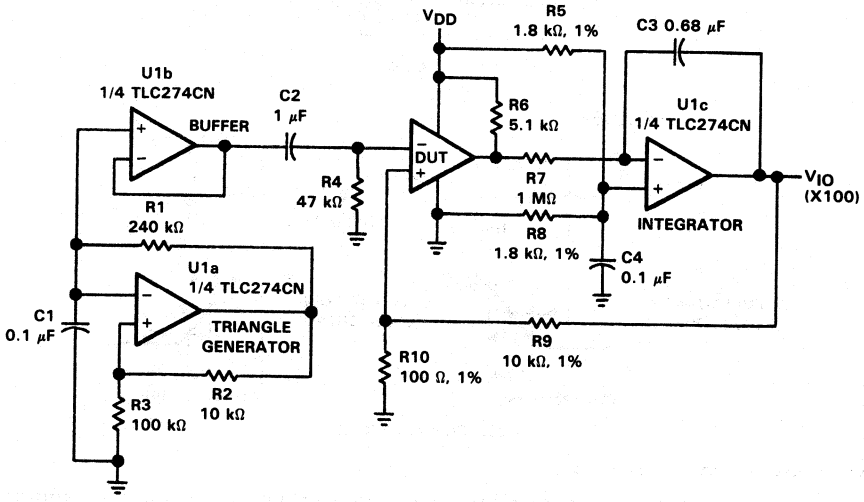
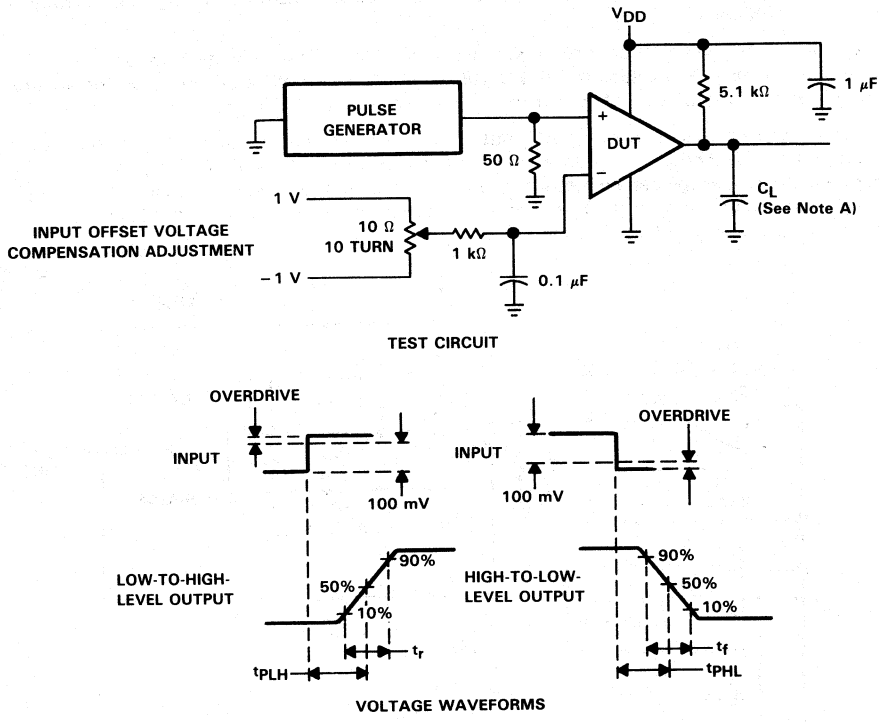


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instan when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measure from the leading edge of the input pulse, while response time, high-to-low-level output, is measured fron the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatl affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the invertin input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for exampl 105-mV or 5-mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

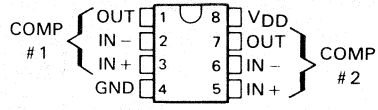
FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

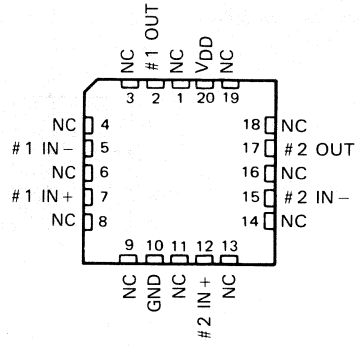
D2821, NOVEMBER 1983—REVISED SEPTEMBER 1988

- Single or Dual-Supply Operation
- Wide Range of Supply Voltages . . . 2 V to 18 V
- Very Low Supply Current Drain 150 μA Typ at 5 V
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- Built-In ESD Protection
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current 5 pA Typ
- Ultrastable Low Input Offset Voltage
- Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days
- Common-Mode Input Voltage Range Includes Ground
- Outputs Compatible with TTL, MOS, and CMOS
- Pin-Compatible with LM393

TLC372M . . . JG PACKAGE
TLC372I, TLC372C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TLC372M . . . FK PACKAGE
(TOP VIEW)

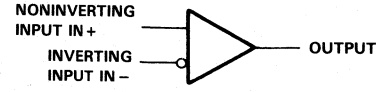


NC—No internal connection

escription

This device is fabricated using LinCMOS™ technology and consists of two independent voltage comparators each designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

symbol (each comparator)



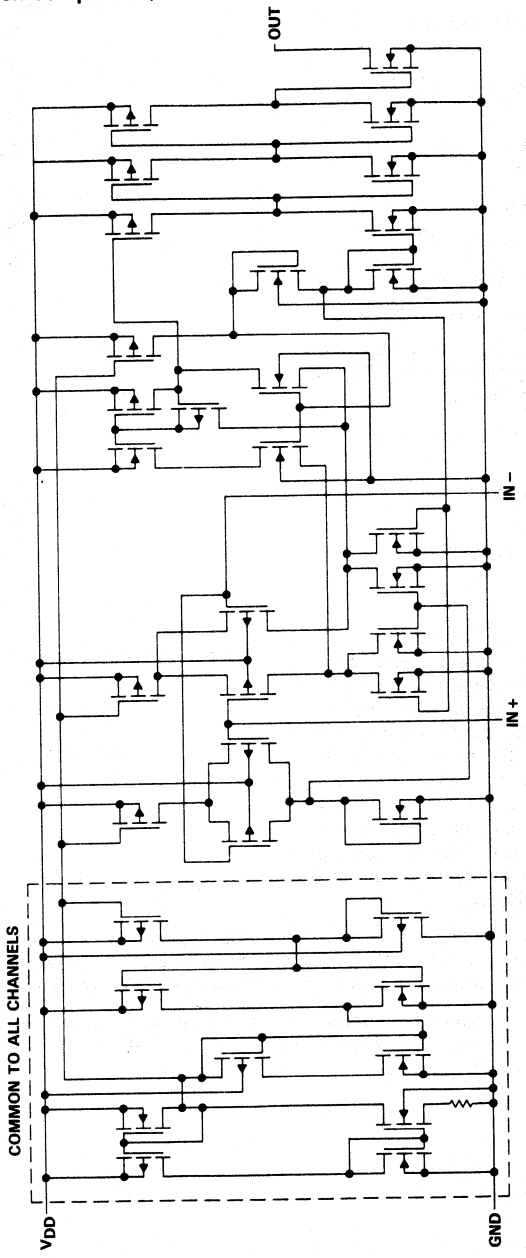
The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372I is characterized for operation from −40°C to 85°C. The TLC372C is characterized for operation from 0°C to 70°C.

3 Voltage Comparators

iCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC372CD	–	TLC372CJG	TLC372CP
−40°C to 85°C	5 mV	TLC372ID	–	TLC372IJG	TLC372IP
−55°C to 125°C	5 mV	–	TLC372MFK	TLC372MJG	–

D packages are availabe taped and reeled. Add "R" suffix to device type (e.g., TLC372CDR).

bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC372M . . . . . −55°C to 125°C
TLC372I . . . . . −40°C to 85°C
TLC372C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or P package . . . . . 260°C

OTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
JG (TLC372M)	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
JG (TLC372I, TLC372C)	500 mW	6.6 mW/°C	74°C	500 mW	429 mW	N/A
P	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC372M			TLC372I			TLC372C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			10			7			6.5	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD}−1			0 to V_{DD}−1			0 to V_{DD}−1			V
				Full range	0 to V_{DD}−1.5			0 to V_{DD}−1.5			0 to V_{DD}−1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			3			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1 V,	No load	25°C		150	300		150	300		150	300	µA
				Full range			400			400			400	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC372M, 0°C to 70°C for TLC372C, and −40°C to 85°C for TLC372I. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

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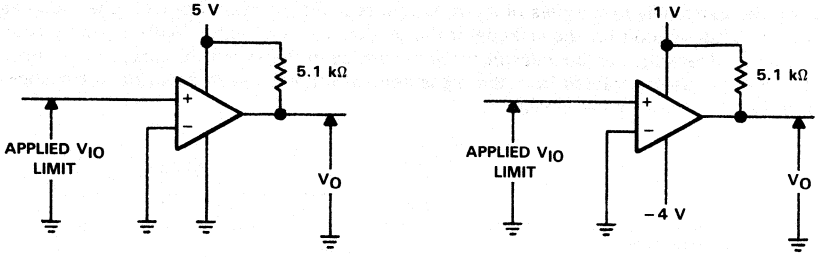
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC372 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is ''sliced'' symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

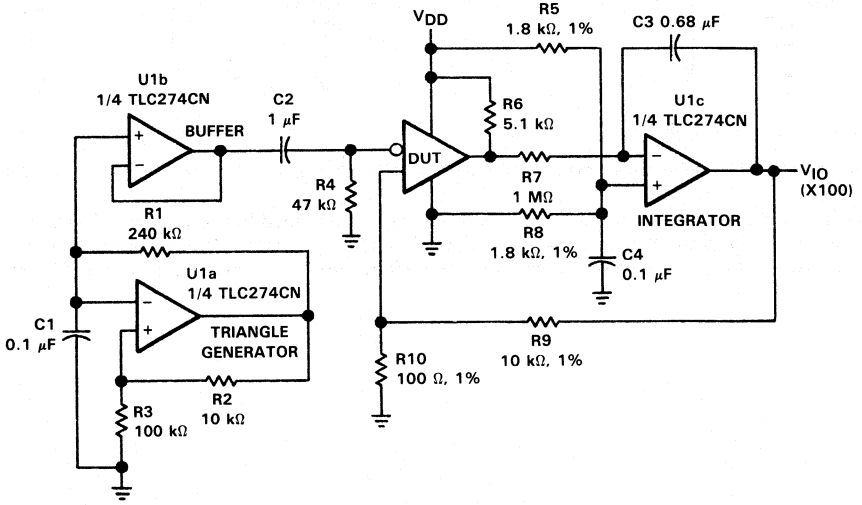


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

TEXAS INSTRUMENTS
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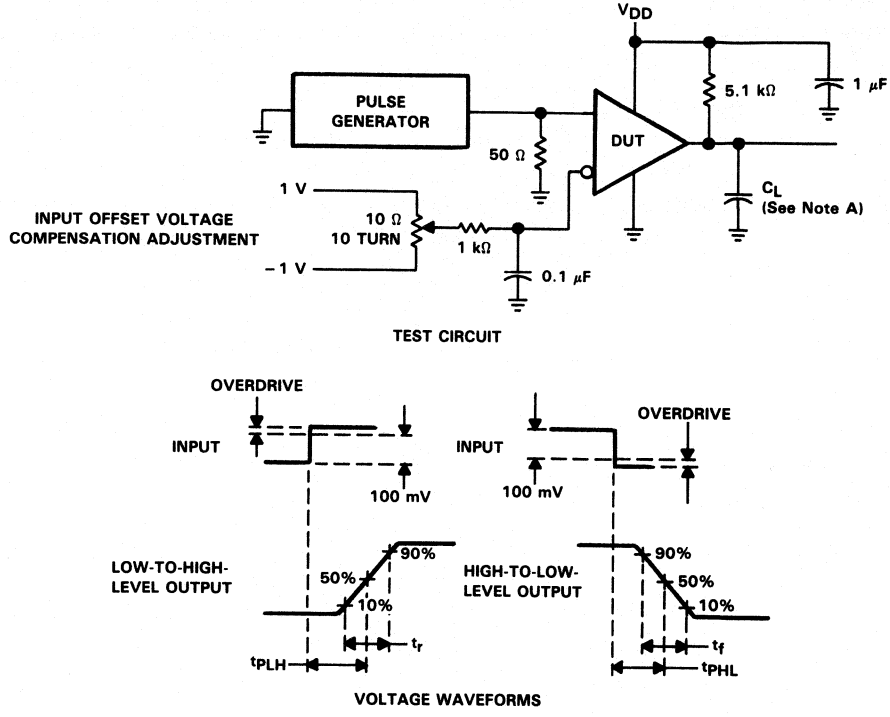
PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



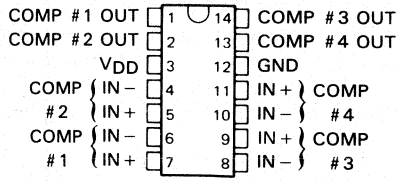
NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

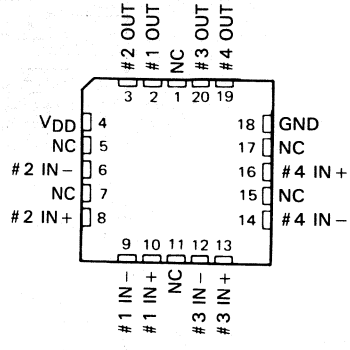
D2783, NOVEMBER 1983—REVISED SEPTEMBER 1988

- **Single or Dual-Supply Operation**
- **Wide Range of Supply Voltages . . . 2 V to 18 V**
- **Very Low Supply Current Drain 0.3 mA Typ at 5 V**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **Built-In ESD Protection**
- **High Input Impedance . . . 10^{12} Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Ultrastable Low Input Offset Voltage**
- **Input Offset Voltage Change at Worst-Case Input Conditions Typically 0.23 μV/Month, Including the First 30 Days**
- **Common-Mode Input Voltage Range Includes Ground**
- **Outputs Compatible with TTL, MOS, and CMOS**
- **Pin-Compatible with LM339**

TLC374M . . . J PACKAGE
TLC374I, TLC374C . . . D, J, OR N PACKAGE
(TOP VIEW)

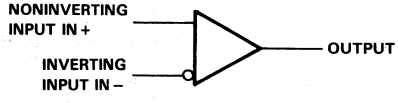


TLC374M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

symbol (each comparator)



description

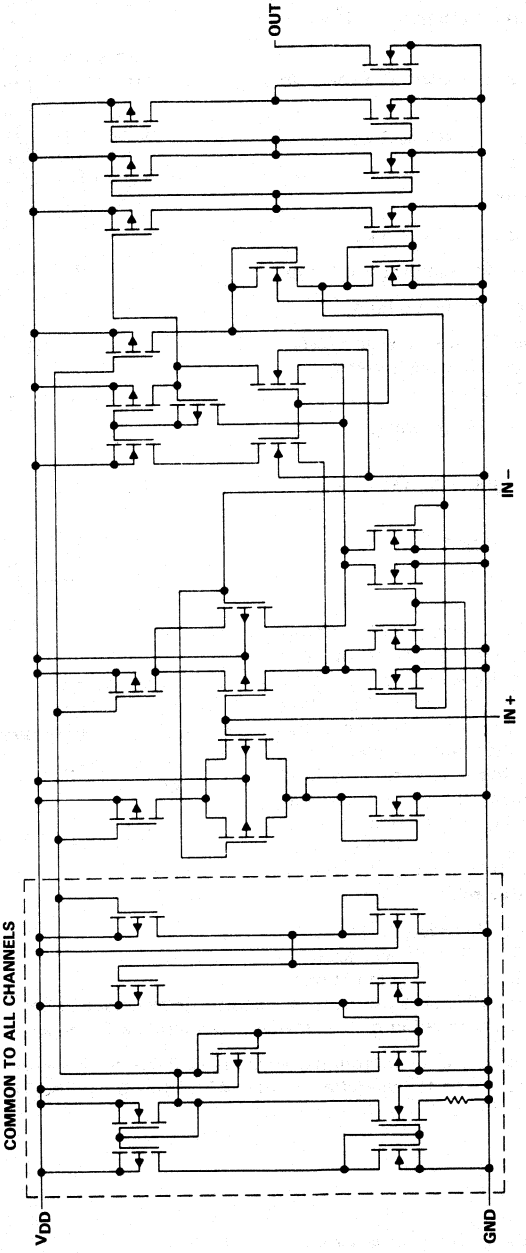
This device is fabricated using LinCMOS™ technology and consists of four independent voltage comparators designed to operate from a single power supply. Operation from dual supplies is also possible so long as the difference between the two supplies is 2 to 18 V. Each device features extremely high input impedance (typically greater than 10^{12} Ω) allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations, and can be connected to achieve positive-logic wired-AND relationships.

The TLC374 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC374M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC374I is characterized for operation from −40°C to 85°C. The TLC374C is characterized for operation from 0°C to 70°C.

nCMOS is a trademark of Texas Instruments Incorporated.

equivalent schematic (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE			
		SMALL-OUTLINE (D)	CHIP-CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC374CD	–	TLC374CJ	TLC374CN
−40°C to 85°C	5 mV	TLC374ID	–	TLC374IJ	TLC374IN
−55°C to 125°C	5 mV	–	TLC374MFK	TLC374MJ	–

D packages are available taped and reeled. Add "R" suffix to device type (e.g., TLC374CDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . V_{DD}
Input voltage range . . . . . −0.3 V to 18 V
Output voltage, V_O . . . . . 18 V
Input current, I_I . . . . . ±5 mA
Output current, I_O . . . . . 20 mA
Duration of output short-circuit to ground (see Note 3) . . . . . unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC374M . . . . . −55°C to 125°C
TLC374I . . . . . −40°C to 85°C
TLC374C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D or N package . . . . . 260°C

NOTES: 1. All voltage values except differential voltages are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	7.6 mW/°C	84°C	494 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC374M)	500 mW	11.0 mW/°C	104°C	500 mW	500 mW	275 mW
J (TLC374I, TLC374C)	500 mW	N/A	N/A	500 mW	500 mW	N/A
N	500 mW	N/A	N/A	500 mW	500 mW	N/A

recommended operating conditions

		M-SUFFIX			I-SUFFIX			C-SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}		4		16	3		16	3		16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	0		3.5	0		3.5	0		3.5	V
	V_{DD} = 10 V	0		8.5	0		8.5	0		8.5	
Operating free-air temperature, T_A		−55		125	−40		85	0		70	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			TLC374M			TLC374I			TLC374C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR} min, See Note 4		25°C		1	5		1	5		1	5	mV
				Full range			10			7			6.5	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX T_A			10			1			0.3	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX T_A			20			2			0.6	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD}−1			0 to V_{DD}−1			0 to V_{DD}−1			V
				Full range	0 to V_{DD}−1.5			0 to V_{DD}−1.5			0 to V_{DD}−1.5			
I_{OH}	High-level output current	V_{ID} = 1 V	V_{OH} = 5 V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15 V	Full range			1			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V,	I_{OL} = 4 mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (four comparators)	V_{ID} = 1 V,	No load	25°C		300	600		300	600		300	600	μA
				Full range			800			800			800	

†All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is −55°C to 125°C for TLC374M, 0°C to 70°C for TLC374C, and −40°C to 85°C for TLC374I. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF‡, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

‡C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

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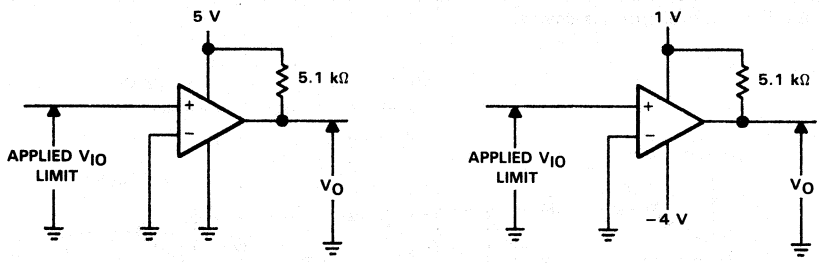
PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLC374 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternative for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 1(b) for the V_{ICR} test, rather than changing the input voltages, to provide greater accuracy.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.



(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is ''sliced'' symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

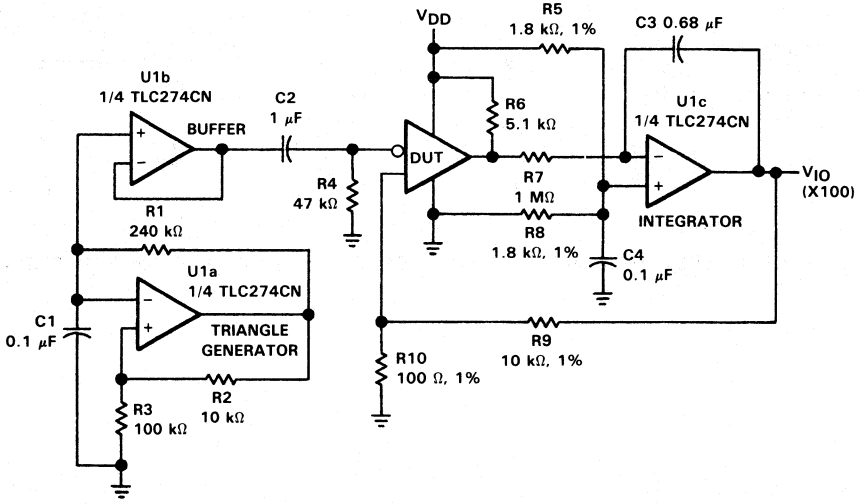


FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

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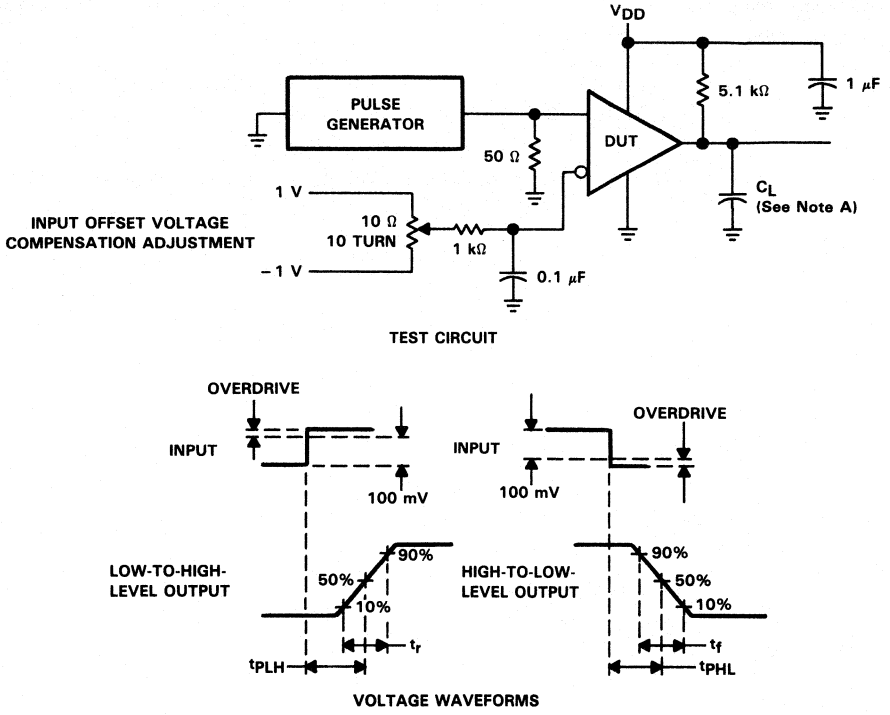
PARAMETER MEASUREMENT INFORMATION

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time, low-to-high-level output, is measured from the leading edge of the input pulse, while response time, high-to-low-level output, is measured from the trailing edge of the input pulse. Response-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



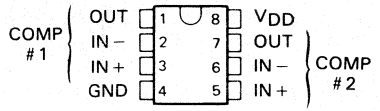
NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. RESPONSE, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

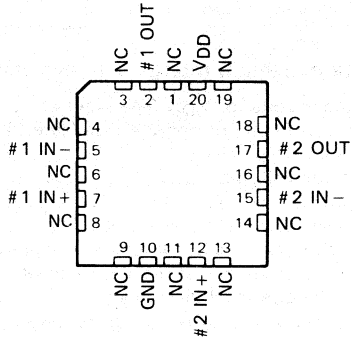
D3241, DECEMBER 1986—REVISED FEBRUARY 1989

- **Very Low Power . . . 100 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive**
- **Single Supply Operation:**
  TLC393M . . . 4 V to 16 V
  TLC393I . . . 3 V to 16 V
  TLC393C . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

TLC393M . . . JG PACKAGE
TLC393I, TLC393C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TLC393M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

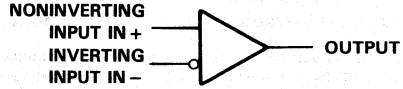
description

The TLC393 consists of two independent differential-voltage comparators designed to operate from a single supply. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The open-drain MOS output stage will interface to a variety of loads and supplies, as well as "wired" logic functions. For a similar device with a push-pull output configuration, see the TLC3702 data sheet.

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC393M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC393I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC393C is characterized for operation over the commercial temperature range of 0°C to 70°C.

symbol (each comparator)



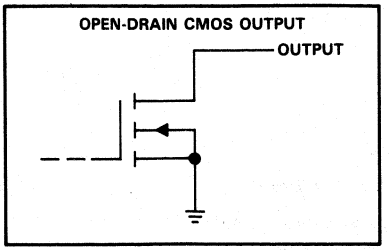
AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC393CD	—	TLC393CJG	TLC393CP
−40°C to 85°C	5 mV	TLC393ID	—	TLC393IJG	TLC393IP
−55°C to 125°C	5 mV	—	TLC393MFK	TLC393MJG	—

The D package is available taped and reeled. Add the suffix R to the device type. (e.g., TLC393CDR)

LinCMOS is a trademark of Texas Instruments Incorporated.

schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . −0.3 V to V_{DD}
Output voltage, V_O . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . 20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 40 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC393M . . . . . −55°C to 125°C
TLC393I . . . . . −40°C to 85°C
TLC393C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (TLC393M)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	528 mW	429 mW	–
P	1000 mW	8.0 mW/°C	640 mW	520 mW	–

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.4	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		84		
			−55°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		84		
			−55°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			125°C			800	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			125°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			−55°C to 125°C			90	

†All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V with a 2.5-kΩ load to V_{DD}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}min$, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−40°C to 85°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C		84		dB
			85°C		84		
			−40°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		84		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			85°C			700	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			85°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			−40°C to 85°C			65	

†All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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ıcommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

lectrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 4	25°C		1.4	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 6 mA	25°C		300	400	mV
			70°C			650	
I_{OH}	High-level output current	V_{ID} = 1 V, V_O = 5 V	25°C		0.8	40	nA
			70°C			1	μA
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		22	40	μA
			0°C to 70°C			50	

All characteristics are measured with zero common-mode voltage unless otherwise noted.
OTE 4: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C (see Figure 3)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		4.5		µs
		Overdrive = 5 mV		2.5		
		Overdrive = 10 mV		1.7		
		Overdrive = 20 mV		1.2		
		Overdrive = 40 mV		1.1		
	V_I = 1.4 V step at IN+ pin			1.1		
t_{PHL} Propagation delay time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 2 mV		3.6		µs
		Overdrive = 5 mV		2.1		
		Overdrive = 10 mV		1.3		
		Overdrive = 20 mV		0.85		
		Overdrive = 40 mV		0.55		
	V_I = 1.4 V step at IN+ pin			0.10		
t_{THL} Transition time, high-to-low level output	f = 10 kHz, C_L = 15 pF	Overdrive = 50 mV		20		ns

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PARAMETER MEASUREMENT INFORMATION

The TLC393 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device. Conventional operational amplifier/comparator testing incorporates the use of a servo-loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for testing parameters such as input offset voltage, common-mode rejection, etc., are suggested.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 1(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

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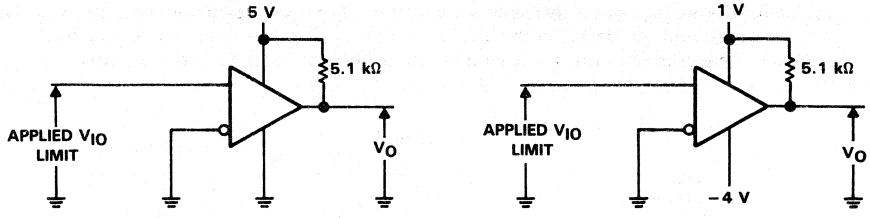

(a) V_{IO} with V_{IC} = 0 (b) V_{IO} with V_{IC} = 4 V

FIGURE 1. METHOD FOR VERIFYING THAT INPUT OFFSET VOLTAGE IS WITHIN SPECIFIED LIMITS

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator into the linear region. The circuit consists of a switching-mode servo-loop in which U1A generates a triangular waveform of approximately 20-mV amplitude. U1B acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by U1C through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is "sliced" symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step-up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

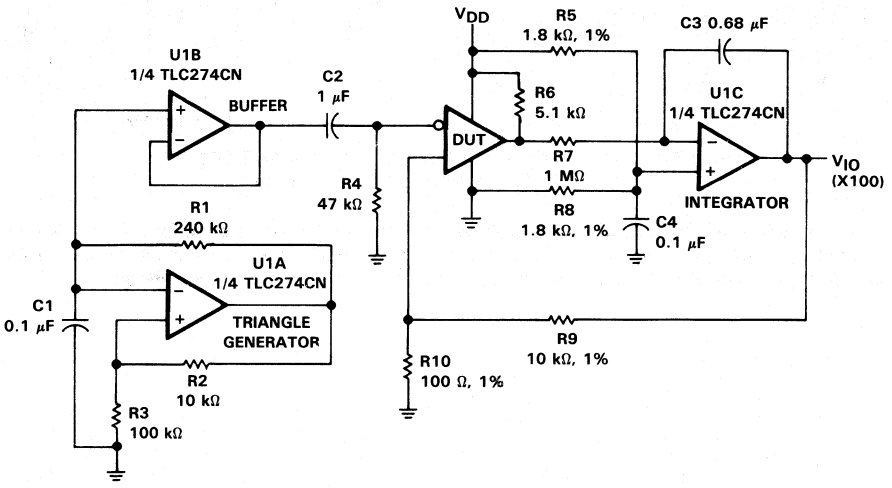

FIGURE 2. CIRCUIT FOR INPUT OFFSET VOLTAGE MEASUREMENT

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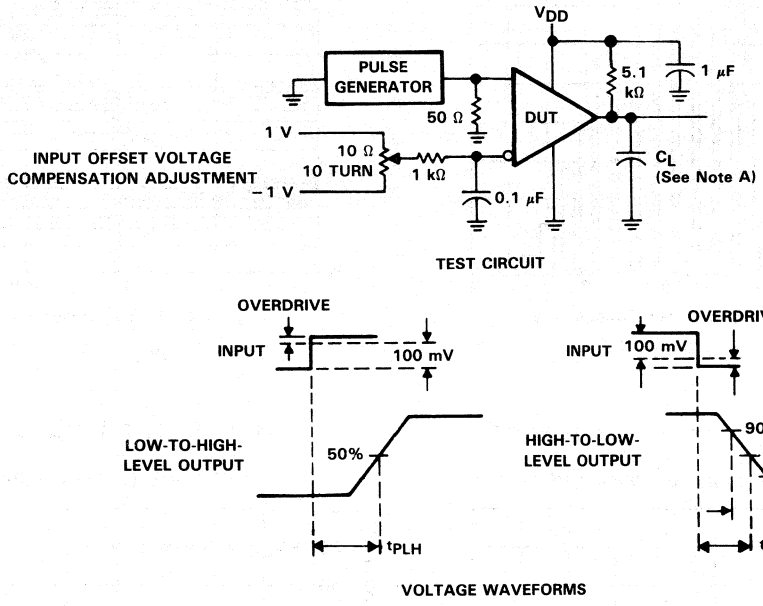
PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Propagation delay time, low-to-high-level output is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105 mV or 5 mV overdrive, will cause the output to change state.



NOTE A: C_L includes probe and jig capacitance.

FIGURE 3. PROPAGATION DELAY, RISE, AND FALL TIMES CIRCUIT AND VOLTAGE WAVEFORMS

TYPICAL CHARACTERISTICS†

DISTRIBUTION OF INPUT OFFSET VOLTAGE

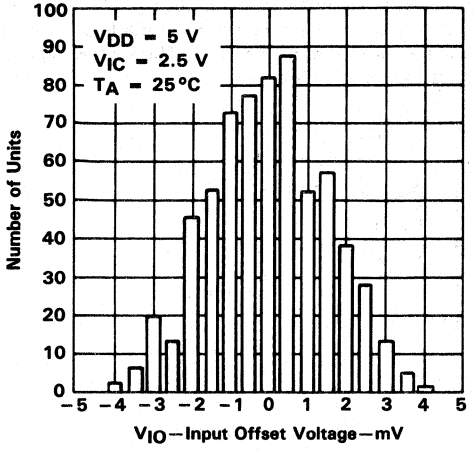


FIGURE 4

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

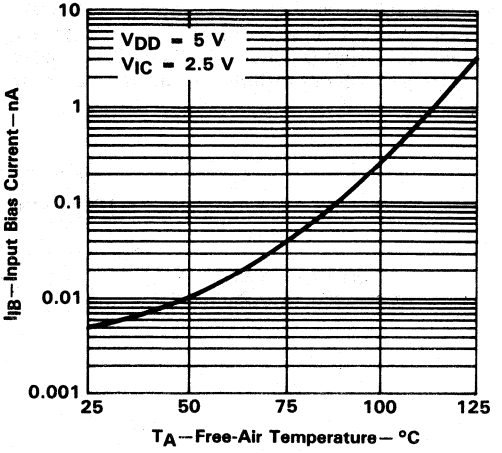


FIGURE 5

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

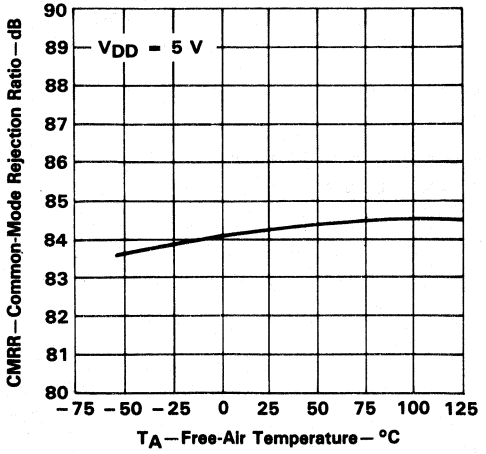


FIGURE 6

SUPPLY VOLTAGE REJECTION RATIO vs FREE-AIR TEMPERATURE

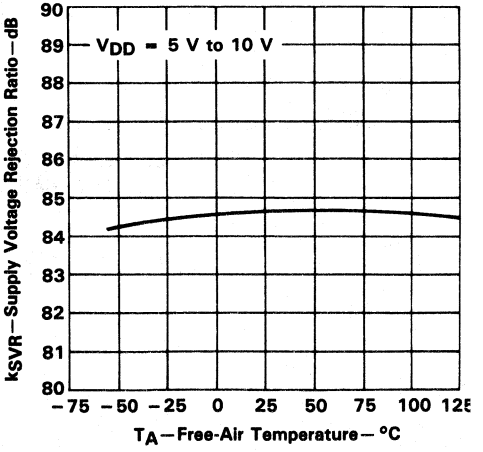


FIGURE 7

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

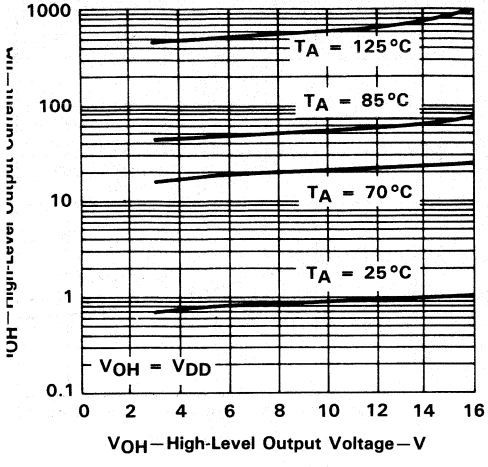


FIGURE 8

HIGH-LEVEL OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

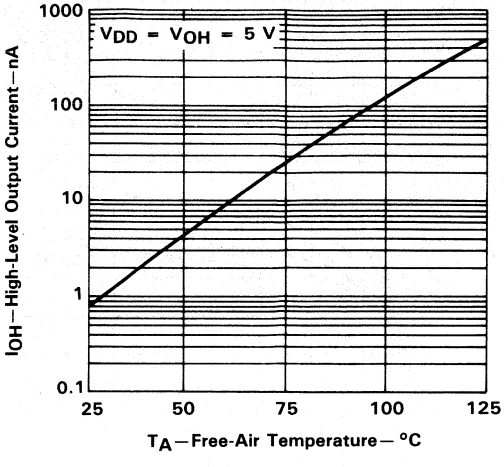


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

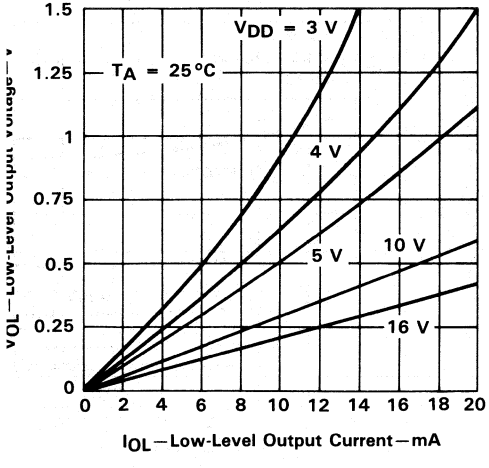


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

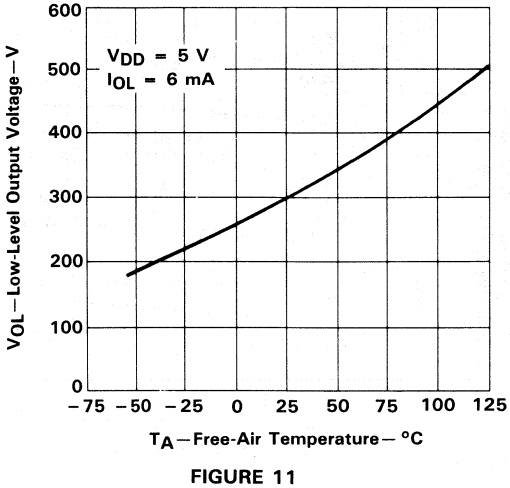


FIGURE 11

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

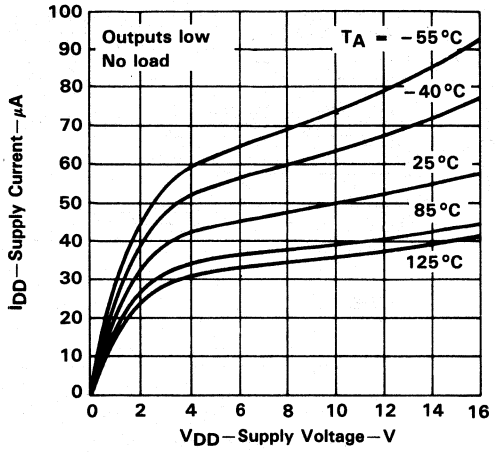


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

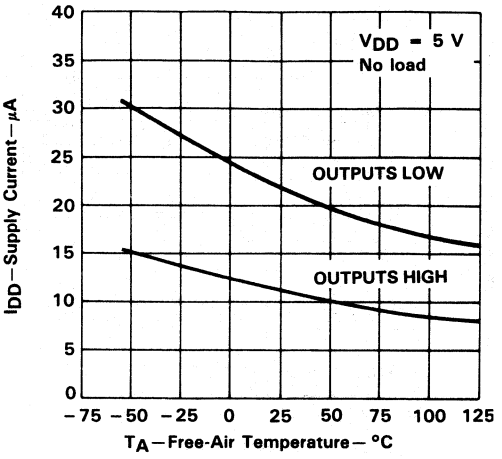


FIGURE 13

LOW-TO-HIGH-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

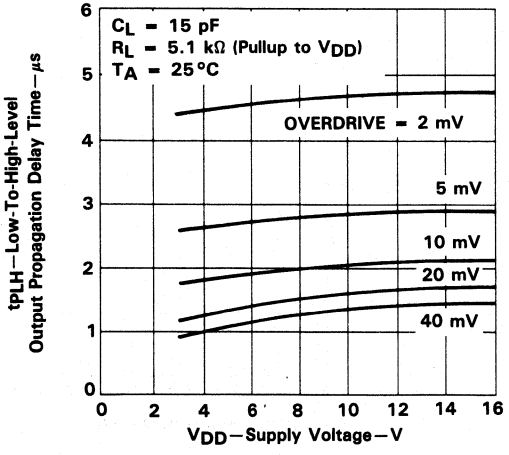


FIGURE 14

HIGH-TO-LOW-LEVEL
OUTPUT RESPONSE TIME
vs
SUPPLY VOLTAGE

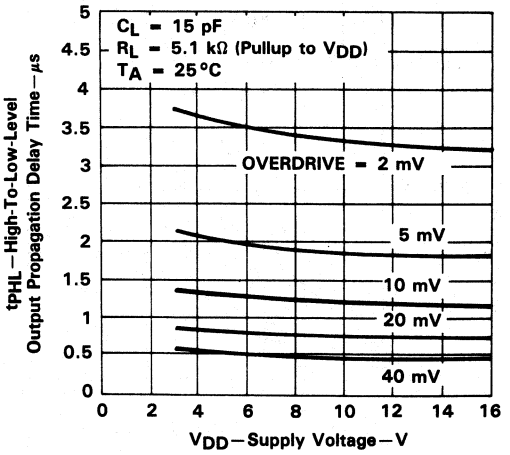


FIGURE 15

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

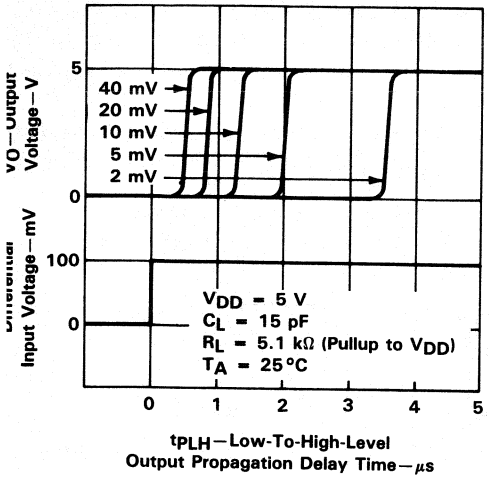


FIGURE 16

OUTPUT FALL TIME vs SUPPLY VOLTAGE

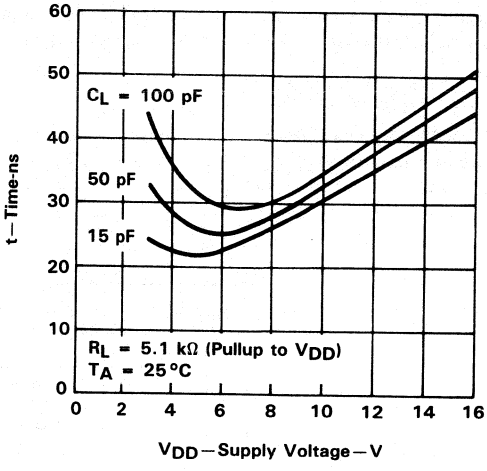


FIGURE 17

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

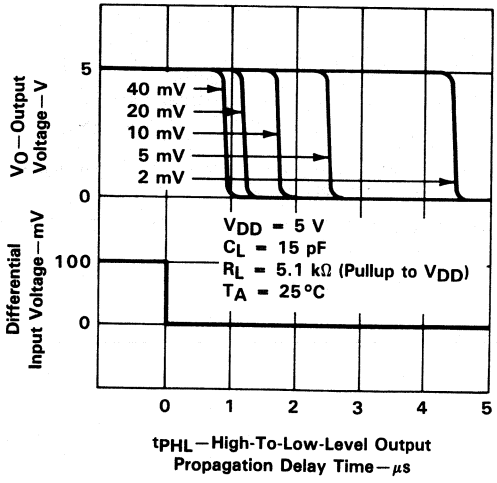


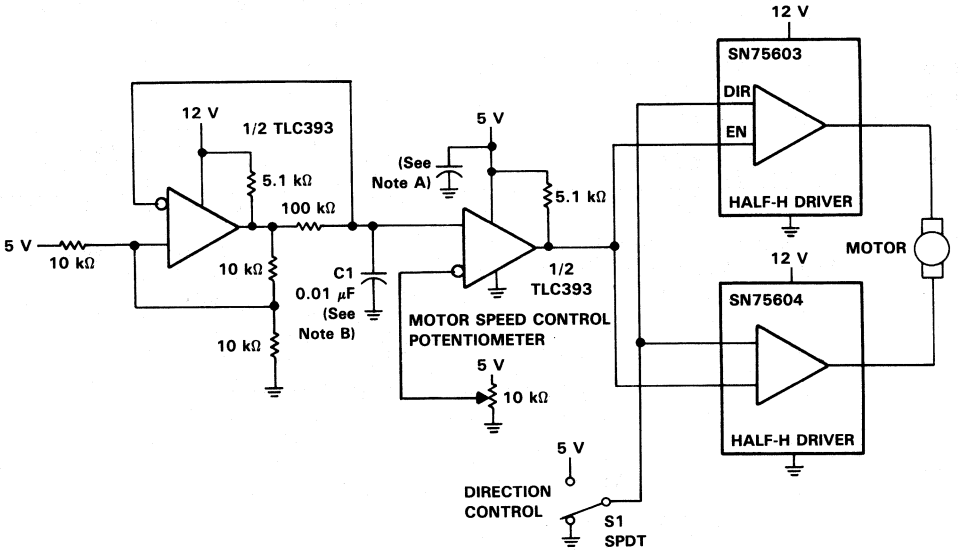
FIGURE 18

TYPICAL APPLICATION DATA

The input should always remain within the supply rails in order to avoid forward biasing the diodes in th electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device will not b damaged as long as the input current is limited to less then 5 mA. To maintain the expected output state, th inputs must remain within the common-mode range. For example, at 25 °C with V_{DD} = 5 V, both inputs mus remain between −0.2 V and 4 V to assure proper device operation.

To assure reliable operation, the supply should be decoupled with a capacitor (0.1 μF) positioned as close t the device as possible.

The TLC393 has internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these device as exposure to ESD may result in the degradation of the device parametric performance.



NOTES: A. The recommended minimum capacitance is 10 μF to eliminate common ground switching noise.
B. Select C1 for change in oscillator frequency.

FIGURE 19. PULSE-WIDTH-MODULATED MOTOR SPEED CONTROLLER

TEXAS INSTRUMENTS
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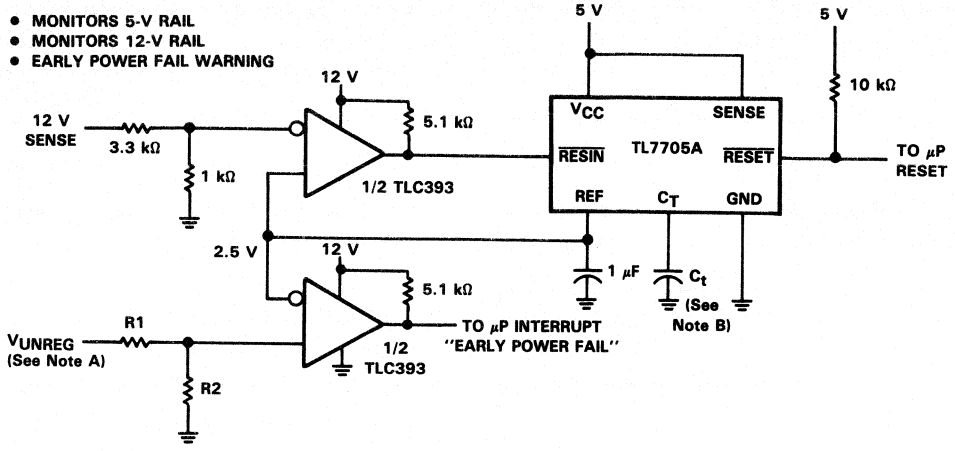
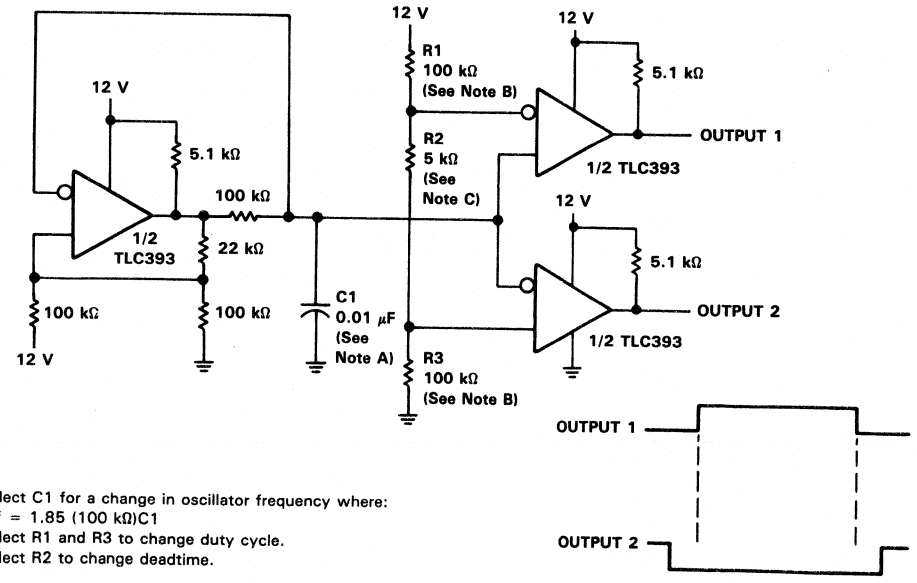
TYPICAL APPLICATION DATA



NOTES: A. $V_{UNREG} = 2.5\left(\frac{R1+R2}{R2}\right)$

B. The value of C_t determines the time delay of reset.

FIGURE 20. ENHANCED SUPPLY SUPERVISOR



NOTES: A. Select C1 for a change in oscillator frequency where:
$1/f = 1.85\ (100\ k\Omega)C1$

B. Select R1 and R3 to change duty cycle.

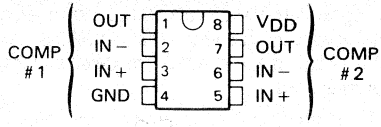
C. Select R2 to change deadtime.

FIGURE 21. TWO-PHASE NONOVERLAPPING CLOCK GENERATOR

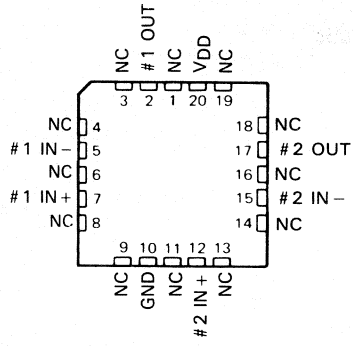
D3209, NOVEMBER 1986—REVISED JANUARY 1989

- **Push-Pull CMOS Output Drives Capacitive Loads without Pull-Up Resistor, $I_O = \pm 8$ mA**
- **Very Low Power . . . 100 µW Typ at 5 V**
- **Fast Response Time . . . 2.5 µs Typ with 5 mV Overdrive**
- **Single Supply Operation:**
  TLC3702M . . . 4 V to 16 V
  TLC3702I . . . 3 V to 16 V
  TLC3702C . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 µV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

TLC3702M . . . JG PACKAGE
TLC3702I, TLC3702C . . . D, JG, OR P PACKAGE
(TOP VIEW)



TLC3702M . . . FK PACKAGE
(TOP VIEW)

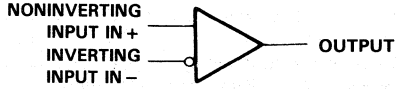


NC—No internal connection

escription

The TLC3702 consists of two independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM393 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

symbol (each comparator)



AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	5 mV	TLC3702CD	—	TLC3702CJG	TLC3702CP
−40°C to 85°C	5 mV	TLC3702ID	—	TLC3702IJG	TLC3702IP
−55°C to 125°C	5 mV	—	TLC3702MFK	TLC3702MJG	—

The D package is available taped and reeled. Add the suffix R to the device type when ordering. (e.g., TL3702CDR)

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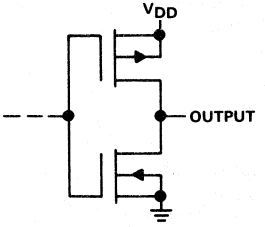
description (continued)

Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3702M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC3702I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC3702C is characterized for operation over the commercial temperature range of 0°C to 70°C.

schematic

PUSH-PULL CMOS OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 V to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . −0.3 V to V_{DD}
Output voltage, V_O . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 40 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC3702M . . . . . −55°C to 125°C
TLC3702I . . . . . −40°C to 85°C
TLC3702C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	–
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (TLC3702M)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (All others)	825 mW	6.6 mW/°C	528 mW	429 mW	–
P	1000 mW	8.0 mW/°C	640 mW	520 mW	–

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ecommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

lectrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise oted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			125°C		83		
			−55°C		82		
kSVR	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		18	40	μA
			−55°C to 125°C			90	

All characteristics are measured with zero common-mode voltage unless otherwise noted.
OTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		V_{DD}−1.5	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwis noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to V_{DD}−1			V
			−40°C to 85°C	0 to V_{DD}−1.5			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C		84		dB
			85°C		84		
			−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		18	40	µA
			−40°C to 85°C			65	

† All characteristics are measured with zero common-mode voltage unless otherwise noted.

NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

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ecommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

lectrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise ıoted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (both comparators)	No load, Outputs low	25°C		18	40	µA
			0°C to 70°C			50	

All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

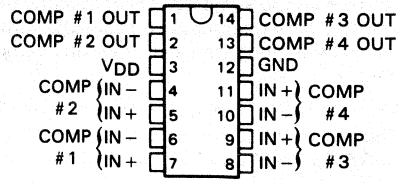
switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		µs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4 V step at IN+ pin			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		µs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4 V step at IN+ pin			0.15		
t_f	Fall time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		125		ns

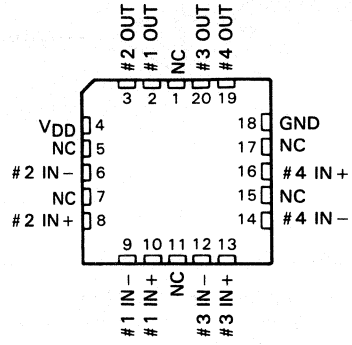
D3240, NOVEMBER 1986—REVISED MARCH 1989

- **Push-Pull CMOS Output Drives Capacitive Loads without Pull-Up Resistor, I_O = ±8 mA**
- **Very Low Power . . . 200 μW Typ at 5 V**
- **Fast Response Time . . . 2.5 μs Typ with 5 mV Overdrive**
- **Single Supply Operation:**
  TLC3704M . . . 4 V to 16 V
  TLC3704I . . . 3 V to 16 V
  TLC3704C . . . 3 V to 16 V
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Input Offset Voltage Change at Worst Case Input Condition Typically 0.23 μV/Month Including the First 30 Days**
- **On-Chip ESD Protection**

TLC3704M . . . J PACKAGE
TLC3704I, TLC3704C . . . D, J, OR N PACKAGE
(TOP VIEW)



TLC3704M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

Description

The TLC3704 consists of four independent differential-voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. It is functionally similar to the LM339 but uses 1/20th the power for similar response times. The push-pull CMOS output stage will drive capacitive loads directly without a power-consuming pull-up resistor to achieve the stated response time. Eliminating the pull-up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

AVAILABLE OPTIONS

T_A	V_{IO}max at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	5 mV	TLC3704CD	—	TLC3704CJ	TLC3704CN
−40°C to 85°C	5 mV	TLC3704ID	—	TLC3704IJ	TLC3704IN
−55°C to 125°C	5 mV	—	TLC3704MFK	TLC3704MJ	—

The D package is available taped and reeled. Add the suffix R to the device type. (e.g., TLC3704CDR)

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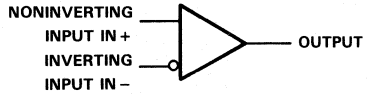
description (continued)

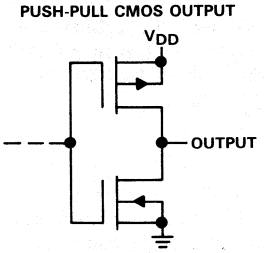
Texas Instruments LinCMOS™ process offers superior analog performance to standard CMOS processes. Along with the standard CMOS advantages of low power without sacrificing speed, high input impedance, and low bias currents, the LinCMOS™ process offers extremely stable input offset voltages, even with differential input stresses of several volts. This characteristic makes it possible to build reliable CMOS comparators.

The TLC3704M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC3704I is characterized for operation over the extended industrial temperature range of −40°C to 85°C. The TLC3704C is characterized for operation over the commercial temperature range of 0°C to 70°C.

symbol (each comparator)



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . −0.3 to 18 V
Differential input voltage (see Note 2) . . . . . ±18 V
Input voltage, V_I . . . . . −0.3 V to V_{DD}
Output voltage, V_O . . . . . −0.3 V to V_{DD}
Input current, I_I . . . . . ±5 mA
Output current, I_O (each output) . . . . . ±20 mA
Total supply current into V_{DD} terminal . . . . . 40 mA
Total current out of ground terminal . . . . . 60 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range: TLC3704M . . . . . −55°C to 125°C
TLC3704I . . . . . −40°C to 85°C
TLC3704C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (TLC3704M)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (All others)	1025 mW	8.2 mW/°C	656 mW	533 mW	—
N	1150 mW	9.2 mW/°C	736 mW	598 mW	—

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4	5	16	V
Common-mode input voltage, V_{IC}	0		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}min$, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			−55°C to 125°C			10	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			125°C			15	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			125°C			30	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−55°C to 125°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C		84		dB
			125°C		83		
			−55°C		82		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			125°C		85		
			−55°C		82		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			125°C	4.2			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			125°C			500	
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		35	80	μA
			−55°C to 125°C			175	

†All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−40		85	°C

electrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			−40°C to 85°C			7	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			85°C			1	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			85°C			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			−40°C to 85°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			85°C		84		
			−40°C		83		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			85°C		85		
			−40°C		83		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			85°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			85°C			400	
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		35	80	μA
			−40°C to 85°C			125	

†All characteristics are measured with zero common-mode voltage unless otherwise noted.
NOTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

ecommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	16	V
Common-mode input voltage, V_{IC}	−0.2		$V_{DD}-1.5$	V
High-level output current, I_{OH}			−20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

lectrical characteristics at specified operating free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, V_{DD} = 5 V to 10 V, See Note 3	25°C		1.2	5	mV
			0°C to 70°C			6.5	
I_{IO}	Input offset current	V_{IC} = 2.5 V	25°C		1		pA
			70°C			0.3	nA
I_{IB}	Input bias current	V_{IC} = 2.5 V	25°C		5		pA
			70°C			0.6	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to $V_{DD}-1$			V
			0°C to 70°C	0 to $V_{DD}-1.5$			
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C		84		dB
			70°C		84		
			0°C		84		
k_{SVR}	Supply voltage rejection ratio	V_{DD} = 5 V to 10 V	25°C		85		dB
			70°C		85		
			0°C		85		
V_{OH}	High-level output voltage	V_{ID} = 1 V, I_{OH} = −4 mA	25°C	4.5	4.7		V
			70°C	4.3			
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 4 mA	25°C		210	300	mV
			70°C			375	
I_{DD}	Supply current (four comparators)	No load, Outputs low	25°C		35	80	μA
			0°C to 70°C			100	

All characteristics are measured with zero common-mode voltage unless otherwise noted.
OTE 3: The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

switching characteristics, V_{DD} = 5 V, T_A = 25°C

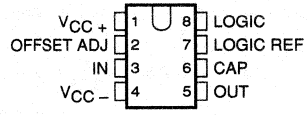
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.5		μs
			Overdrive = 5 mV		2.7		
			Overdrive = 10 mV		1.9		
			Overdrive = 20 mV		1.4		
			Overdrive = 40 mV		1.1		
		V_I = 1.4-V step at IN+ pin			1.1		
t_{PHL}	Propagation delay time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 2 mV		4.0		μs
			Overdrive = 5 mV		2.3		
			Overdrive = 10 mV		1.5		
			Overdrive = 20 mV		0.95		
			Overdrive = 40 mV		0.65		
		V_I = 1.4-V step at IN+ pin			0.15		
t_f	Fall time, high-to-low-level output	f = 10 kHz, C_L = 50 pF	Overdrive = 50 mV		50		ns
t_r	Rise time, low-to-high-level output	f = 10 kHz C_L = 50 pF	Overdrive = 50 mV		125		ns

Contents

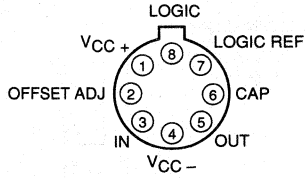
D3218, JULY 1988 – REVISED MARCH 1989

- **Acquisition Time . . . 4 μs Typ**
- **Gain Error . . . 0.01% Max, 0.001% Typ for LF198A, LF398A**
- **Input Offset Voltage . . . 1 mV Max for LF198A, 2 mV Max for LF398A**
- **Hold Step . . . 1 mV Max for LF198A, LF398A**
- **Very Low Feedthrough Attenuation Ratio at f = 1 kHz . . . 96 dB Typ**
- **High Input Impedance . . . 10^{10} Ω Typ**
- **Logic Inputs Compatible With All Logic Families**

JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



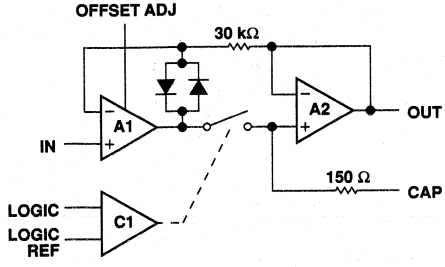
description

These sample-and-hold amplifiers use a combination of bipolar and junction FET transistors to provide precision, high speed, and long hold times. Input offset voltages as low as 1 mV (LF198A) and gain errors as low as 0.001% (LF198A, LF398A) allow these amplifiers to be used in 12-bit systems. Properly selecting the external hold capacitor optimizes the dynamic performance. Acquisition times can be as low as 4 μs for small capacitors, while hold step and droop errors can be held below 0.1 mV and 30 μV/s, respectively, when using larger capacitors.

The LF198 and LF398 are fixed at unity gain with 10^{10}-Ω input impedance independent of the sample or hold mode. The logic inputs are at a high differential impedance to allow easy interfacing to any logic family without ground loop problems. A separate offset adjust pin can be used to zero the input offset voltage in either the sample or hold mode. Additionally, the hold capacitor can be driven with an external signal to provide precision level shifting or "differencing" operation. The devices operate over a wide supply voltage range from ±5 V to ±18 V with very little change in performance. Key parameters are specified over this full supply range.

The LF198 and LF198A are characterized for operation over the full military temperature range of –55°C to 125°C. The LF398 and LF398A are characterized for operation from 0°C to 70°C.

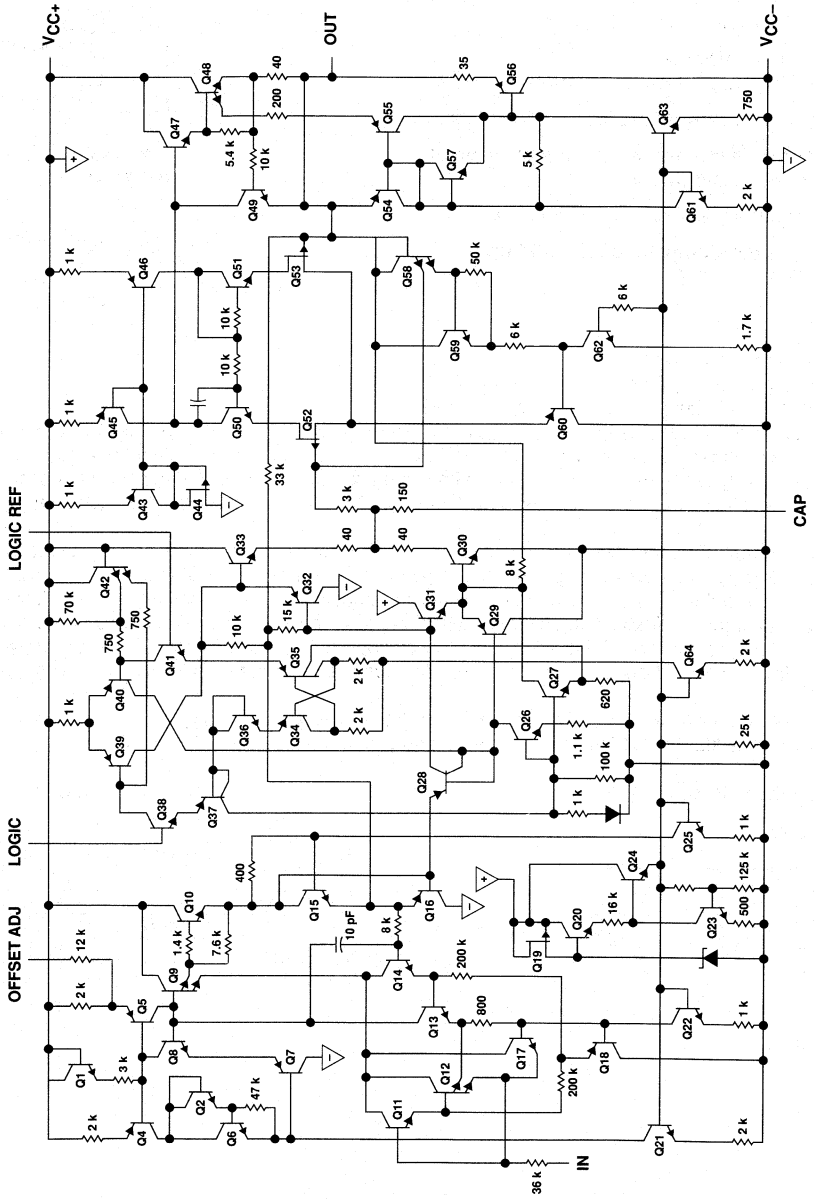
functional block diagram



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE		
		CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	2 mV	—	LF398AL	LF398AP
	7 mV	LF398JG	LF398L	LF398P
–55°C to 125°C	1 mV	—	LF198AL	—
	3 mV	—	LF198L	—

schematic



All resistor values shown are nominal and in ohms.

definition of terms

Acquisition Time
The time required to acquire, within a defined error, a new analog input voltage with an output change of 10 V. Acquisition time includes output settling time and includes the time required for all internal nodes to settle so that the output is at the proper value when switched to the hold mode.

Aperture Time
The delay required between a hold command and an input analog transition so that the transition does not affect the held output.

Dynamic Sampling Error
The error introduced into the held output voltage due to a changing analog input at the time the hold command is given. Dynamic sampling error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error
The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time
The time required for the output to settle within 1 mV of final value after a hold command is initiated.

Hold Step
The voltage step at the output of the amplifier when switching from sample mode to hold mode with a constant analog input voltage and a logic swing of 5 V.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 18 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −18 V
Input voltage range, V_I (any input, see Note 1) . . . . . $V_{CC\pm}$
Differential input voltage, logic to logic reference (see Note 2) . . . . . ±30 V
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . . unlimited
Duration of hold capacitor short-circuit current . . . . . 10 s
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: LF198, LF198A . . . . . −55°C to 125°C
LF398, LF398A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. The logic inputs are protected to ±30 V differential as long as the voltage on both pins does not exceed the supply voltage. For proper operation, however, both the logic and logic reference pins must be at least 2 V below the positive supply, and one of these pins must be at least 3 V above the negative supply.
3. The output may be shorted to either supply.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATING ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
JG (LF198_)	500 mW	8.4 mW/°C	90°C	500 mW	210 mW
JG (LF398_)	500 mW	6.6 mW/°C	74°C	500 mW	N/A
L (LF198_)	500 mW	6.6 mW/°C	74°C	500 mW	165 mW
L (LF398_)	500 mW	5.2 mW/°C	54°C	416 mW	N/A
P	500 mW	8.0 mW/°C	88°C	500 mW	200 mW

electrical characteristics in sample mode, $V_{CC\pm}$ = ±15 V, V_I = ±11.5 V, C_h = 0.01 µF, R_L = 10 kΩ, logic reference at 0 V, logic at 2.5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A†	LF198			LF398			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±5 V to ±18 V	25°C		1	3		2	7	mV
			Full range			5			10	
I_{IB}	Input bias current		25°C		5	25		10	50	nA
			Full range			75			100	
	Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
	Input current, logic and logic reference		25°C		2	10		2	10	µA
	Leakage current into hold capacitor terminal	$V_{CC\pm}$ = ±5 V to ±18 V, Hold mode, See Note 4	25°C		30	100		30	200	pA
	Hold capacitor charging current	$V_I - V_O$ = 2 V	25°C		5			5		mA
z_i	Input impedance		25°C		10^{10}			10^{10}		Ω
z_o	Output impedance	Hold mode	25°C		0.5	2		0.5	4	Ω
			Full range			4			6	
	Gain error (see Note 5)	R_L = 10 kΩ	25°C		0.002	0.005		0.004	0.01	%
			Full range			0.02			0.02	
	Feedthrough attenuation ratio	f = 1 kHz	25°C	86	96		80	96		dB
	Hold step (see Note 6)	V_O = 0	25°C		0.5	2		0.5	2.5	mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ±5V to ±18 V, V_O = 0	25°C	80	110		80	110		V
I_{CC}	Supply current	$V_{CC\pm}$ = ±5 V to ±18 V, $T_A \geq 25°C$	25°C		4.5	5.5		4.5	6.5	mA
	Acquisition time to 0.1% (see Note 5)	ΔV_O = 10 V, C_h = 1 µF	25°C		4			4		µs
		ΔV_O = 10 V, C_h = 0.01 µF			16			16		

†Full range is −55°C to 125°C for the LF198 and 0°C to 70°C for the LF398.

NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.
5. See definition of terms.
6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics in sample mode, $V_{CC\pm}$ = ±15 V, V_I = ±11.5 V, C_h = 0.01 µF, R_L = 10 kΩ, logic reference at 0 V, logic at 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LF198A			LF398A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{CC\pm}$ = ±5 V to ±18 V	25°C		0.5	1		1	2	mV
			Full range			2			3	
I_{IB}	Input bias current		25°C		5	25		10	25	nA
			Full range			75			50	
	Differential logic threshold voltage		25°C	0.8	1.4	2.4	0.8	1.4	2.4	V
	Input current, logic and logic reference		25°C		2	10		2	10	µA
	Leakage current into hold capacitor terminal	$V_{CC\pm}$ = ±5 V to ±18 V, Hold mode, See Note 4	25°C		10	100		10	100	pA
	Hold capacitor charging current	$V_I - V_O$ = 2 V	25°C		5			5		mA
z_i	Input impedance		25°C		10^{10}			10^{10}		Ω
z_o	Output impedance	Hold mode	25°C		0.5	1		0.5	1	Ω
			Full range			4			6	
	Gain error (see Note 5)	R_L = 10 kΩ	25°C		0.001	0.005		0.001	0.005	%
			Full range			0.01			0.01	
	Feedthrough attenuation ratio	f = 1 kHz	25°C	86	96		86	96		dB
	Hold step (see Note 6)	V_O = 0	25°C		0.25	1		0.25	1	mV
k_{SVR}	Supply-voltage rejection ratio	$V_{CC\pm}$ = ±5 V to ±18 V, V_O = 0	25°C	90	110		90	110		V
I_{CC}	Supply current	$V_{CC\pm}$ = ±5 V to ±18 V, T_A ≥ 25°C	25°C		4.5	5.5		4.5	6.5	mA
	Acquisition time to 0.1% (see Note 5)	ΔV_O = 10 V, C_h = 1 µF	25°C		4	6		4	6	µs
		ΔV_O = 10 V, C_h = 0.01 µF			16	25		16	25	

†Full range is −55°C to 125°C for the LF198A and 0°C to 70°C for the LF398A.

NOTES: 4. The effects of a rise in junction temperature due to power dissipation or elevated ambient free-air temperature can be approximated by doubling the 25°C value for each 11°C increase in junction temperature. The specified limit applies for the full input signal range.
5. See definition of terms.
6. See definition of terms. Hold step is sensitive to stray capacitance coupling between input logic signals and the hold capacitor. Stray capacitance of 1 pF, for example, creates an additional 0.5-mV step with a 5-V logic swing and a 0.01-µF hold capacitor. The magnitude of the hold step is inversely proportional to the value of the hold capacitor.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

INPUT BIAS CURRENT
vs
JUNCTION TEMPERATURE

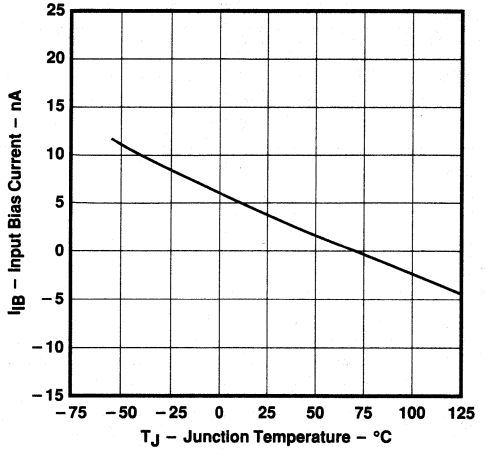


FIGURE 1

LF198A, LF398A
CAPACITOR TERMINAL LEAKAGE CURRENT
vs
JUNCTION TEMPERATURE

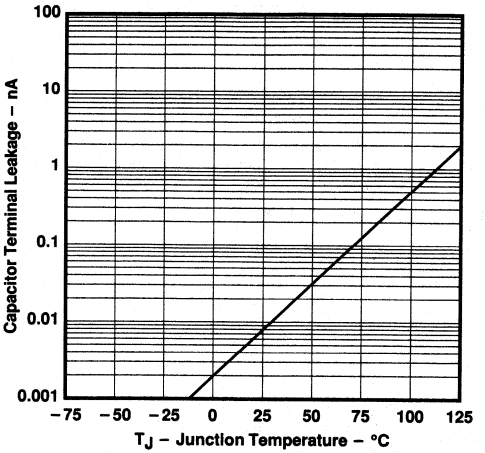


FIGURE 2

GAIN ERROR

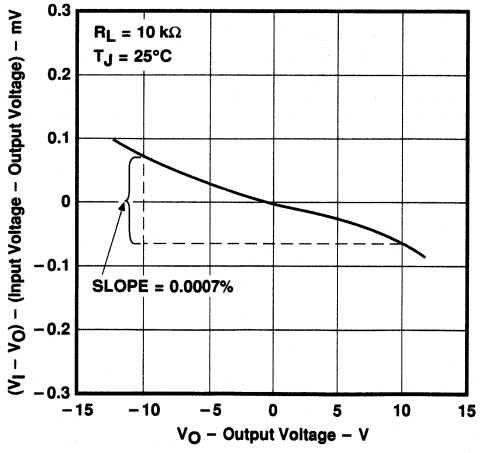


FIGURE 3

FEEDTHROUGH ATTENUATION RATIO
vs
FREQUENCY

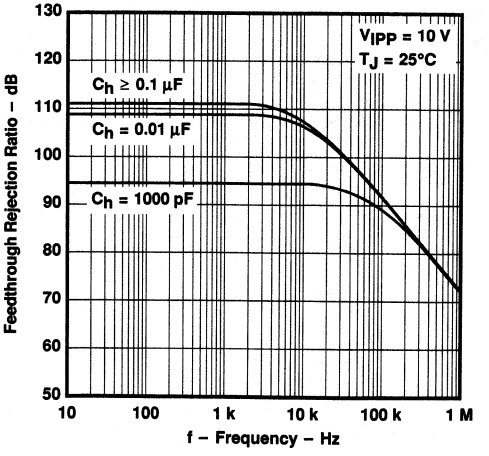


FIGURE 4

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

HOLD STEP
vs
INPUT VOLTAGE

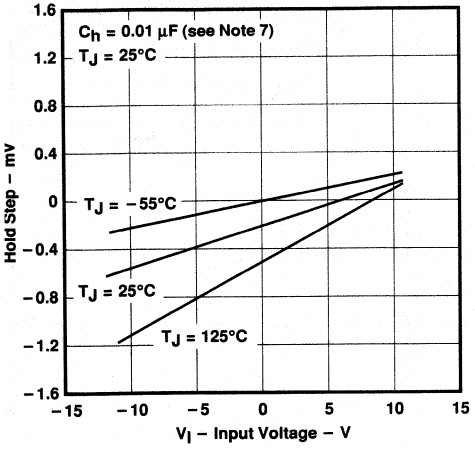

FIGURE 5

HOLD STEP
vs
HOLD CAPACITANCE

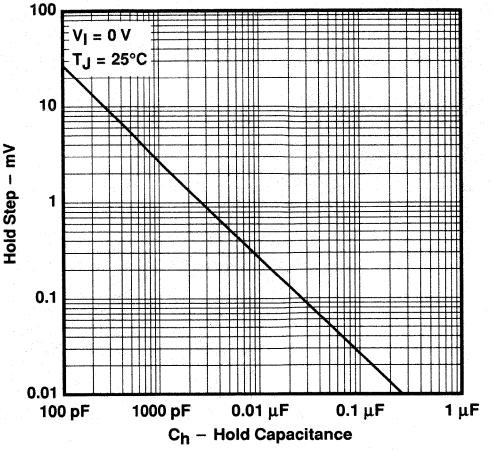

FIGURE 6

HOLD STEP
vs
LOGIC SLEW RATE

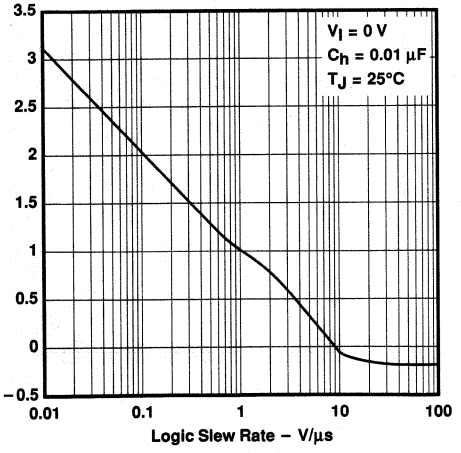

FIGURE 7

SMALL-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION and PHASE DELAY
vs
FREQUENCY

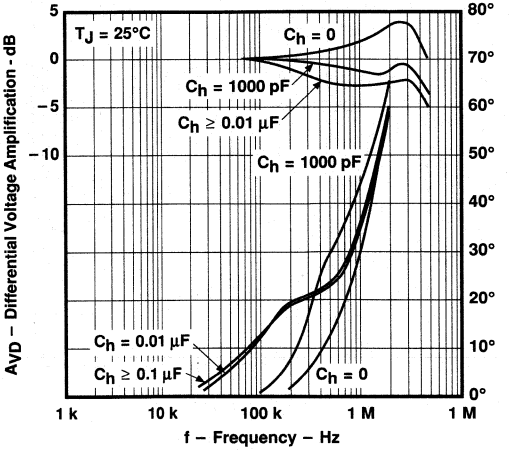

FIGURE 8

ata at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
TE 7: The amplitude of the hold step varies inversely with the value of the hold capacitor.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

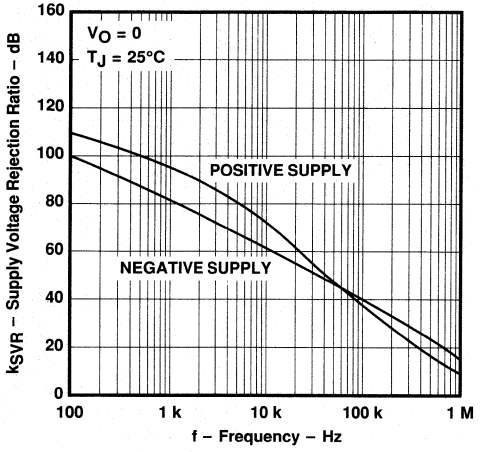

FIGURE 9

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

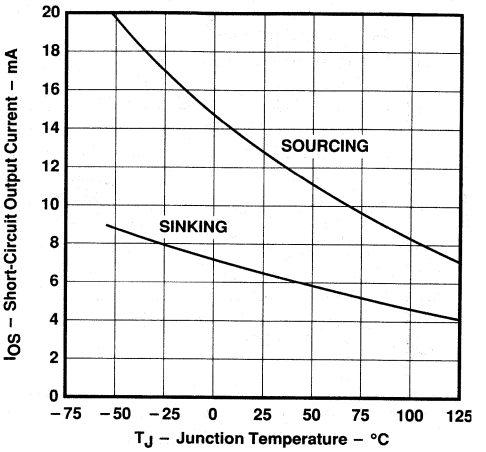

FIGURE 10

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

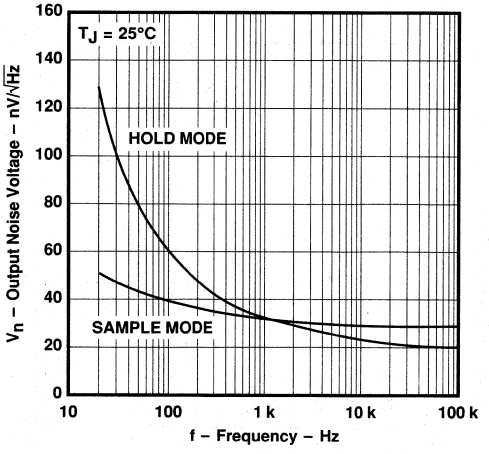

FIGURE 11

DYNAMIC SAMPLING ERROR
vs
INPUT SLEW RATE

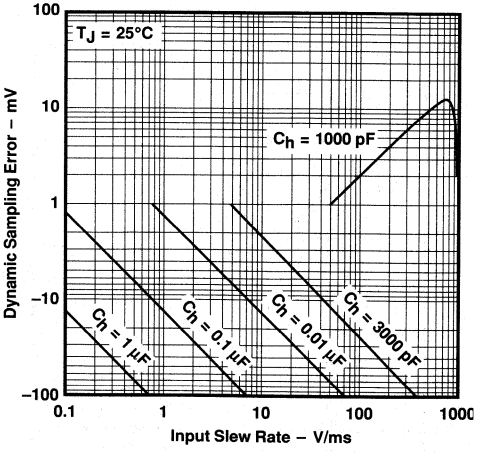

FIGURE 12

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

APERTURE TIME
vs
JUNCTION TEMPERATURE

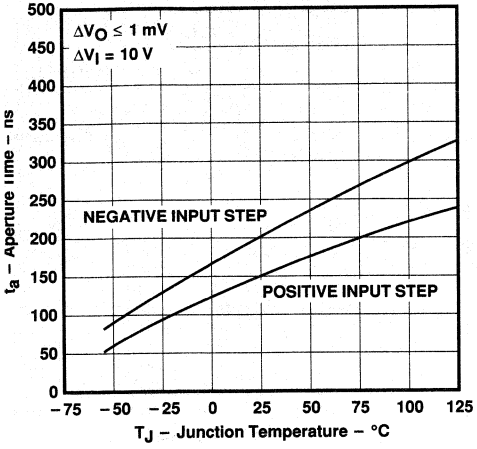

FIGURE 13

HOLD SETTLING TIME
vs
JUNCTION TEMPERATURE

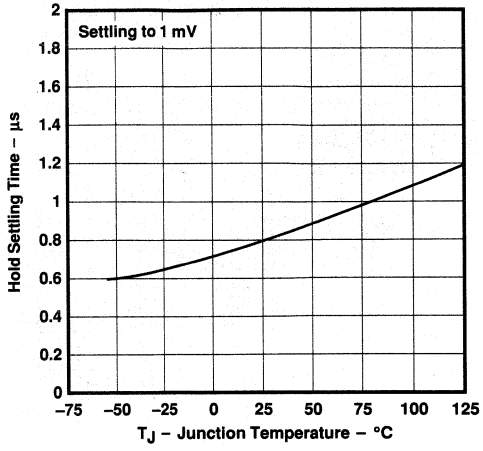

FIGURE 14

ACQUISITION TIME
vs
HOLD CAPACITANCE

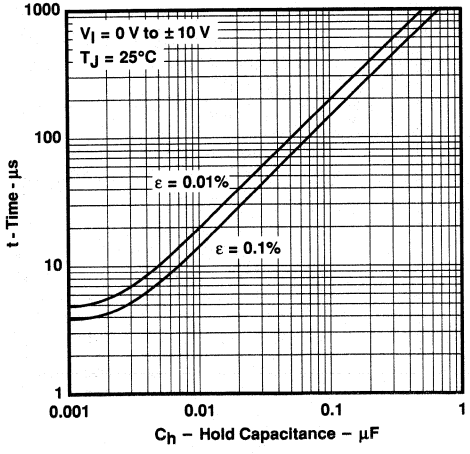

FIGURE 15

OUTPUT DROOP RATE
vs
HOLD CAPACITANCE

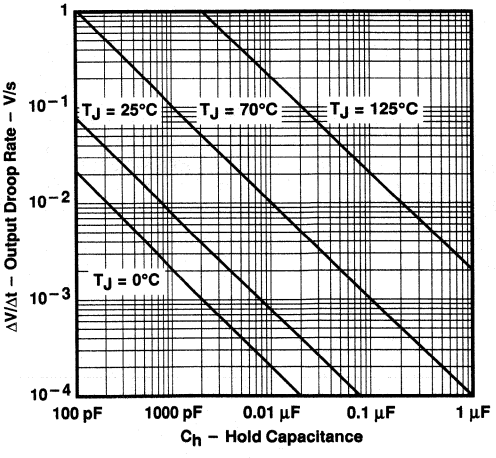

FIGURE 16

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS, $V_{CC\pm}$ = ±15 V†

CAPACITOR DIELECTRIC ABSORPTION
vs
SAMPLE TIME

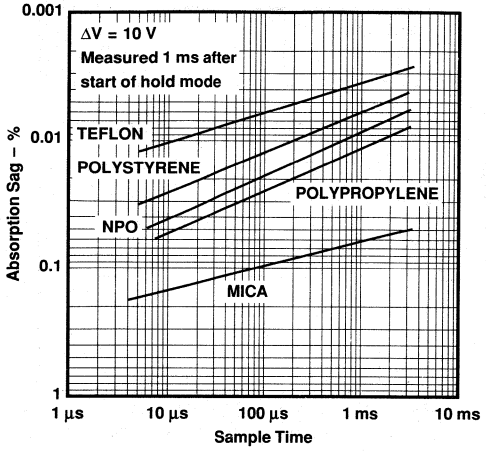

FIGURE 17

CAPACITOR DIELECTRIC ABSORPTION
vs
TIME IN HOLD MODE

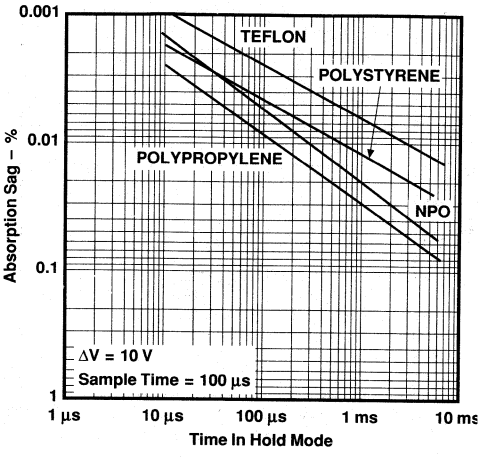

FIGURE 18

OUTPUT TRANSIENT
AT START OF HOLD MODE

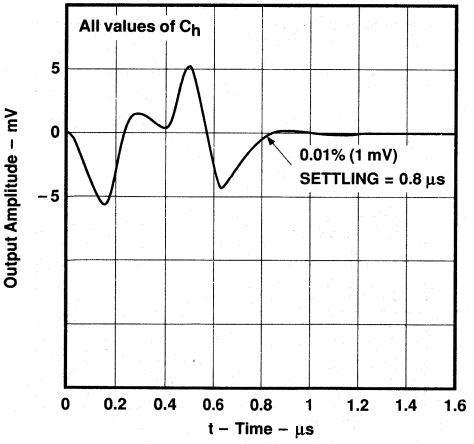

FIGURE 19

OUTPUT TRANSIENT
AT START OF SAMPLE PERIOD

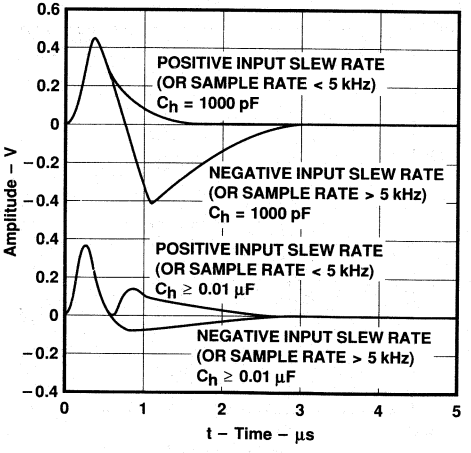

FIGURE 20

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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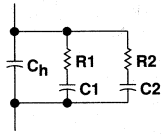
TYPICAL APPLICATION DATA

old capacitor

For fast sample-and-hold applications, the value of the hold capacitor is critical. A low value gives fast acquisition but also increases errors due to hold step and droop caused by amplifier bias current. The capacitor should be made as large as possible consistent with acquisition time and dynamic sampling error requirements. Capacitors larger than 0.1 μF are generally not available in the low-loss dielectrics like Teflon, Polystyrene, and NPO, at least not at a reasonable price and size. Mylar, even with its poor dielectric absorption properties, may be a reasonable choice when very long sample times are used and low droop rates are needed.

Dielectric absorption in the hold capacitor can often be the major source of error in a sample-and-hold amplifier. The equivalent "circuit" of a typical capacitor with parallel RC networks used to model dielectric absorption is shown in Figure 21. In this capacitor, rapid changes in capacitor voltage are not tracked by the internal parasitic capacitors because of the resistance in series with them. This leads to a "sag" effect in the hold capacitor after a sudden change in voltage followed by a rapid switch to the hold mode. The capacitor remembers its previous state via the charge in the internal parasitic capacitance and sags back slightly toward the previous voltage. The magnitude of the sag depends upon the voltage change and the time spent sampling the new voltage. Several time constants are typically evident in the sag, although some capacitors tend to exhibit a single time constant, while others show a sag that indicates a blending of many time constants. Figures 17 and 18 show the amount of sag found after a 10-V step, with sample time at the new voltage and hold time at the new voltage as variables. It is obvious that sag problems are minimized by long sample times and short hold times. While this is often in conflict with basic sampling requirements, the sample-and-hold amplifier should be kept in the "tracking", or sampling, mode as much as possible to maximize the time the hold capacitor spends near the voltage at which it eventually "holds".



NOTE: C1 and C2 are approximately equal to $0.01C_h$ to $0.1C_h$. R1 and R2 generate time constants of 0.1 to 50 ms with C1 and C2.

FIGURE 21. TYPICAL HOLD CAPACITOR EQUIVALENT CIRCUIT

The best capacitor for sample-and-hold applications is Teflon, which is clearly superior with regard to dielectric absorption and operates over the full temperature range (–55°C to 125°C). If size or price is a problem, the second choice for full-temperature-range operation is NPO (or COG) ceramic units. Some care must be used because not all NPO capacitors use the low-dielectric-constant ceramic necessary for low dielectric absorption. For lower temperature (≤ 70°C), Polystyrene has traditionally been the best hold capacitor. The best units are cylindrical and fairly large; there seems to be a strong correlation between small size and poor dielectric performance. Polypropylene has nearly the same absorption properties as polystyrene and offers 85°C operation; it also tends to be smaller. Other standard dielectrics such as mica, glass, mylar, and ordinary ceramic are much worse with regard to dielectric absorption. Mylar is sometimes used for large values when the ratio of sample to hold time is large and extremely low droop is required.

dynamic sampling error

A significant sampling error can occur in any sample-and-hold amplifier if the input is moving when the unit is put into the hold mode. The two major causes for this error are digital delay in switch opening and analog delay across the hold capacitor. The switch opening delay is obvious and leads to a "held" output error of $(dv/dt) \times t_d$; dv/dt is the slew rate of the input signal and t_d is the switch delay. For this device, t_d is approximately 150 ns, giving a 4.5-mV error when sampling the zero crossing of a 5-V (peak) sine wave at 1 kHz ($dv/dt = A \times 2\pi f = 5 \times 2\pi \times 10^3$). The analog delay is the difference between input signal and capacitor voltage. It is determined by the RC product of the hold capacitor and the effective series resistance, which in this device is about 150 Ω.

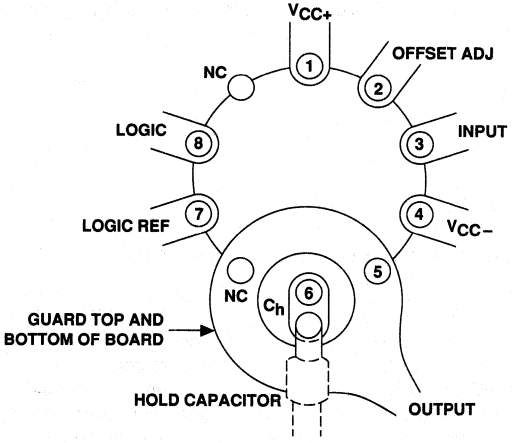
TYPICAL APPLICATION DATA

This analog delay with a 0.01-μF hold capacitor is $R \times C = 150 \times 10^{-8} = 1.5\ \mu s$, or about ten times the dela of the switch. The held output is related in time to the input voltage *before* the hold command was given. Th overall dynamic sampling error is the sum of the digital and analog errors. Figure 12 helps estimate these erro as a function of input slew rate and hold capacitor size.

Dynamic sampling error can be reduced by a factor of ten or more by inserting a delay in the logic input so th the "hold" command is delayed by an amount equal to the RC time constant of the device and the external ho capacitor. For a 0.01-μF hold capacitor and the 150-Ω resistor internal to this device, this value is 1.5 μs. A simp RC network can be used in front of the logic input for delays up to approximately 1 μs. Longer delays requi the addition of a logic gate to speed up the rise time of the delayed signal. See "logic rise time" for further detail

hold step

Hold step is the small voltage step (after settling) seen at the output of a sample-and-hold amplifier when it switched from the sample mode to the hold mode with a steady dc input. Hold step is typically the result of, can be modeled as, a fixed quantity of charge transferred to the hold capacitor due to internal switching th occurs during the hold command. In the case of this device, that charge is approximately 5 pC, giving a hold ste of 0.5 mV for a 0.01-μF hold capacitor and 5 mV for a 1000-pF hold capacitor (V = Q/C). Hold step is reasonab independent of logic amplitude if care is taken to minimize the stray capacitance between the logic input and th hold capacitor. With thoughtful layout, including the guarding technique shown in Figure 21, stray capacitanc should be under 0.3 pC, limiting charge variations to less than 0.3 pC/V.



NOTE: Use 10-pin layout. The guard around C_h is tied to output.

FIGURE 22. GUARDING TECHNIQUE (BOTTOM VIEW)

Hold step varies slightly with analog input voltage (see Typical Characteristics). A typical unit changes at a rat of 0.4 pC/V. This slight variation manifests itself as a gain error when the amplifier is switched to the hold mode With a 0.01-μF capacitor, the resulting gain error is (0.4 pC/V)/0.01 μF = 0.004%. This gain error is in th opposite direction of dc (sample mode) gain error. When the hold capacitor has a high value, dc gain erro dominates and gain is slightly below unity (0.002%). When the hold capacitor has a low value (< 0.01 μF), gai error induced by hold step dominates, and hold-mode gain is slightly above unity. Zeroing out hold step doe not change the variation of hold step with regard to input voltage.

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TYPICAL APPLICATION DATA

›ffset zeroing

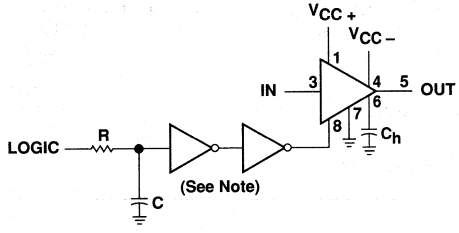
A sample-and-hold amplifier has two distinct offset voltages. The first is the dc offset voltage of the amplifier while in the sample, or "tracking," mode. It is identical to the input offset voltage of any operational amplifier. The second offset voltage is the sum of the dc offset voltage plus a dynamic term called hold step. Hold step is a change in output voltage when the amplifier is switched from sample mode to hold mode with the input held steady. This second offset voltage is often called hold-mode offset voltage. It can be less than or much greater than the dc offset voltage, depending on the magnitude and sign of hold step.

A fairly accurate model for hold step is a fixed charge injected into the hold capacitor by the switch turn-off circuitry. The magnitude of the charge is reasonably independent of logic input amplitude. The resulting change in the hold capacitor is Q/C_h. The charge Q is typically 5 pC, giving a 0.5-mV hold step with a 0.01-μF hold capacitor. Since most sample-and-hold amplifiers are "used" (i.e., have their outputs read by an A-to-D converter), during the hold mode, hold-mode offset voltage is arguably more important than the sample-mode dc offset voltage.

Adjusting dc offset voltage is accomplished with a 1-kΩ low TC cermet potentiometer tied to V_{CC+} with 0.6 mA flowing through it and the wiper tied to pin 2. This allows pin 2 to be moved ± 300 mV around its nominal voltage (0.3 V below V_{CC+}). The offset voltage adjustment range is ± 9 mV, and the adjustment procedure nominally improves offset voltage drift when the dc offset voltage is reduced to zero. This offset method *can* be used to zero out hold-mode offset voltage, but at the expense of some induced offset voltage drift. Each millivolt of hold-step offset corrected by this method introduces 3.3 μV/°C drift. For 0.002-μF hold capacitors or larger with hold step a few millivolts or less, this is a practical solution to hold-mode offset voltage. In precision, wide-temperature-range applications, or when C_h is less than 0.002 μF, a separate hold-mode zeroing method should be used. The circuit shown in Figure 28, which uses a logic inverter and a 5-pF capacitor, is recommended.

logic fall time

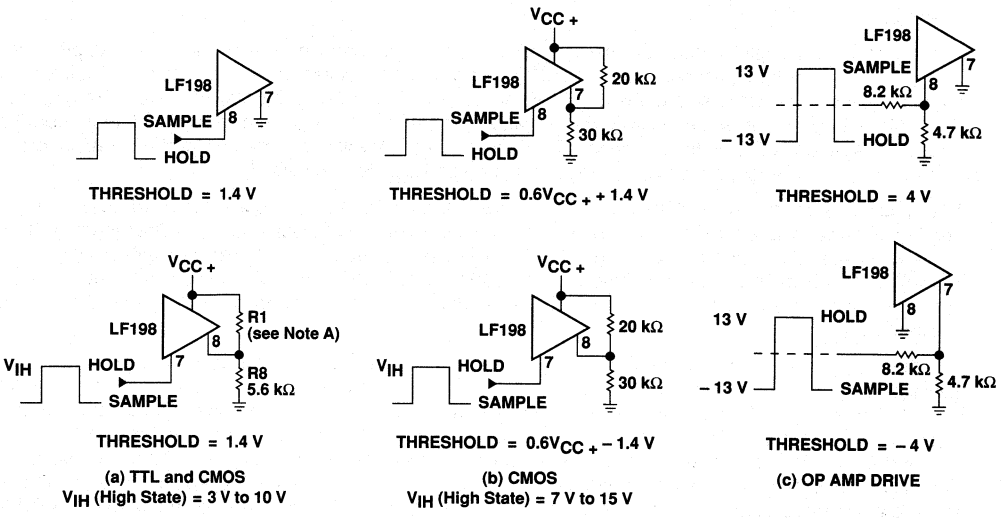
Hold step is independent of logic input fall time only for fall times faster than 10 V/μs. For example, as logic fall time changes from 10 V/μs to 1 V/μs, hold step with a 0.01-μF hold capacitor typically increases from 0.25 mV to 1 mV. (See Figure 7 for more data and refer to Figure 23.) If logic slew rate is not constant, use the value at the threshold point (1.5 V with respect to logic reference). An RC network will have a discharge slew rate of V_L/RC, where V_L is the logic threshold of the LF198. The delay generated by the network will be $RC \times \ln(V_{CC+}/V_L)$, where V_{CC+} is logic amplitude. For a 1-μs delay with 5-V logic , an RC time constant of 0.8 μs is required. This has a slew rate of 2 V/μs at threshold, which slightly degrades hold step. It is obvious that an RC delay network significantly longer than 1 μs will have a large effect on hold step. If longer delays are required, they should be followed by several inverter stages or a Schmitt trigger to increase slew rate.



NOTE: Inverters may be eliminated for RC ≤ 3 μs.

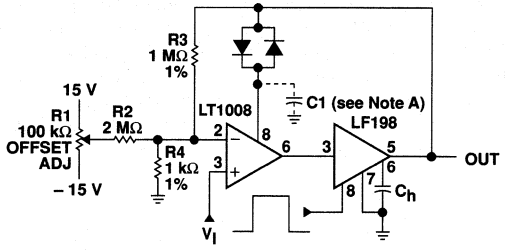
FIGURE 23. ADDING DELAY TO LOGIC INPUT

TYPICAL APPLICATION DATA



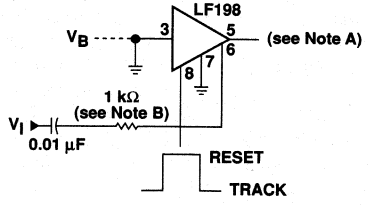
NOTES: A. Select R1 for 2.8 V at pin 8.
B. The logic input signal high level must be at least 2 V below the positive supply voltage of the device.

FIGURE 24. LOGIC INPUT CONFIGURATIONS



NOTE A: For lower gains, the LT1008 must be frequency compensated. Use approximately (100/A_V) pF from comp2 to ground.

FIGURE 25. x1000 SAMPLE-AND-HOLD



NOTES: A. $V_O = V_B + \Delta V_I$ (Hold mode).
B. This resistor protects input from surge currents but increases sample time. It can be eliminated if input is otherwise protected.
C. Output follows input in hold mode and resets to V_B in sample mode.

FIGURE 26. SAMPLE-AND-DIFFERENCE CIRCUIT

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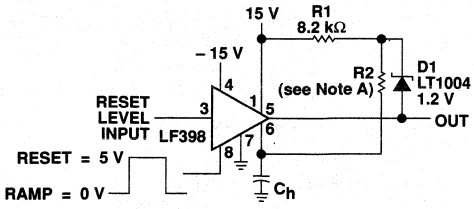
TYPICAL APPLICATION DATA



NOTE A: Select R2 for ramp rate $\Delta V/\Delta t = 1.2\ V/(R2)(C_h)$, $R \geq 10\ k\Omega$.

FIGURE 27. RAMP GENERATOR WITH VARIABLE RESET LEVEL

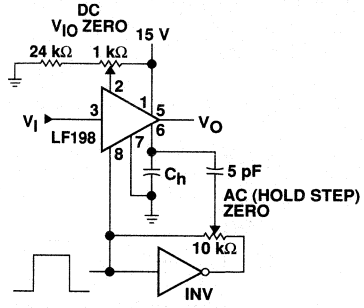
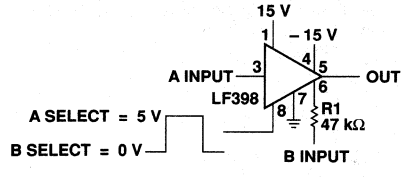
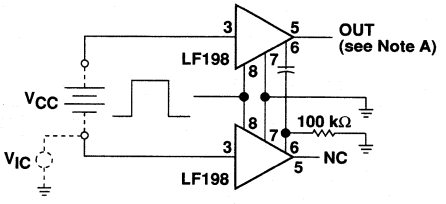


FIGURE 28. DC AND AC ZEROING



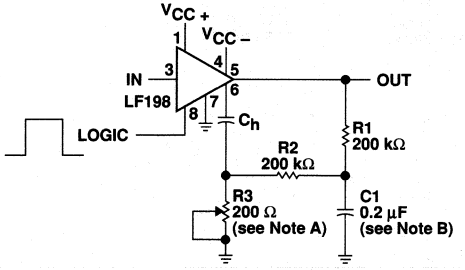
PARAMETER	A	B	UNIT
Gain	1 ± 0.02	1 ± 0.2	%
z_i	10^7	47	kΩ
BW	≈ 1000	≈ 400	kHz
Crosstalk at 1 kHz	– 90	– 90	dB
Offset	≤ 6	≤ 75	mV

FIGURE 29. 2-CHANNEL SWITCH



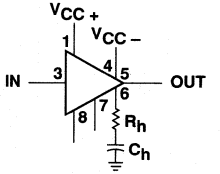
NOTE A: Output equals V_{CC} when in hold mode. Output equals (V_{CC} + V_{IC}) when in sample mode.

FIGURE 30. DIFFERENTIAL HOLD



NOTES: A. Adjust R3 for amplitude.
B. Select for time constant C1 = τ /100 kΩ.

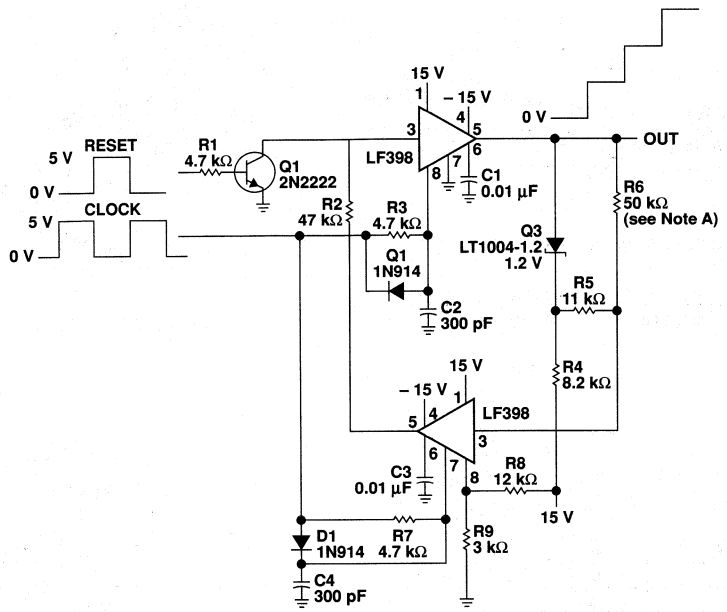
FIGURE 31. CAPACITOR HYSTERESIS COMPENSATION



NOTE A: Select $(R_h)(C_h) >> \frac{1}{2\pi f_{I(MIN)}}$

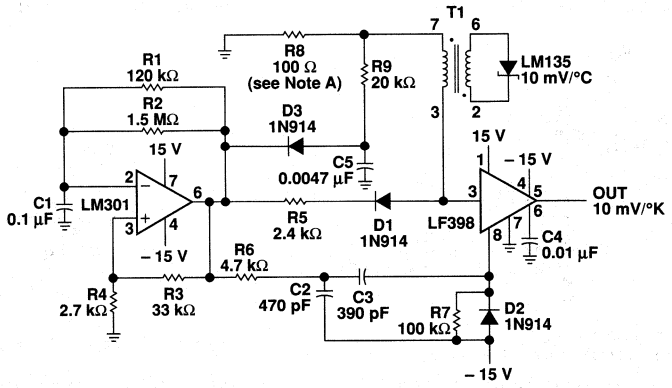
FIGURE 32. OUTPUT HOLDS AT AVERAGE OF SAMPLED INPUT

TYPICAL APPLICATION DATA



NOTE A: Select R6 for step height. 50 kΩ ≈ 1-V step.

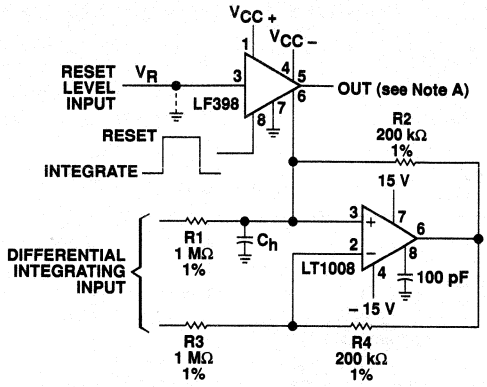
FIGURE 33. STAIRCASE GENERATOR



NOTE A: R8 compensates for transformer resistance. Select for flat output from LF198 while in sample mode.

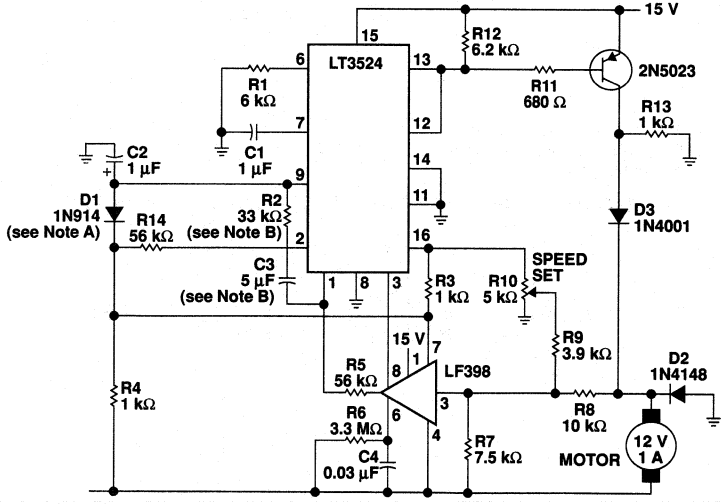
FIGURE 34. ISOLATED TEMPERATURE SENSOR

TYPICAL APPLICATION DATA



NOTE A: $V_{O(Hold\ mode)} = \left[\frac{1}{(R1)(C_h)}\int_0^t V_I dt\right] + V_R$

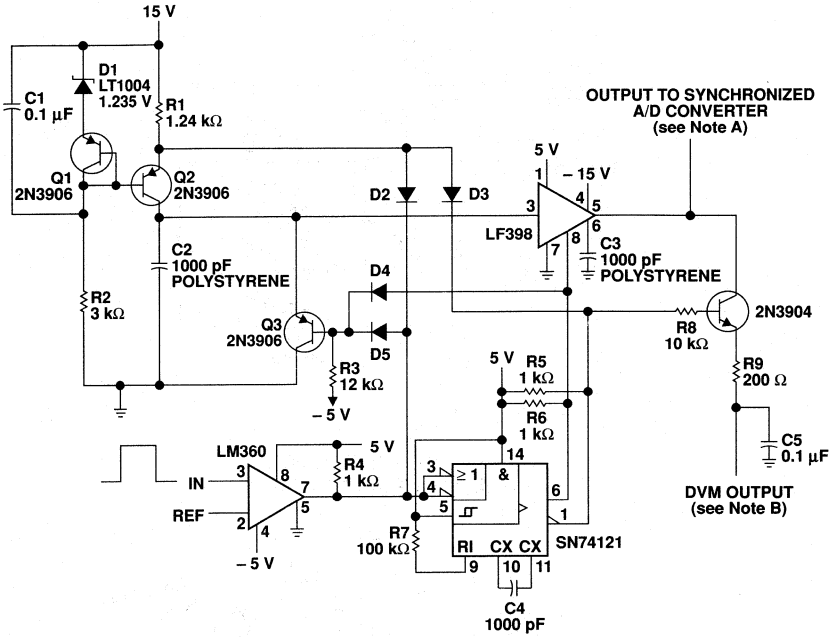
FIGURE 35. INTEGRATOR WITH PROGRAMMABLE RESET LEVEL



NOTES: A. D1 is used for start-up. It limits duty cycle to approximately 75%.
B. Select for optimum loop stability. C3 is nonpolarized.
C. No tachometer is needed; back EMF of motor is sampled and used to control speed.

FIGURE 36. MOTOR SPEED CONTROLLER

TYPICAL APPLICATION DATA



NOTES: A. Read ≥ 1 µs after Q goes low.
B. For repetitive pulses only. Increase C5 for f ≤ 10 kHz.
C. D2-D5 1N914.

FIGURE 37. PULSE DURATION TO VOLTAGE CONVERTER

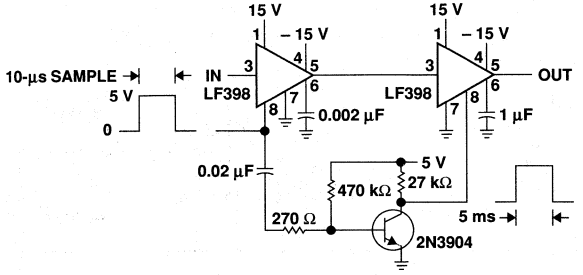


FIGURE 38. FAST-ACQUISITION, LOW-DROOP SAMPLE-AND-HOLD

TEXAS INSTRUMENTS
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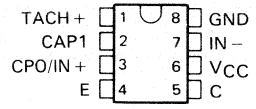
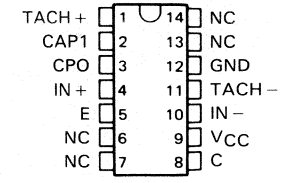
D3003, MARCH 1986—REVISED OCTOBER 1988

- **Output Swings to Ground for Zero-Frequency Input**
- **Only One RC Network Provides Frequency Doubling for Low Ripple**
- **8-Pin Versions Interface Directly to Variable-Reluctance Magnetic Pickups**
- **Uncommitted Collector and Emitter Outputs Provide 40-mA Sink or Source Current to Operate Relays, Solenoids, Meters, or LEDs**
- **Built-In Hysteresis for Noise Immunity**
- **Linearity Typically ±0.3%**
- **8-Pin Versions are Fully Protected from Damage Due to TACH Input Swing Above V_{CC} and Below Ground**

LM2907, LM2917 . . . D OR P PACKAGE
(TOP VIEW)



LM2907, LM2917 . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

pplications

Over/under speed sensing
Frequency-to-voltage conversion
Speedometers
Breaker-point dwell meters
Hand-held tachometers
Speed governors
Cruise control
Automotive door-lock control
Clutch control
Horn control
Touch or sound switches

escription

The LM2907 and LM2917 are monolithic frequency-to-voltage converters with an output circuit designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The converter (tachometer) section consists of a comparator driving a charge pump and offers frequency doubling for low ripple, full input protection in 8-pin versions, and an output swing to ground for a zero-frequency input. The output section consists of an operational amplifier, normally operating as a comparator, that drives an output transistor with both the collector and emitter floating. The circuit can either sink or source 40 mA of load current.

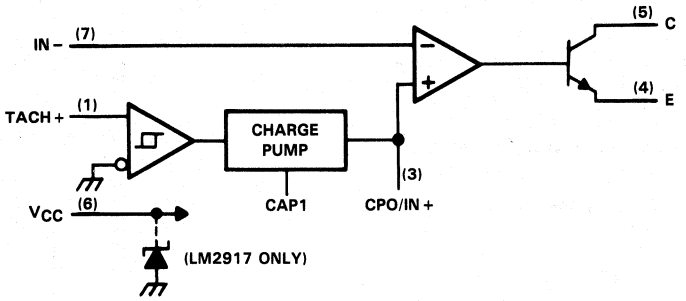
Two basic configurations of the devices are offered; an 8-pin version and a 14-pin version. The 8-pin versions have a ground-referenced tachometer input and an internal connection between the tachometer output and the operational amplifier input. The 8-pin version is well suited to single-speed or single-frequency switching or fully buffered frequency-to-voltage conversion applications. The more versatile 14-pin versions provide differential tachometer inputs and uncommitted operational amplifier inputs. In the 14-pin versions, the tachometer input can be floated and the operational amplifier becomes suitable for active filter conditioning of the tachometer output.

The LM2917 has an active shunt regulator connected across the power leads. The regulator clamps the supply voltage so that stable frequency-to-voltage and frequency-to-current conversions are possible with any supply voltage and a suitable resistor.

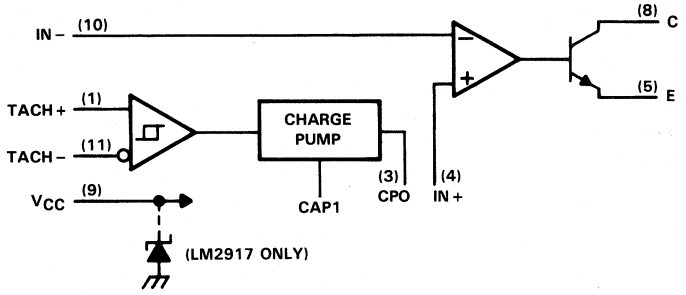
The LM2907 and LM2917 are designed for operation from −40°C to 85°C.

functional block diagrams

8-PIN VERSIONS



14-PIN VERSIONS



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}: LM2907 . . . . . 28 V
Supply current, I_{CC}: LM2917 . . . . . 25 mA
Collector-to-emitter voltage . . . . . 28 V
Operational amplifier input voltage, IN+ and IN– . . . . . 0 V to V_{CC}
Tachometer input voltage: 8-pin version TACH+ . . . . . 0 V to 28 V
14-pin version TACH+ and TACH– . . . . . 0 V to V_{CC}
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . –40°C to 85°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperture range 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D (8 pins)	725 mW	5.8 mW/°C	377 mW
D (14 pins)	900 mW	7.2 mW/°C	468 mW
N	1000 mW	7.7 mW/°C	500 mW
P	900 mW	7.2 mW/°C	468 mW

TEXAS INSTRUMENTS
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ectrical characteristics, V_{CC} = 12 V (LM2907), V+ = 12 V through 470 Ω (LM2917), T_A = 25°C

nverter (tachometer) section

PARAMETER			TEST CONDITIONS	LM2907			LM2917			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_T	Input threshold voltage		V_I = 250 mV, f = 1 kHz	±10	±15	±40	±10	±15	±40	mV
V_{hys}	Input hysteresis (see Note 1)		V_I = 250 mV, f = 1 kHz		30			30		mV
V_{IO}	Input offset voltage (see Note 1)	8-pin versions	V_I = 250 mV, f = 1 kHz		5	15		5	15	mV
		14-pin versions	V_{ID} = 250 mV, f = 1 kHz		3.5	10		3.5	10	
I_B	Input bias current		V_I = ±50 mV		0.1	1		0.1	1	μA
V_{OH}	High-level output voltage, CAP1		V_I or V_{ID} = 125 mV		8.3			5.0		V
V_{OL}	Low-level output voltage, CAP1		V_I or V_{ID} = −125 mV		2.3			1.2		V
I_O	Output current, CAP1, CPO		CAP1 and CPO at 6 V	140	180	240				μA
			CAP1 and CPO at 3.8 V				140	180	240	
	Leakage current, CPO		CAP1 open, CPO at 0 V, See Note 3			0.1			0.1	μA
	Gain constant			0.9	1	1.1	0.9	1	1.1	
	Nonlinearity (see Note 2)		f = 1 kHz, 5 kHz, or 10 kHz		0.3	±1		0.3	±1	%

tput section

PARAMETER		TEST CONDITIONS	LM2907			LM2917			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_I = 6 V, See Note 3		3	10				mV
		V_I = 3.8 V, See Note 3					3	10	
I_B	Bias current	V_I = 6 V		50	500				nA
		V_I = 3.8 V					50	500	
A_V	Voltage amplification			200			200		V/mV
I_C	Collector output (sink) current	V_C = 1 V, V_E = 0	40	50		40	50		mA
I_E	Emitter output (source) current	V_C = V_{CC}, V_E = V_{CC} − 2		−10			−10		mA
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 5 mA		0.1	0.5		0.1	0.5	V
		I_C = 20 mA			1			1	
		I_C = 50 mA		1	1.5		1	1.5	

OTES: 1. Hysteresis is the algebraic difference $V_{T+} - V_{T-}$; offset voltage is the difference in magnitudes $|V_{T+}| - |V_{T-}|$. See parameter measurement information test circuits.
2. Nonlinearity is defined as the deviation of V_O at CPO for f = 5 kHz from a straight line defined by the V_O at 1 kHz and V_O at 10 kHz, with C1 = 1000 pF, R1 = 68 kΩ, C2 = 0.22 μF.
3. Pin 2 must be bypassed with a 0.001-μF capacitor to prevent oscillation for these tests.

electrical characteristics

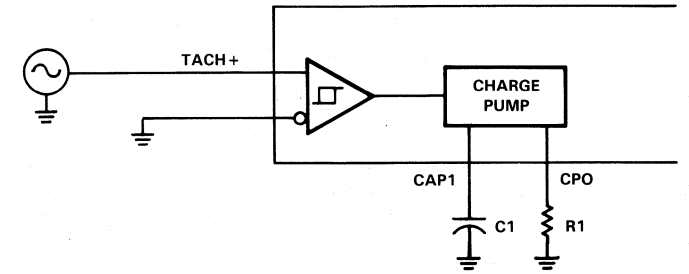
zener regulator (LM2917 only) V+ = 12 V through 470 Ω, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Regulated supply voltage		7.56		V
r_s	Series resistance		10.5	15	Ω
αV_{CC}	Temperature coefficient of regulated supply voltage		1		mV/°C

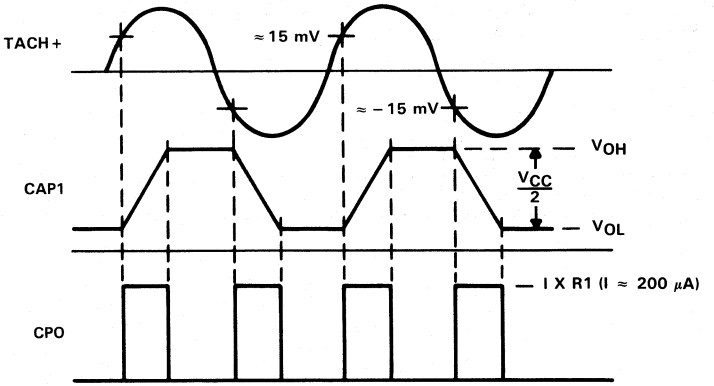
total device (LM2907 only) V_{CC} = 12 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
I_{CC}	Supply current		3.8	6	mA

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

FIGURE 1. TEST CIRCUIT AND WAVEFORMS

4 Special Functions

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

The LM2907 and LM2917 frequency-to-voltage converter circuits are designed for maximum versatility with a minimum of external parts. The first stage of these devices is a differential comparator. The single-input 8-pin versions have one input grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This version is specifically for magnetic variable-reluctance pickups, which typically provide a single-ended ac output. These single-ended inputs are fully protected against voltage swings to ±28 V, which are easily attained by these types of pickups.

The differential-input 14-pin versions provide the option of setting the input reference level and still having hysteresis around that level to provide excellent noise rejection in any application. The input protection is removed in the 14-pin versions. Therefore, neither of the differential inputs should exceed the limits of the supply voltage. An input must not go below ground without a resistance in the lead to limit the current that will flow in the epi-substrate diode. The charge pump circuit that follows the input stage produces a dc output voltage proportional to the input frequency. The charge pump circuit (see Figure 2) consists of a timing capacitor (C1), an output resistor (R1), and an integrating or filter capacitor (C2). When the input changes state (due to a suitable zero crossing or differential voltage on the input), the timing capacitor is either charged or discharged linearly with a constant current of 200 μA through CAP1 between two voltages whose difference is $V_{CC}/2$. Within one-half cycle of the input frequency or a time equal to 1/2f, the change in charge on C1 is equal to (VCC/2)C1. The average amount of current pumped into or out of the capacitor is:

$$\text{CAP1 current (average)} = \frac{Q}{T} = C1 \cdot \frac{V_{CC}}{2} \cdot 2f = V_{CC} \cdot f \cdot C1$$

The output of the charge pump accurately mirrors the CAP1 current into the load resistor (R1) connected to CPO. If the pulses of current are integrated with a filter capacitor, the output voltage is the average CAP1 current times R1, and the total equation becomes:

$$V_O = V_{CC} \cdot f \cdot C1 \cdot R1 \cdot K$$

where K is the gain factor, which is typically 1.

The size of C2 is dependent only on the amount of ripple allowable and the required response time.

selection of R1, C1, and C2

To achieve optimum performance, there are some limitations to be considered in the selection of R1 and C1. The timing capacitor controls the RC time and provides internal compensation for the charge pump circuit. For very accurate operation it should be 100 pF or greater. Smaller values, especially at lower temperatures, can cause an error current through R1. $V_O/R1$ must be less than or equal to the output current at CPO, which is fixed typically at 180 μA. If R1 is too large it becomes a significant fraction of the output impedance at CPO, which degrades the linearity. In addition, ripple voltage must be considered when selecting R1. The size of C2 is directly affected by the size of R1. An expression that describes the ripple content at CPO is:

$$V_{ripple} = \frac{V_{CC}}{2} \cdot \frac{C1}{C2} \cdot \left(1 - V_{CC} \cdot f \cdot \frac{C1}{200}\right) \quad \text{volts peak-to-peak}$$

where

C1 and C2 are in farads
V_{CC} is in volts
f is in hertz.

TYPICAL APPLICATION DATA

R1 cannot be chosen independently of ripple because response time or the time it takes V_O to stabilize at a new level increases as the size of C2 increases. A compromise between ripple, response time, and linearity must be chosen carefully. As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1, and I_{cap} (current through CAP1).

$$f_{max} = \frac{I_{cap}}{C1 \cdot V_{CC}} \quad \text{hertz}$$

where

I_{cap} is typically 200 μA
C1 is in farads
V_{CC} is in volts.

zener regulator options (LM2917)

For those applications in which an output voltage or current must be obtained independently of supply voltage variations, the LM2917 can be used. The most important factor in selecting a dropping resistor for the unregulated supply is that the frequency-to-voltage converter circuit and the operational amplifier alone require approximately 3 mA at the voltage level set by the zener diode. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the supply voltage varies between 9 and 16 V, a resistance of 470 Ω will minimize the zener voltage variation to typically 160 mV. If the resistance goes under 400 Ω or above 600 Ω, the zener variation quickly rises above 200 mV for the same input variation.

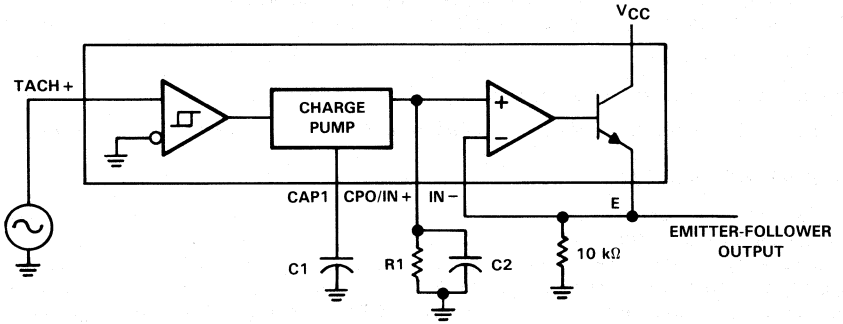

FIGURE 2. MINIMUM-COMPONENT TACHOMETER

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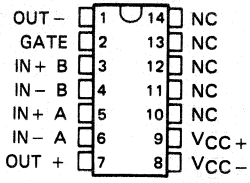
D2572, JANUARY 1980—REVISED APRIL 1988

- **Differential Inputs and Outputs**
- **Channel Select Time . . . 20 ns Typ**
- **Bandwidth Typically 50 MHz**
- **16-dB Minimum Gain**
- **Common-Mode Rejection Typically 85 dB**
- **Broadband Noise Typically 25 μV**

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

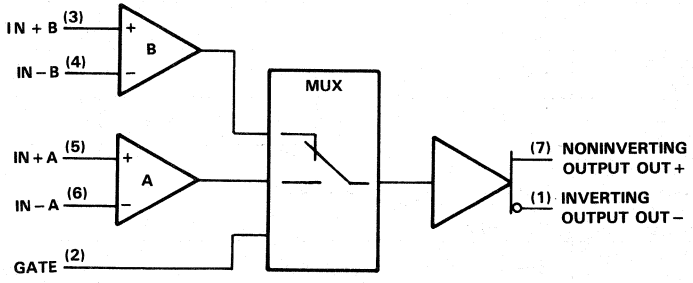
GATE INPUT	SELECT
H	Channel A
L	Channel B

description

The MC1445 is a general-purpose, gated, dual-channel wideband amplifier designed for use in video-signal mixing and switching. Channel selection is accomplished by control of the voltage level at the gate. A high logic level selects channel A; a low logic level selects channel B. The unselected channel will have a gain of one or less.

The MC1445 is characterized for operation from 0°C to 75°C.

block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 12 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −12 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Output current, I_O . . . . . ±25 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values, except differential input voltage, are with respect to the midpoint of V_{CC+} and V_{CC-}.
2. Differential input voltages are measured at a noninverting input terminal with respect to the appropriate inverting input terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 75°C$ POWER RATING
J	626 mW	8.2 mW/°C	74°C	615 mW
N	625 mW	N/A	N/A	625 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		5	8	V
Supply voltage, V_{CC-}		−5	−8	V
Operating free-air temperature range, T_A	0		75	°C

electrical characteristics at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

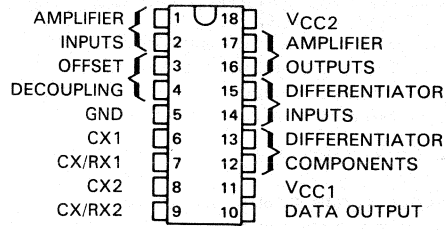
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{VS}	Large-signal single-ended voltage amplification	f = 125 kHz,	V_i = 20 mV	16	19.5	23	dB
BW	Bandwidth	V_i = 20 mV			50		MHz
V_{IO}	Input offset voltage					7.5	mV
I_{IO}	Input offset current				2		μA
I_{IB}	Input bias current				15	30	μA
V_{ICR}	Common-mode voltage range				±2.5		V
V_{OQ}	Quiescent output voltage				0.1		V
ΔV_{OQ}	Change in quiescent output voltage	Gate input change from 5 V to 0 V			±15		mV
V_{OPP}	Maximum peak-to-peak output voltage swing	f = 125 kHz,	R_L = 1 kΩ	1.5	2.5		V
z_i	Input impedance	f = 125 kHz		3	10		kΩ
z_o	Output impedance	f = 50 kHz			25		Ω
CMRR	Common-mode rejection ratio	f = 50 kHz			85		dB
V_n	Broadband equivalent input noise voltage	BW = 5 Hz to 10 MHz, R_S = 50 Ω			25		μV
V_{TH}	High-level gate threshold voltage	$A_{VS(A)} \geq$ 16 dB,	$A_{VS(B)} \leq$ 0 dB		1.3	3	V
V_{TL}	Low-level gate threshold voltage	$A_{VS(B)} \geq$ 16 dB,	$A_{VS(A)} \leq$ 0 dB	0.2	0.4		V
I_{IH}	High-level gate current	V_I = 5 V				4	μA
I_{IL}	Low-level gate current	V_I = 0				4	mA
t_{PLH}	Propagation delay time, low-to-high-level output	ΔV_I = 20 mV,	50% to 50%		6.5		ns
t_{PHL}	Propagation delay time, high-to-low-level output	ΔV_I = 20 mV,	50% to 50%		6.3		ns
t_{TLH}	Transition time, low-to-high-level output	ΔV_I = 20 mV,	10% to 90%		6.5		ns
t_{THL}	Transition time, high-to-low-level output	ΔV_I = 20 mV,	10% to 90%		7		ns
I_{CC+}	Supply current from V_{CC+}	No load,	No signal		7	15	mA
I_{CC-}	Supply current from V_{CC-}	No load,	No signal		−7	−15	mA
P_D	Power dissipation	No load,	No signal		70	150	mW

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2759, NOVEMBER 1983—REVISED FEBRUARY 1988

- **Combines All Read-Amplifier Active Circuitry into One Monolithic Circuit**
- **Peak Shift . . . 2% Max (MC3470A)**
- **Designed to be Interchangeable with Motorola MC3470**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)

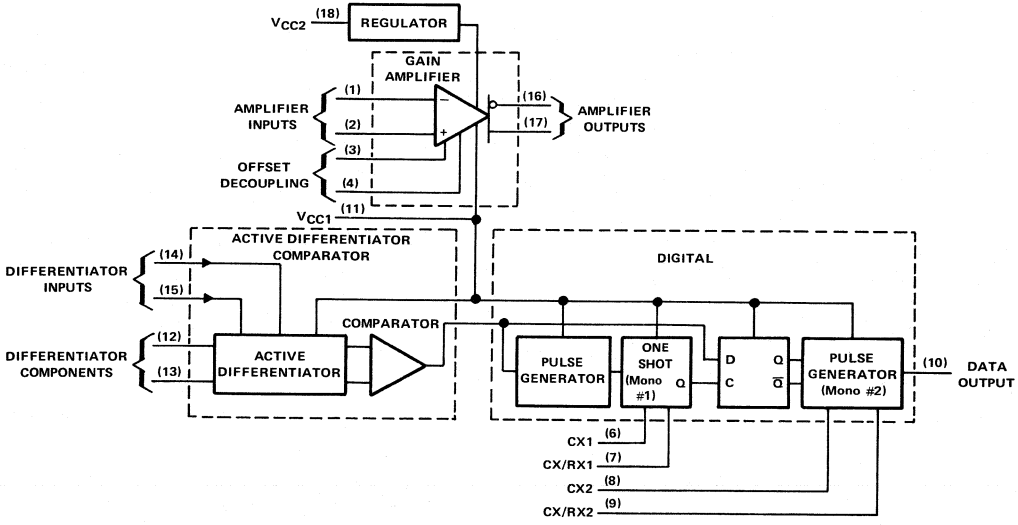


Description

The MC3470 and MC3470A are monolithic read-amplifier systems each containing all the active circuitry necessary for obtaining digital information from floppy disk storage. They are designed to accept the ac differential signal from the magnetic head and produce a digital output pulse corresponding to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

The MC3470 and MC3470A are characterized for operation from 0°C to 70°C.

Functional block diagram



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC2} . . . . . 16 V
Input voltage range (amplifier inputs) . . . . . −0.2 V to 7 V
Output voltage, V_O (data output) . . . . . −0.2 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage V_{CC1}		4.75	5	5.25	V
Supply voltage V_{CC2}		10	12	14	V
Timing capacitor CX1 (see Note 2)		150		680	pF
Timing capacitor CX2		100		800	pF
Timing resistors RX1 and RX2		1.5		10	kΩ
Timing of digital section	Monostable no. 1	500		4000	ns
	Monostable no. 2	150		1000	
Operating free-air temperature, T_A		0		70	°C

NOTE 2: To minimize current transients, CX1 should be kept as small as convenient.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

lectrical characteristics over recommended ranges of supply voltages and operating free-air temperature unless otherwise noted)

ain amplifier section

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
A_{VD}	Differential voltage amplification	MC3470	V_{id} = 5 mV rms,	f = 200 kHz	80	100	120	V/V
		MC3470A			100	110	130	
I_{IB}	Input bias current					−10	−25	μA
V_{ICR}	Common-mode input voltage range		THD ≤ 5%		−0.1 to 1.5			V
V_{IDR}	Differential input voltage range		THD ≤ 5%		±25			mV
V_{OPP}	Peak-to-peak differential output voltage				3	4		V
V_{OC}	Common-mode output voltage		V_I = 0,	V_{ID} = 0		3		V
V_{OD}	Differential output offset voltage		V_I = 0, T_A = 25°C	V_{ID} = 0,			0.4	V
I_{OS}	Short-circuit output current (each amplifier output)		Output shorted to ground			−8		mA
			Output shorted to V_{CC1}		2.8	4		
r_i	Small-signal input resistance		T_A = 25°C		100	250		kΩ
r_o	Small-signal output resistance (single-ended)		V_{CC1} = 5 V, T_A = 25°C	V_{CC2} = 12 V,		15		Ω
BW	Bandwidth (3 dB)		V_{id} = 2 mV rms, V_{CC2} = 12 V,	V_{CC1} = 5 V, T_A = 25°C	5			MHz
CMRR	Common-mode rejection ratio		V_{CC1} = 5 V, A_{VD} = 40 dB, T_A = 25°C	V_{IPP} = 200 mV, f = 100 kHz,	50			dB
k_{SVR}	Supply voltage rejection ratio		A_{VD} = 40 dB, T_A = 25°C	V_{CC1} = 5 ± 0.25 V, V_{CC2} = 12 V	50			dB
				V_{CC1} = 5 V, V_{CC2} = 12 ±2 V	60			
V_n	Equivalent input noise voltage		BW = 10 Hz to 1 MHz, T_A = 25°C			15		μV

All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

active-differentiator section

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{sink}	Sink current at pins 12 and 13		$V_{OD} = V_{CC1}$	1	1.4		mA
	Peak shift	MC3470	V_{CC1} = 5 V, V_{CC2} = 12 V, V_{IDPP} = 1 V, f = 250 kHz, I_{cap} = 500 μA, See Figure 1			5%	
		MC3470A				2%	
r_{id}	Differential input resistance				30		kΩ
r_{od}	Differential output resistance				40		Ω

digital section

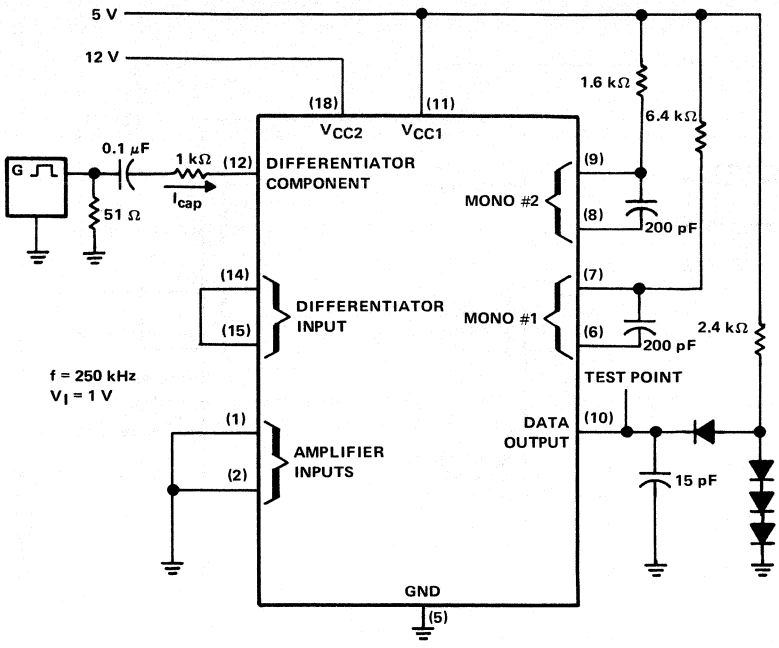
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage (pin 10)	V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = −0.4 mA	2.7			V
V_{OL}	Low-level output voltage (pin 10)	V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8 mA			0.5	V
I_{CC1}	Supply current from V_{CC1}	V_{CC1} = 5.25 V		35	50	mA
I_{CC2}	Supply current from V_{CC2}	V_{CC2} = 14 V		4.5	10	mA

timing characteristics over recommended ranges of supply voltages and operating free-air temperatur (unless otherwise noted) (see Figure 2)

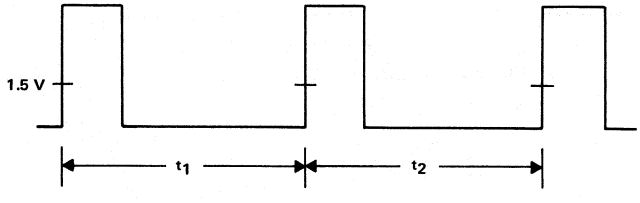
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_r	Rise time (pin 10)				20	ns
t_f	Fall time (pin 10)				25	ns
	Timing accuracy of monostable no. 1 compared to 0.625 RX1 • CX1 + 200 ns	RX1 = 1.5 kΩ to 10 kΩ, CX1 = 150 pF to 680 pF	85%		115%	
	Timing accuracy of monostable no. 2 compared to 0.625 RX2 • CX2	RX2 = 1.5 kΩ to 10 kΩ, CX2 = 100 pF to 800 pF	85%		115%	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 12 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

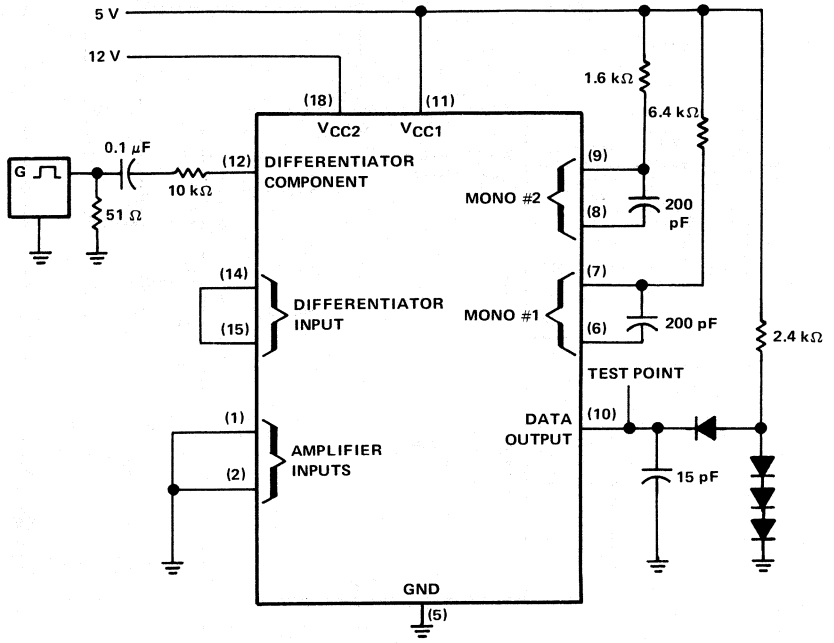


$$\text{Peak shift} = \frac{(t_1 - t_2)}{2\,(t_1 + t_2)} \times 100\%$$

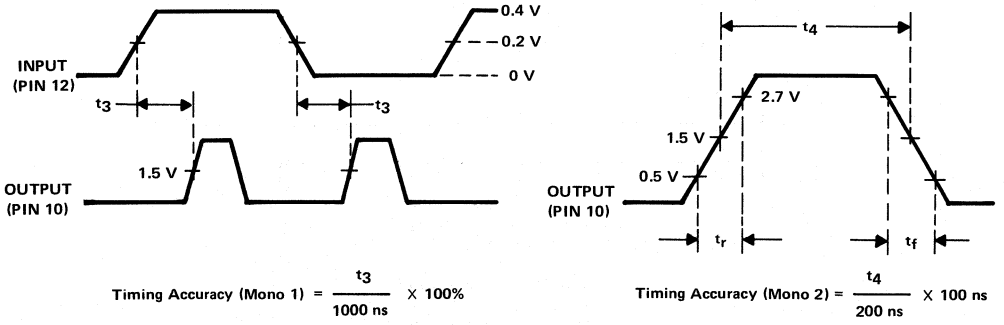
VOLTAGE WAVEFORMS

FIGURE 1. PEAK SHIFT

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



$$\text{Timing Accuracy (Mono 1)} = \frac{t_3}{1000\ \text{ns}} \times 100\%$$

$$\text{Timing Accuracy (Mono 2)} = \frac{t_4}{200\ \text{ns}} \times 100\ \text{ns}$$

VOLTAGE WAVEFORMS

FIGURE 2. TIMING ACCURACY

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TYPICAL CHARACTERISTICS

NORMALIZED POWER SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

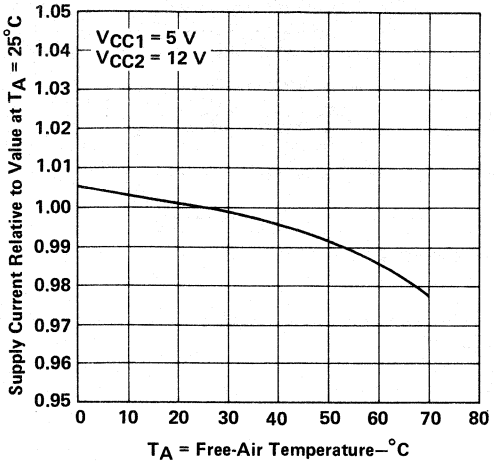

FIGURE 3

NORMALIZED VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

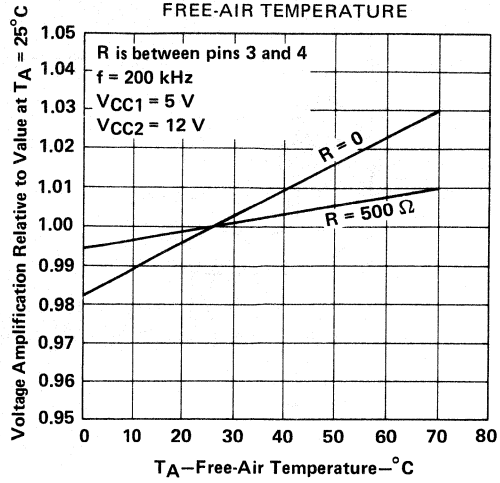

FIGURE 4

NORMALIZED TIME DELAY (PIN 12 TO PIN 10)
vs
FREE-AIR TEMPERATURE

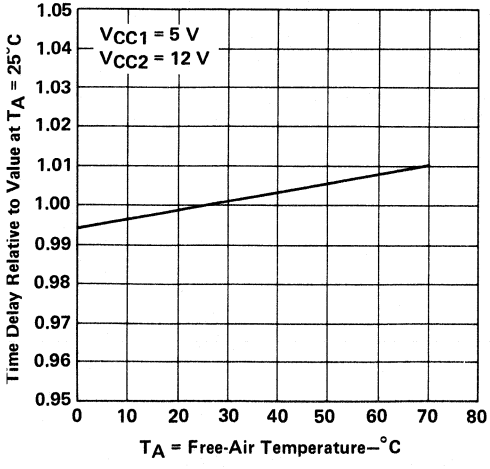

FIGURE 5

VOLTAGE AMPLIFICATION (NORMALIZED)
and PHASE SHIFT
vs
FREQUENCY

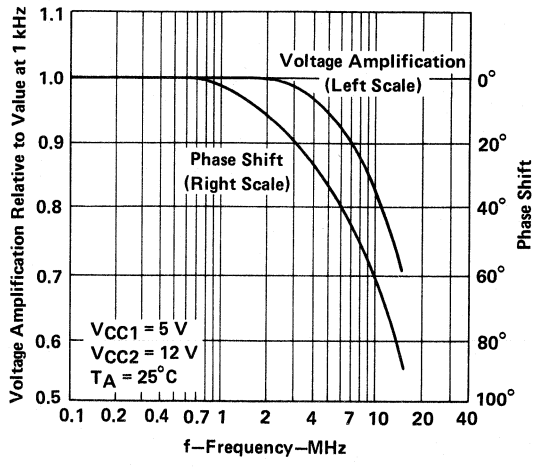

FIGURE 6

TYPICAL APPLICATION INFORMATION

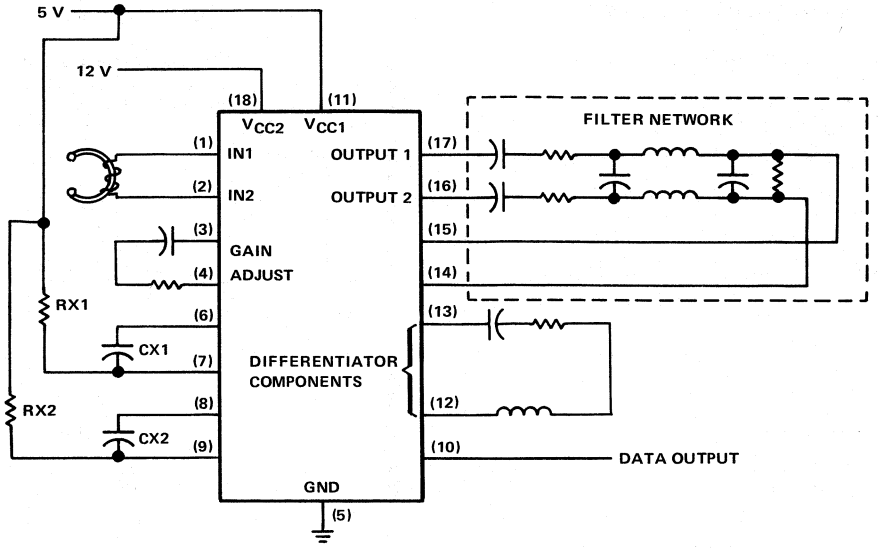

FIGURE 7

TEXAS INSTRUMENTS
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D1669, SEPTEMBER 1973—REVISED OCTOBER 1988

- **Timing from Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source Up to 200 mA**
- **Functionally Interchangeable with the Signetics SE555, SE555C, SA555, NE555; Have Same Pinout**

SE555C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

description

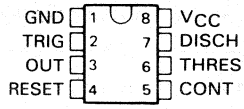
These devices are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

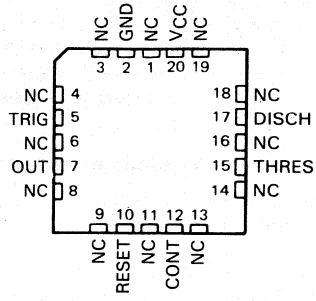
The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

The SE555 and SE555C are characterized for operation over the full military range of −55°C to 125°C. The SA555 is characterized for operation from −40°C to 85°C, and the NE555 is characterized for operation from 0°C to 70°C.

SE555, SE555C . . . JG PACKAGE
SA555, NE555 . . . D, JG, OR P PACKAGE
(TOP VIEW)

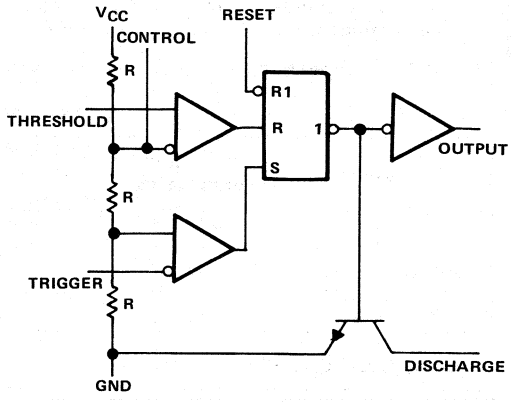


SE555, SE555C . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

functional block diagram



Reset can override Trigger, which can override Threshold.

AVAILABLE OPTIONS

T_A RANGE	V_{thres} MAX V_{CC} = 15 V	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	11.2 V	NE555D		NE555JG	NE555P
−40°C to 85°C	11.2 V	SA555D		SA555JG	SA555P
−55°C to 125°C	10.6 V 11.2 V		SE555FK SE555CFK	SE555JG SE555CJG	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE555DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 18 V
Input voltage (control, reset, threshold, and trigger) . . . . . V_{CC}
Output current . . . . . ±225 mA
Continuous total dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range: SE555, SE555C . . . . . −55°C to 125°C
SA555 . . . . . −40°C to 85°C
NE555 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG (SE555, SE555C)	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
JG (SA555, NE555)	825 mW	6.6 mW/°C	528 mW	429 mW	N/A
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

recommended operating conditions

	SE555		SE555C		SA555		NE555		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at 25 °C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			SE555C, SA555, NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.2		0.1	0.35	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

NOTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is R = R_A + R_B ≈ 3.4 MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE555			SE555C, SA555, NE555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§Values specified are for a device in a monostable circuit similar to Figure 9, with component values as follow: R_A = 2 kΩ to 100 kΩ, C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 12, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

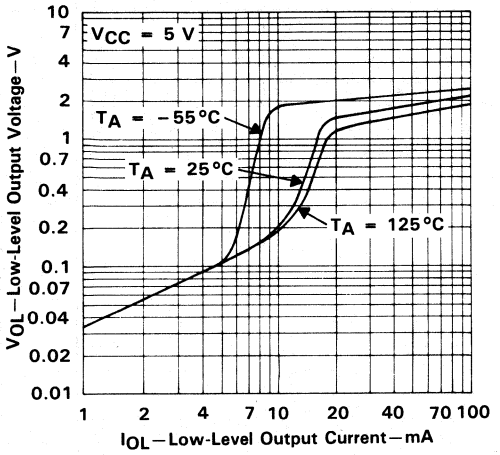


FIGURE 1

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

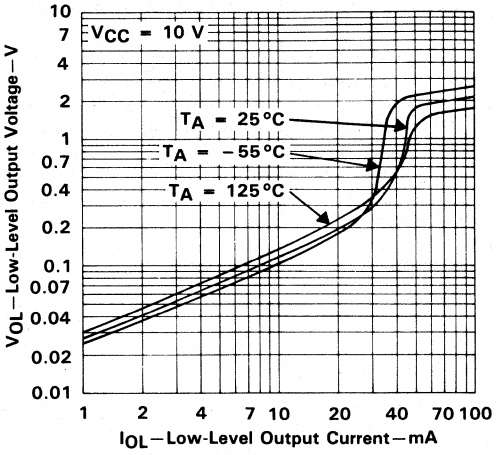


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

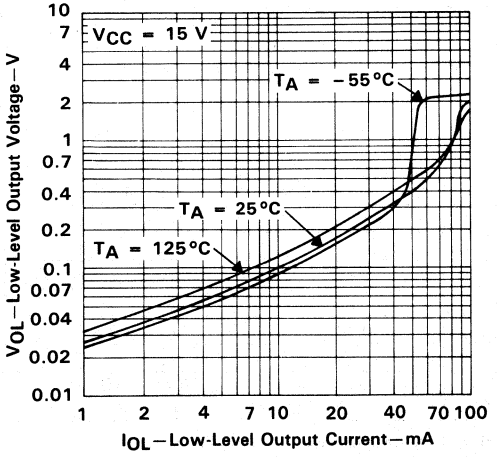


FIGURE 3

DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT

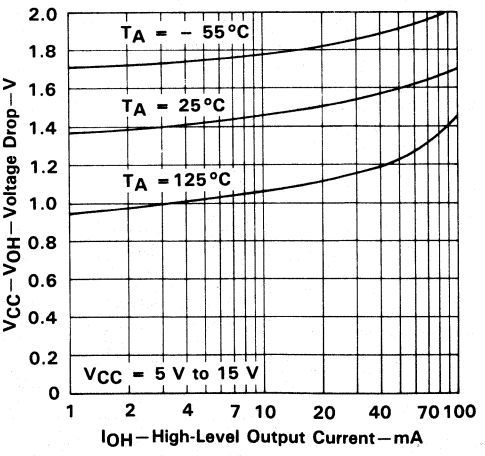


FIGURE 4

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

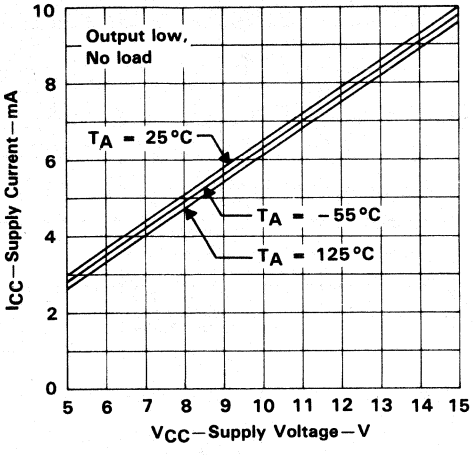

FIGURE 5

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

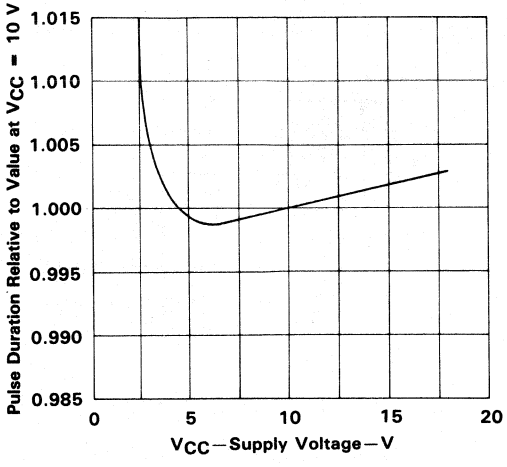

FIGURE 6

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

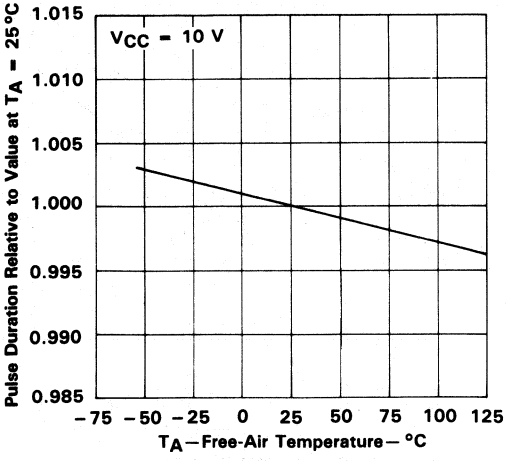

FIGURE 7

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

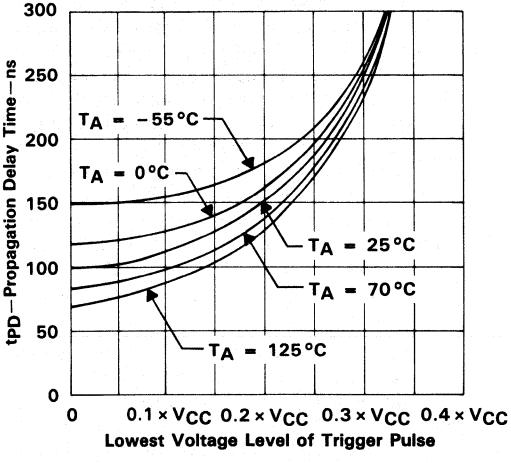

FIGURE 8

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

TYPICAL APPLICATION DATA

monostable operation

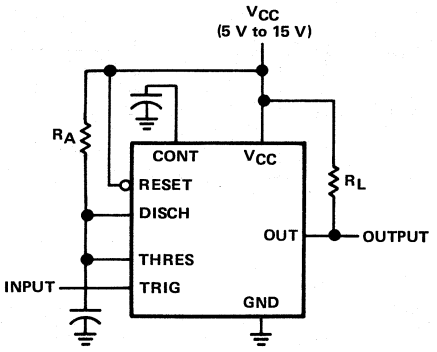

FIGURE 9. CIRCUIT FOR MONOSTABLE OPERATION

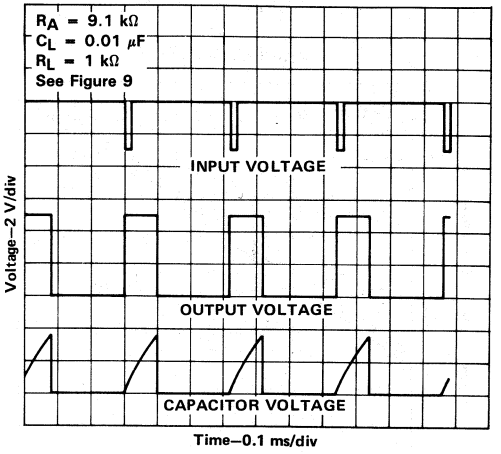

FIGURE 10. TYPICAL MONOSTABLE WAVEFORMS

For monostable operation, any of these timers may be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger input sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C is then charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold input. If the trigger input has returned to a high level, the output of the threshold comparator will reset the flip-flop ($\overline{Q}$ goes high), drive the output low, and discharge C through Q1.

Monostable operation is initiated when the trigger input voltage falls below the trigger threshold. Once initiated, the sequence ends only if the trigger input is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_W = 1.1\ R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates are both directly proportional to the supply voltage, V_{CC}. The timing interval is therefore independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to the reset and trigger terminals during the timing interval discharges C and re-initiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when the reset input is not used, it should be connected to V_{CC}.

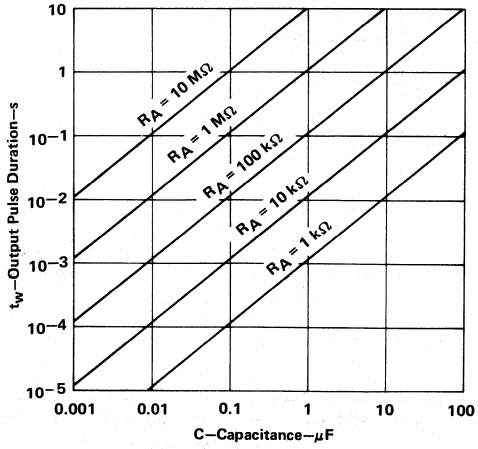

FIGURE 11. OUTPUT PULSE DURATION vs CAPACITANCE

4 Special Functions

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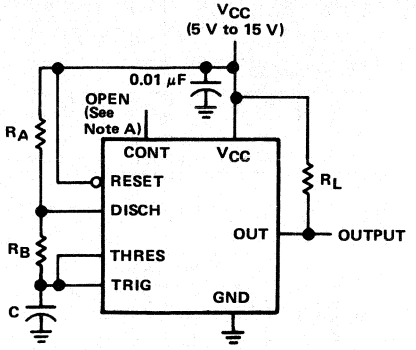
TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 12. CIRCUIT FOR ASTABLE OPERATION

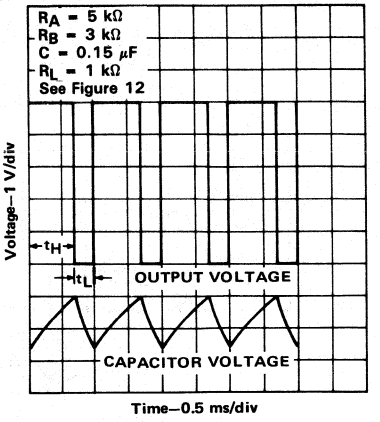


FIGURE 13. TYPICAL ASTABLE WAVEFORMS

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B and then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L may be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$

$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

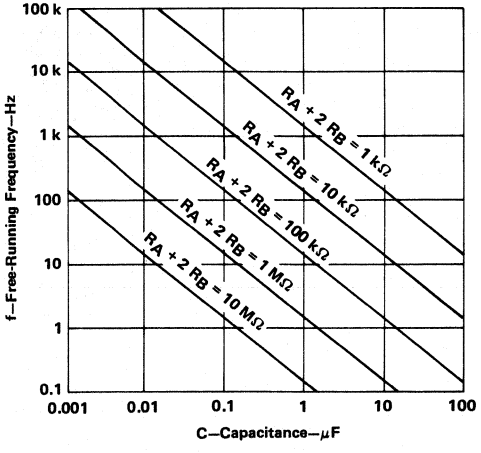


FIGURE 14. FREE-RUNNING FREQUENCY

TYPICAL APPLICATION DATA

missing-pulse detector

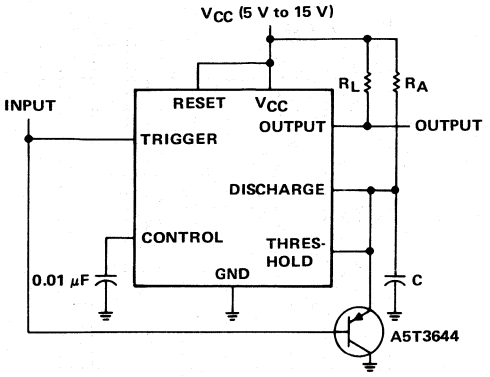


FIGURE 15. CIRCUIT FOR MISSING-PULSE DETECTOR

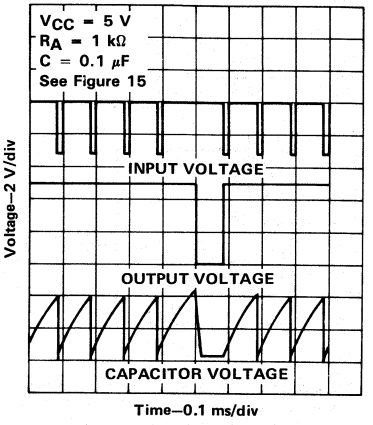


FIGURE 16. MISSING-PULSE DETECTOR WAVEFORMS

The circuit shown in Figure 15 may be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is continuously retriggered by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as illustrated in Figure 16.

frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 illustrates a divide-by-3 circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

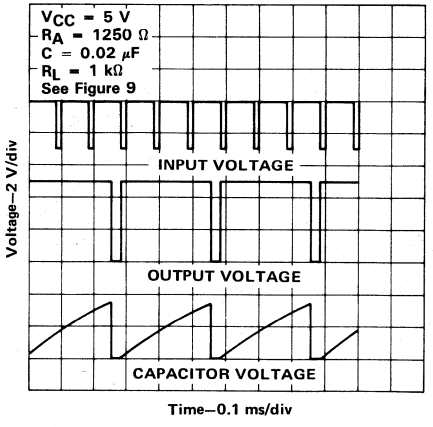


FIGURE 17. DIVIDE-BY-THREE CIRCUIT WAVEFORMS

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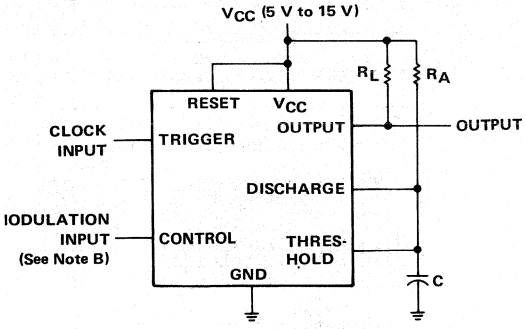
TYPICAL APPLICATION DATA

ulse-width modulation



IOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 18. CIRCUIT FOR PULSE-WIDTH MODULATION

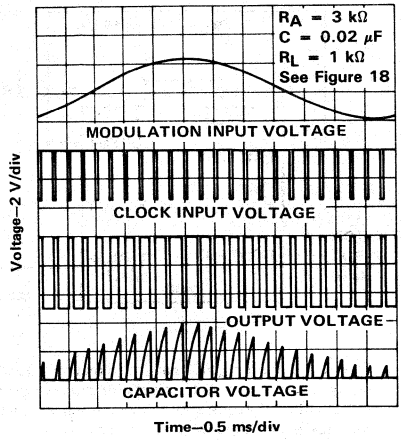
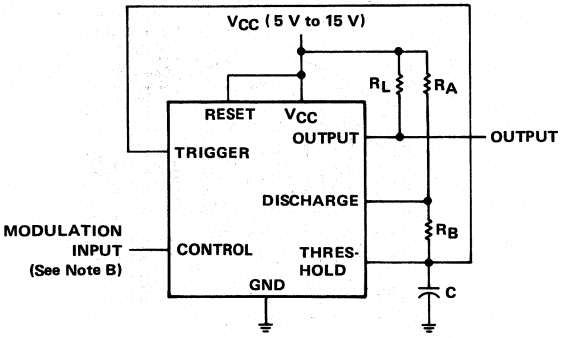


FIGURE 19. PULSE-WIDTH MODULATION WAVEFORMS

The operation of the timer may be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to the control pin. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 illustrates the resulting output pulse-width modulation. While a sine-wave modulation signal is illustrated, any wave shape could be used.

TYPICAL APPLICATION DATA

pulse-position modulation



NOTE B: The modulating signal may be direct or capacitively coupled to the control terminal. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

FIGURE 20. CIRCUIT FOR PULSE-POSITION MODULATION

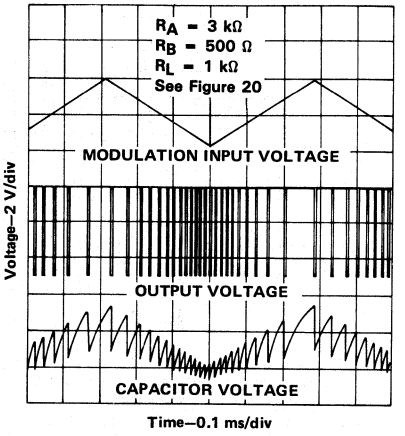


FIGURE 21. PULSE POSITION-MODULATION WAVEFORMS

As shown in Figure 20, any of these timers may be used as a pulse-position modulator. This application modulates the threshold voltage, and thereby the time delay, of a free-running oscillator. Figure 21 illustrates a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

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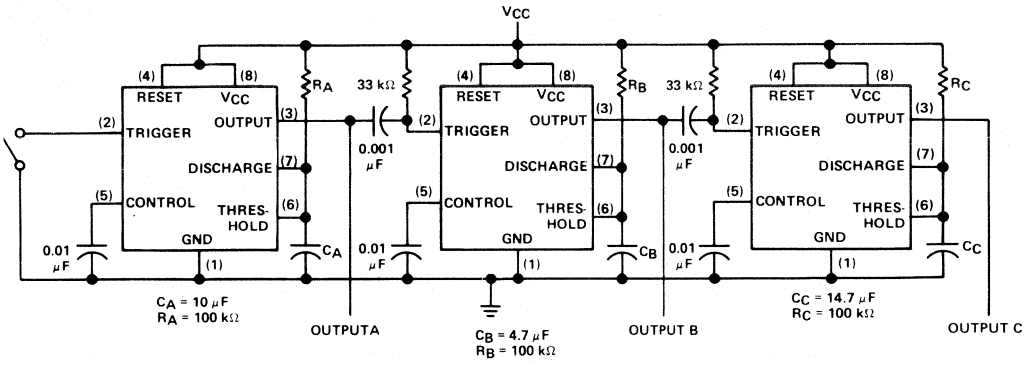
TYPICAL APPLICATION DATA

ıquential timer



closes momentarily at t = 0.

FIGURE 22. SEQUENTIAL TIMER CIRCUIT

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits may be connected to provide such sequential control. The timers may be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 illustrates a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.

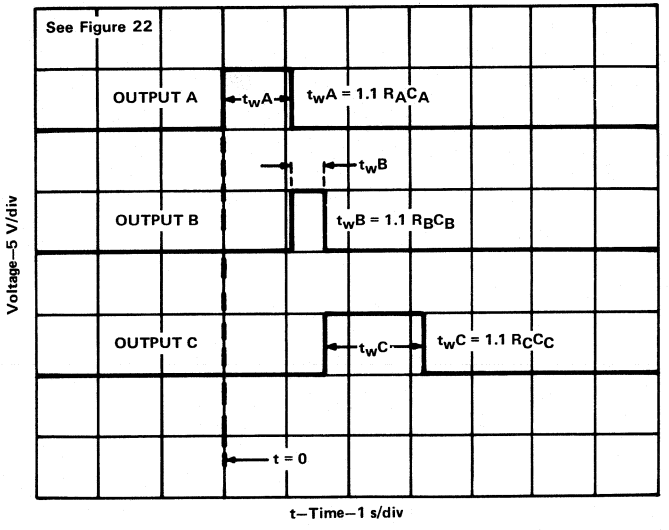


FIGURE 23. SEQUENTIAL TIMER WAVEFORMS

D2440, APRIL 1978—REVISED OCTOBER 1988

- **Two Precision Timing Circuits per Package**
- **Astable or Monstable Operation**
- **TTL-Compatible Output Can Sink or Source Up to 150 mA**
- **Active Pull-Up or Pull-Down**
- **Designed to be Interchangeable with Signetics SE556, SE556C, SA556, NE556**

APPLICATIONS

Precision Timer from Microseconds to Hours	**Sequential Timer**
Pulse-Shaping Circuit	**Pulse Generator**
Missing-Pulse Detector	**Time-Delay Circuit**
Tone-Burst Generator	**Frequency Divider**
Pulse-Width Modulator	**Appliance Timer**
Pulse-Position Modulator	**Industrial Controls**
	Touch-Tone Encoder

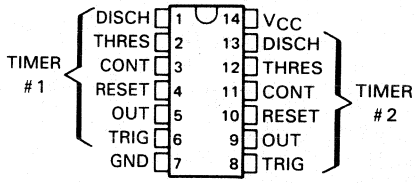
SE556C FROM TI IS NOT RECOMMENDED FOR NEW DESIGNS

scription

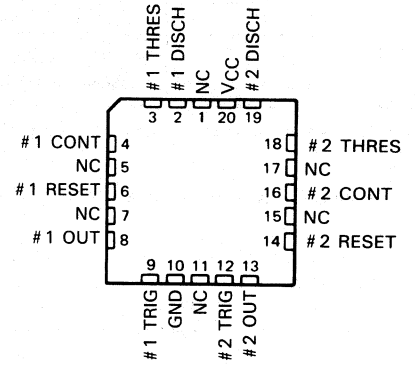
These devices provide two monolithic, independent timing circuits of the SE555, SE555C, SA555, or NE555 type in each package. These circuits can be operated in the astable or the monostable mode with external resistor-capacitor timing control. The basic timing provided by the RC time constant may be actively controlled by modulating the bias of the control voltage input.

The threshold and trigger levels are normally two-thirds and one-third respectively of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below trigger level,, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. Whenever the output is low, a low impedance path is provided between the discharge terminal and ground.

SE556, SE556C . . . J PACKAGE
SA556, NE556 . . . D, J, OR N PACKAGE
(TOP VIEW)

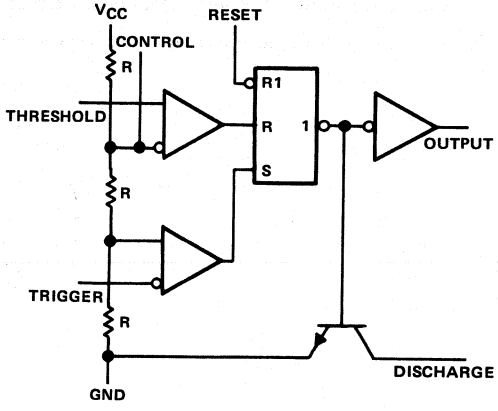


SE556, SE556C . . . FK PACKAGE
(TOP VIEW)



NC—No internal correction

functional block diagram (each timer)



Reset can override Trigger, which can override Threshold.

4 Special Functions

The SE556 and SE556C are characterized for operation over the full military range of −55°C to 125°C. The SA556 is characterized for operation from −40°C to 85°C, and the NE556 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A RANGE	V_{thres} MAX V_{CC} = 15 V	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	11.2 V	NE556D		NE556J	NE556N
−40°C to 85°C	11.2 V	SA556D		SA556J	SA556N
−55°C to 125°C	10.6 V 11.2 V		SE556FK SE556CFK	SE556J SE556CJ	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., NE556DR).

FUNCTION TABLE

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARG SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	< 1/3 V_{DD}	Irrelevant	High	Off
High	> 1/3 V_{DD}	> 2/3 V_{DD}	Low	On
High	> 1/3 V_{DD}	< 2/3 V_{DD}	As previously established	

†Voltage levels shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) 18
Input voltage (control, reset, threshold, and trigger) . . . . . V_C
Output current . . . . . ±225 m
Continuous total dissipation . . . . . see Dissipation Rating Tab
Operating free-air temperature range: SE556, SE556C . . . . . −55°C to 125°
SA556 . . . . . −40°C to 85°
NE556 . . . . . 0°C to 70°
Storage temperature range . . . . . −65°C to 150°
Case temperature for 60 seconds: FK package . . . . . 260°
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SE556, SE556C)	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J (SA556, NE556)	1025 mW	8.2 mW/°C	656 mW	533 mW	N/A
N	1575 mW	12.6 mW/°C	1008 mW	819 mW	N/A

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ecommended operating conditions

	SE556		SE556C		SA556		NE556		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	4.5	18	4.5	16	4.5	16	4.5	16	V
Input voltage (control, reset, threshold, and trigger)		V_{CC}		V_{CC}		V_{CC}		V_{CC}	V
Output current		±200		±200		±200		±200	mA
Operating free-air temperature, T_A	−55	125	−55	125	−40	85	0	70	°C

lectrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
Threshold current (see Note 2)				30	250		30	250	nA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
Trigger current	Trigger at 0 V			0.5	0.9		0.5	2	μA
Reset voltage level			0.3	0.7	1	0.3	0.7	1	V
Reset current	Reset at V_{CC}			0.1	0.4		0.1	0.4	mA
	Reset at 0 V			−0.4	−1		−0.4	−1.5	
Discharge switch off-state current				20	100		20	100	nA
Control voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.15		0.1	0.25	
		I_{OL} = 8 mA		0.15	0.25		0.15	0.3	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		20	24		20	30	mA
		V_{CC} = 5 V		6	10		6	12	
	Output high, No load	V_{CC} = 15 V		18	20		18	26	
		V_{CC} = 5 V		4	8		4	10	

OTE 2: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 1. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \approx 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is ≈ 10 MΩ.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER		TEST CONDITIONS†	SE556			SE556C, SA556, NE556			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A = 25°C		0.5	1.5		1	3	%
	Each timer, astable¶			1.5			2.25		
	Timer 1 — Timer 2			±0.5			±1		
Temperature coefficient of timing interval	Each timer, monostable§	T_A = MIN to MAX		30	100		50		ppm/°C
	Each timer, astable¶			90			150		
	Timer 1 — Timer 2			±10			±10		
Supply voltage sensitivity of timing interval	Each timer, monostable§	T_A = 25°C		0.05	0.2		0.1	0 5	%/V
	Each timer, astable¶			0.15			0.3		
	Timer 1 — Timer 2			±0.1			±0.2		
Output pulse rise time		C_L = 15 pF, T_A = 25°C		100	200		100	300	ns
Output pulse fall time				100	200		100	300	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each proces run.
§Values specified are for a device in a monostable circuit similar to Figure 2, with component values as follow: R_A = 2 kΩ to 100 kΩ C = 0.1 μF.
¶Values specified are for a device in an astable circuit similar to Figure 1, with component values as follow: R_A = 1 kΩ to 100 kΩ, C = 0.1 μF

TYPICAL APPLICATION DATA

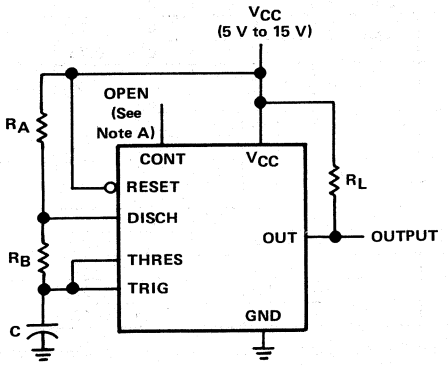


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

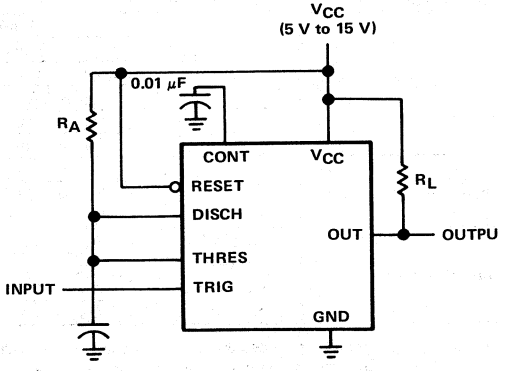


FIGURE 2. CIRCUIT FOR MONOSTABLE OPERATIO

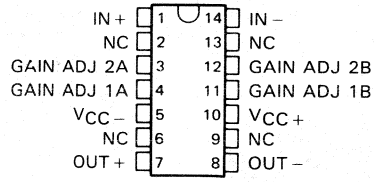
NOTE A: Bypassing the control voltage input to ground with a capacitor may improve operation. This should be evaluated for individual applications.

D2667, FEBRUARY 1984—REVISED FEBRUARY 1988

- **90-MHz Bandwidth**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Passband**
- **Designed to be Interchangeable with Signetics SE592 and NE592**

DEVICE TYPE	TEMPERATURE RANGE	A_{VD} RANGE (GAIN OPTION 1)
SE592	−55°C to 125°C	300—500
NE592	0°C to 70°C	250—600
NE592A	0°C to 70°C	400—600

NE592, NE592A . . . D OR N PACKAGE
SE592 . . . J PACKAGE
(TOP VIEW)



NC—No internal connection

Description

These devices are monolithic two-stage amplifiers with differential inputs and differential outputs.

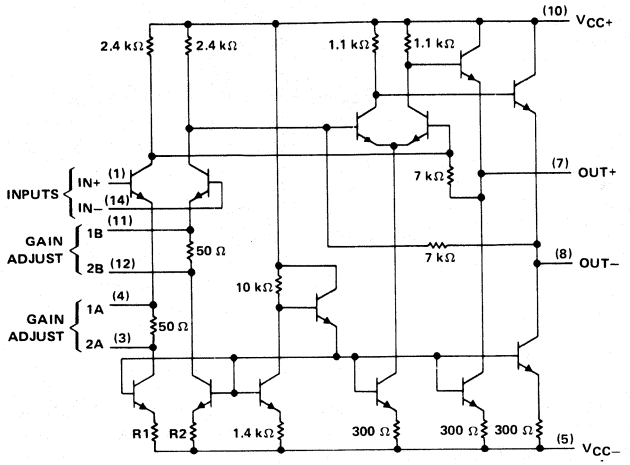
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the devices to drive capacitive loads, and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 100 or 400 may be selected without external components; or amplification may be adjusted from 0 to 400 by the use of a single external resistor connected between the gain-adjustment pins 1A and 1B. External frequency-compensating components are not required for any gain option.

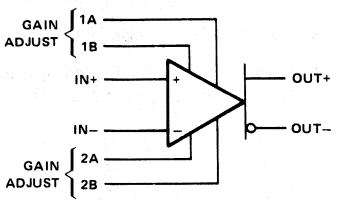
The devices are particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The SE592 is characterized for operation over the full military temperature range of −55°C to 125°C. The NE592 and NE592A are characterized for operation from 0°C to 70°C.

schematic



symbol



All resistor values shown are in ohms and nominal.
In NE592 or SE592, R1 = 500 Ω, R2 = 500 Ω.
In NE592A, R1 = 600 Ω, R2 = 600 Ω.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	8 V
Supply voltage V_{CC-} (see Note 1)	−8 V
Differential input voltage	±5 V
Common-mode input voltage	±6 V
Output current	10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range: SE592	−55°C to 125°C
NE592, NE592A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	
J	500 mW	11 mW/°C	105°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

recommended operating conditions

	SE592			NE592 NE592A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC+}	3	6	8	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	−3	−6	−8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592			UNIT
					MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	300	400	500	V/V
				2	90	100	110	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40		MHz
				2		90		
I_{IO}	Input offset current			1, 2, or 3		0.4	3	μA
I_{IB}	Input bias current			1, 2, or 3		9	20	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1, 2, or 3	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{IO} = 0, R_L = ∞	1			1.5	V
				2			1	
				3		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		V
r_i	Input resistance			1		4		kΩ
				2	20	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5		ns
				2		4.5	10	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24	mA

The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	SE592 MIN	SE592 TYP	SE592 MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V	1	200		600	V/V
				2	80		120	
I_{IO}	Input offset current			1 or 2			5	µA
I_{IB}	Input bias current			1 or 2			40	µA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1			1.5	V
				2			1.2	
				3			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.5			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	2.5			mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B; pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B; pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

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electrical characteristics at 25°C operating free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ	1	250	400	600	400	440	600	V/V
				2	80	100	120	80	100	120	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V	1		40			40		MHz
				2		90			90		
I_{IO}	Input offset current		V_{IC} = 0	1, 2, or 3		0.4	5		0.4	5	μA
I_{IB}	Input bias current		V_{IC} = 0	1, 2, or 3		9	30		10	30	μA
V_{ICR}	Common-mode input voltage range	3		1, 2, or 3	±1			±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3		0.35	0.75		0.35	0.75	
V_{OPP}	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1, 2, or 3	3	4		3	4		V
r_i	Input resistance			1		4			4		kΩ
				2	10	30		10	30		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance					2			2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	60	86		60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60			60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz	1, 2, or 3		12			12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V	1		7.5			7.5		ns
				2		6	10		6	10	
t_r	Rise time	2	ΔV_O = 1 V	1		10.5			10.5		ns
				2		4.5	12		4.5	12	
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3	3	4		3	4		mA
I_{CC}	Supply current		No load, No signal	1, 2, or 3		18	24		19	24	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	NE592			NE592A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large signal differential voltage amplification	1	V_{OPP} = 3 V	1	250		600	400		600	V/V
				2	80		120	80		120	
I_{IO}	Input offset current			1 or 2			6			6	μA
I_{IB}	Input bias current			1 or 2			40			40	μA
V_{ICR}	Common-mode input voltage range	3		1 or 2	±1			±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5			1.5	V
				3			1			1	
V_{OPP}	Maximum output voltage peak-to-peak swing	1	R_L = 2 kΩ	1 or 2	2.8			2.8			V
r_i	Input resistance			2	8			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	2	50			50			dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			50			dB
$I_{sink(max)}$	Maximum output sink current			1, 2, or 3				2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1, 2, or 3			27			27	mA

†The gain option is selected as follows:
Gain Option 1 . . Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2 . . Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.
Gain Option 3 . . All Gain Adjust pins are open.

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PARAMETER MEASUREMENT INFORMATION

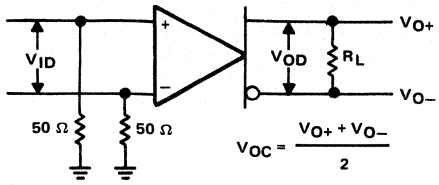


FIGURE 1

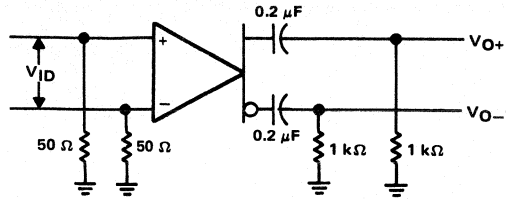


FIGURE 2

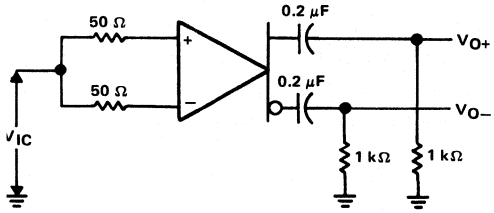


FIGURE 3

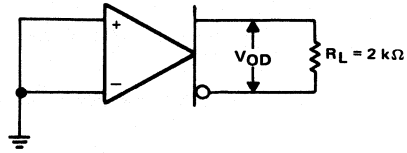
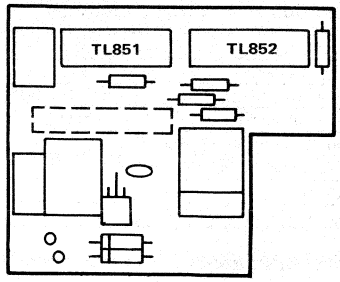


FIGURE 4

D2780, OCTOBER 1983—REVISED MARCH 1988

- **Accurate Sonar Ranging from 6 Inches to 35 Feet**
- **Drives 50-kHz Electrostatic Transducer with No Additional Interface**
- **Operates from Single Supply**
- **Accurate Clock Output Provided for External Use**
- **Selective Echo Exclusion**
- **TTL-Compatible**
- **Multiple Measurement Capability**
- **Uses TL851 and TL852 Sonar Ranging Integrated Circuits**



See schematic, Figure 4, for terminal assignments.

Description

The SN28827 is an economical sonar ranging module that can drive a 50-kHz, 300-V electrostatic transducer with no additional interface. This module, with a simple interface, is able to measure distances of from 6 inches to 35 feet. The typical absolute accuracy is ±2% at one foot or greater.

This module has an external blanking input that allows selective echo exclusion for operation in a multiple-echo mode. The module is able to differentiate echos from objects that are only three inches apart. The digitally controlled-gain, variable-bandwidth amplifier minimizes noise and sidelobe detection in sonar applications.

The module has an accurate ceramic-resonator-controlled 420-kHz time-base generator. An output based on the 420-kHz time base is provided for external use. The sonar transmit output is 16 pulses at a frequency of 49.4 kHz.

The SN28827 operates over a supply voltage range of from 4.5 V to 6.8 V and is characterized for operation from 0°C to 40°C.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage from any pin to ground (see Note 1)	7 V
Voltage from any pin except XDCR to V_{CC} (see Note 1)	−7 V to 0.5 V
Operating free-air temperature range	0°C to 40°C
Storage temperature range	−40°C to 85°C

NOTE 1: The XDCR pin may be driven from −1 V to 300 V typical with respect to ground.

recommended operating conditions

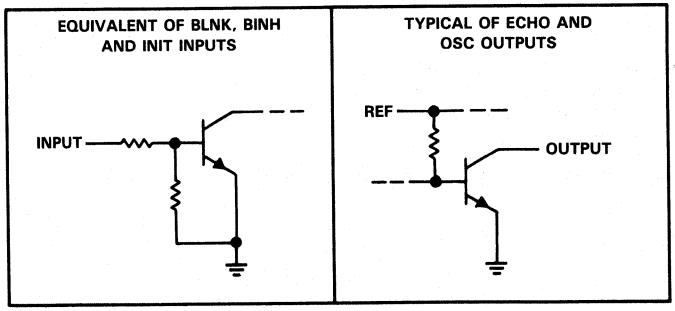
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
ECHO and OSC output voltage			6.8	V
Delay time, power up to INIT high		5		ms
Recycle period		80		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC	I_{OL} = 1.6 mA			0.4	V
Transducer bias voltage				150		V
Transducer output voltage (peak-to-peak)				300		V
Number of cycles for XDCR output to reach 300 V		C = 500 pF			7	
Internal blanking interval		See Note 2		2.38		ms
Frequency during 16-pulse transmit period	OSC output	See Note 2		49.4		kHz
	XMIT output			49.4		
Frequency after 16-pulse transmit period	OSC output	See Note 2		93.3		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				2000	mA
	After transmit period				100	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 2: These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



operation with Polaroid electrostatic transducer

There are two basic modes of operation for the SN28827 Sonar ranging module: single-echo mode and multiple-echo mode. The application of power (V_{CC}), the activation of the Initiate (INIT) input, and the resulting transmit output, and the use of the Blanking Inhibit (BINH) input are basically the same for either mode of operation. After applying power (V_{CC}), a minimum of 5 ms must elapse before the INIT input can be taken high. During this time, all internal circuitry is reset and the internal oscillator stabilizes. When INIT is taken high, drive to the Transducer (XDCR) output occurs. Sixteen pulses at 49.4 kHz with 300-V amplitude will excite the transducer as transmission occurs. At the end of the 16 transmit pulses, a dc bias of 150 V will remain on the transducer as recommended for optimum operation by the transducer manufacturer.

In order to eliminate ringing of the transducer from being detected as a return signal, the receive (REC) input of the ranging control IC is inhibited by internal blanking for 2.38 ms after the initiate signal. If a reduced blanking time is desired, then the BINH input can be taken high to end the blanking of the Receive input anytime prior to internal blanking. This may be desired to detect objects closer than 1.33 feet corresponding to 2.38 ms and may be done if transducer damping is sufficient that ringing is not detected as a return signal.

In the single-echo mode of operation (Figure 1), all that must be done next is to wait for the return of the transmitted signal, traveling at approximately 0.9 ms per foot out and back. The returning signal is amplified and appears as a high-logic-level echo output. The time between INIT going high and the echo (ECHO) output going high is proportional to the distance of the target from the transducer. If desired, the cycle can now be repeated by returning INIT to a low-logic level and then taking it high when the next transmission is desired.

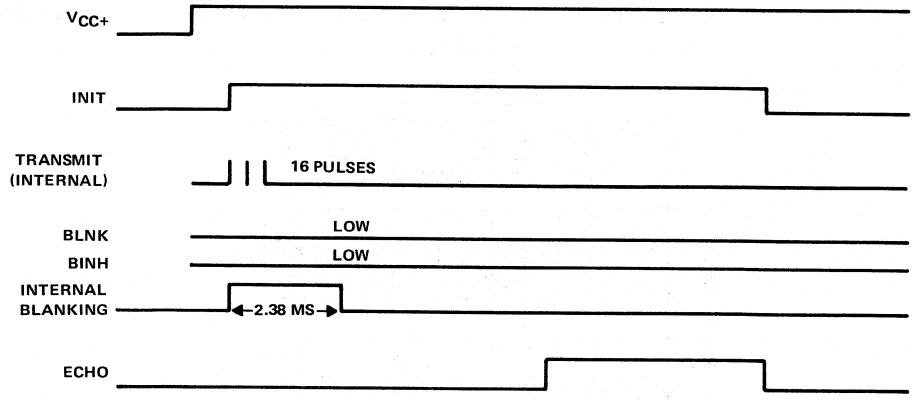


FIGURE 1. EXAMPLE OF A SINGLE-ECHO-MODE CYCLE WITHOUT BLANKING INPUT

If there is more than one target and multiple echos are to be detected from a single transmission, then the cycle is slightly different (Figure 2). After receiving the first return signal, which causes the ECHO output to go high, the Blanking (BLNK) input must be taken high then back low to reset the Echo output for the next return signal. The blanking signal must be at least 0.44 ms in duration to account for all 16 returning pulses from the first target and allow for internal delay times. This corresponds to the two targets being 3 inches apart.

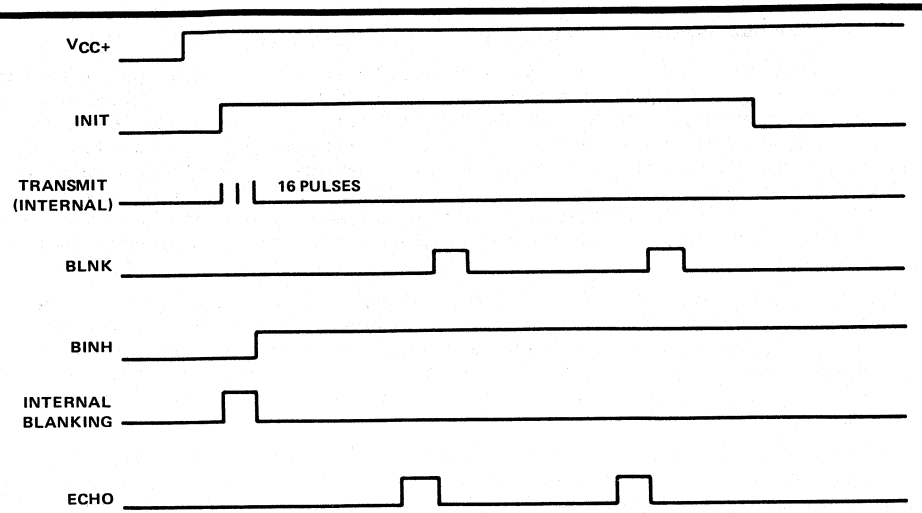


FIGURE 2. EXAMPLE OF A MULTIPLE-ECHO-MODE CYCLE WITH BLANKING INPUT

During a cycle starting with INIT going high, the receiver amplifier gain is incremented higher at discrete times (Figure 3) since the transmitted signal is attentuated with distance. At approximately 38 ms, the maximum gain is attained. For this reason, sufficient gain may not be available for objects greater than

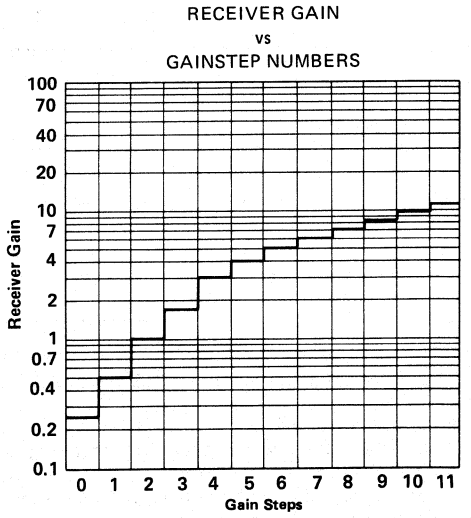
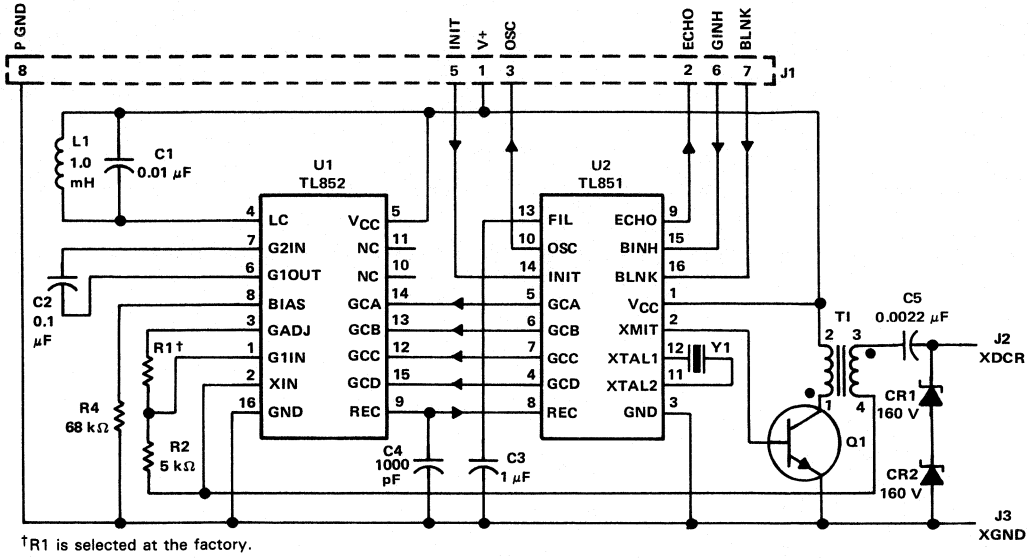


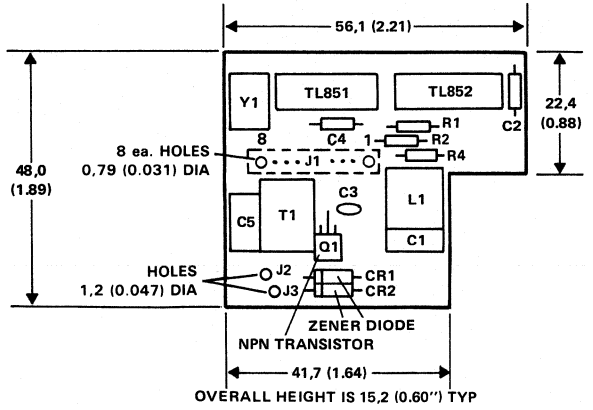
FIGURE 3

35 feet away. Although gain can be increased by varying R1 (Figure 4), there is a limit to which the gain can be increased for reliable module operation. This will vary from application to application. The modules are "kitted" prior to their final test during manufacture. This is necessary because the desired gain distribution is much narrower than the module gain distribution if all were kitted with one value resistor. As kitted, these modules will perform satisfactorily in most applications. As a rule of thumb, the gain can be increased by up to a factor of 4, if required, by increasing R1 correspondingly. Gain is directly proportional to R1.



†R1 is selected at the factory.

FIGURE 4. SCHEMATIC

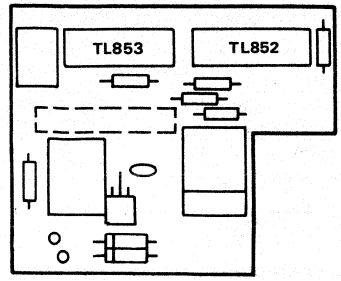


NOTE: All dimensions are in millimeters and parenthetically in inches.

FIGURE 5. COMPONENT LAYOUT AND DIMENSIONS OF MODULE

D2842, JANUARY 1985

- **Accurate Sonar Ranging from 6 Inches to 35 Feet**
- **Drives 40-kHz Piezoelectric Transducer**
- **Operates from Single Supply**
- **Accurate Clock Output Provided for External Use**
- **Selective Echo Exclusion**
- **TTL-Compatible**
- **Multiple Measurement Capability**
- **Uses TL852 and TL853 Sonar Ranging Integrated Circuits**



See schematic, Figure 4, for terminal assignments.

description

The SN28828 is an economical sonar ranging module that can drive a 40-kHz piezoelectric transducer with no additional interface. This module, with a simple interface, is able to measure distances ranging from 6 inches to 35 feet. The typical absolute accuracy is ±2% at one foot or greater.

This module has an external blanking input that allows selective echo exclusion for operation in a multiple-echo mode. The module is able to differentiate echos from objects that are only 3.5 inches apart. The digitally controlled-gain, variable-bandwidth amplifier minimizes noise and side-lobe detection in sonar applications.

The module has an accurate ceramic-resonator-controlled 420-kHz time-base generator. An output based on the 420-kHz time base is provided for external use. The sonar transmit output is 16 pulses at a frequency of 40 kHz.

The SN28828 operates over a supply voltage range of from 4.5 V to 6.8 V and is characterized for operation from 0°C to 40°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage from any pin to ground (see Note 1)	7 V
Voltage from any pin except XDCR to V_{CC} (see Note 1)	−7 V to 0.5 V
Operating free-air temperature range	0°C to 40°C
Storage temperature range	−40°C to 85°C

NOTE 1: The XDCR pin may be driven to ±35 V typical with respect to ground.

recommended operating conditions

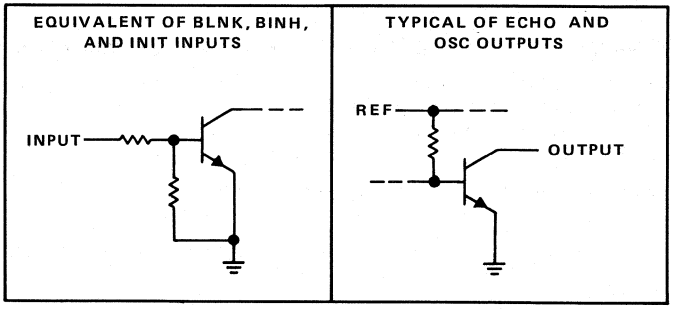
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
ECHO and OSC output voltage			6.8	V
Delay time, power up to INIT high		5		ms
Recycle period		80		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC	I_{OL} = 1.6 mA			0.4	V
Transducer output voltage (peak-to-peak)				70		V
Internal blanking interval		See Note 2		2.46		ms
Frequency during 16-pulse transmit period	OSC output	See Note 2		40		kHz
	XMIT output			40		
Frequency after 16-pulse transmit period	OSC output	See Note 2		93.3		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				350	mA
	After transmit period				100	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 2: These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

›peration with 40-kHz piezoelectric transducer

There are two basic modes of operation for the SN28828 Sonar ranging module: single-echo mode and multiple-echo mode. The application of power (V_{CC}), the activation of the Initiate (INIT) input and the resulting transmit output, and the use of the Blanking Inhibit (BINH) input are basically the same for either mode of operation. After applying power (V_{CC}), a minimum of 5 ms must elapse before the INIT input can be taken high. During this time, all internal circuitry is reset and the internal oscillator stabilizes. When INIT is taken high, drive to the Transducer (XDCR) output occurs. Sixteen pulses at 40 kHz with 70-V peak-to-peak amplitude will excite the transducer as transmission occurs.

In order to eliminate ringing of the transducer from being detected as a return signal, the Receive (REC) input of the ranging control IC is inhibited by internal blanking for 2.46 ms after the initiate signal. If a reduced blanking time is desired, then the BINH input can be taken high to end the blanking of the Receive input anytime prior to internal blanking. This may be desired to detect objects closer than 1.37 feet corresponding to 2.46 ms and may be done if transducer damping is sufficient that ringing is not detected as a return signal.

In the single-echo mode of operation (Figure 1), all that must be done next is to wait for the return of the transmitted signal, traveling at approximately 0.9 ms per foot out and back. The returning signal is amplified and appears as a high-logic-level echo output. The time between INIT going high and the Echo (ECHO) output going high is proportional to the distance of the target from the transducer. If desired, the cycle can now be repeated by returning INIT to a low-logic level and then taking it high when the next transmission is desired.

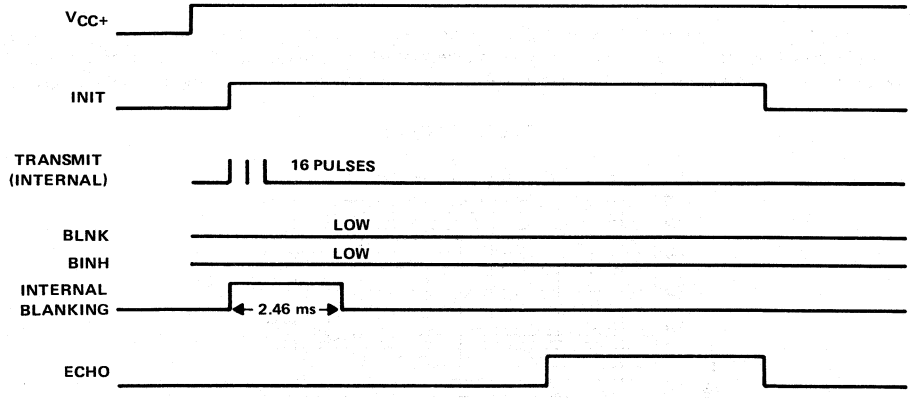


FIGURE 1. EXAMPLE OF A SINGLE-ECHO-MODE CYCLE WITHOUT BLANKING INPUT

If there is more than one target, and multiple echos are to be detected from a single transmission, then the cycle is slightly different (Figure 2). After receiving the first return signal, which causes the ECHO output to go high, the Blanking (BLNK) input must be taken high then back low to reset the Echo output for the next return signal. The blanking signal must be at least 0.52 ms in duration to account for all 16 returning pulses from the first target and allow for internal delay times. This corresponds to the two targets being 3.5 inches apart.

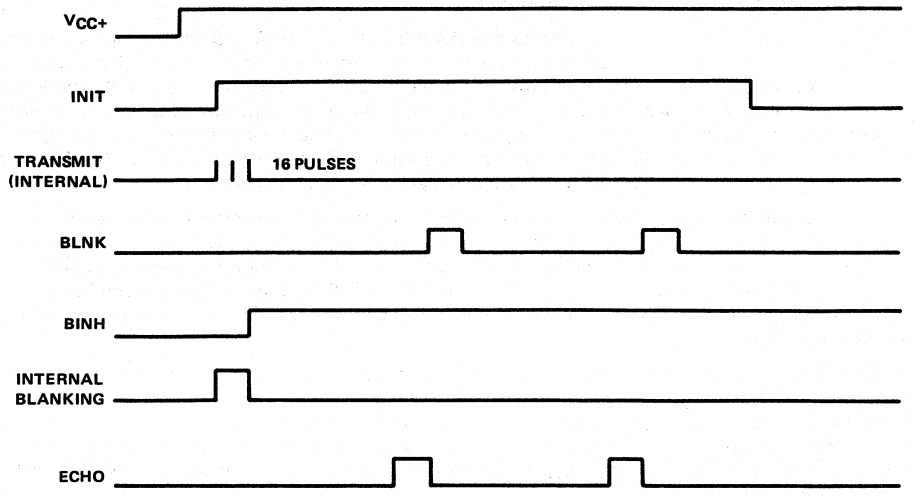


FIGURE 2. EXAMPLE OF A MULTIPLE-ECHO-MODE CYCLE WITH BLANKING INPUT

During a cycle starting with INIT going high, the receiver amplifier gain is incremented higher at discrete times (Figure 3) since the transmitted signal is attenuated with distance. At approximately 38 ms, the maximum gain is attained. For this reason, sufficient gain may not be available for objects greater than

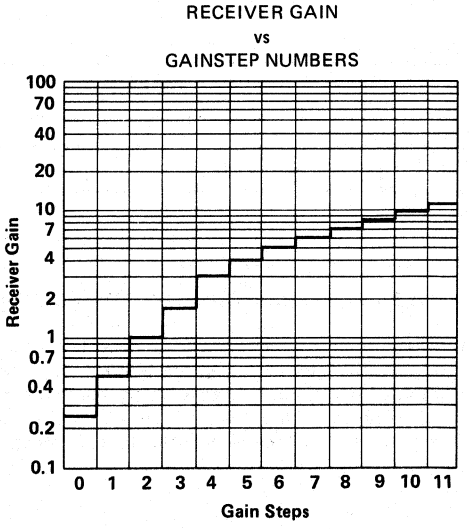


FIGURE 3

TEXAS INSTRUMENTS
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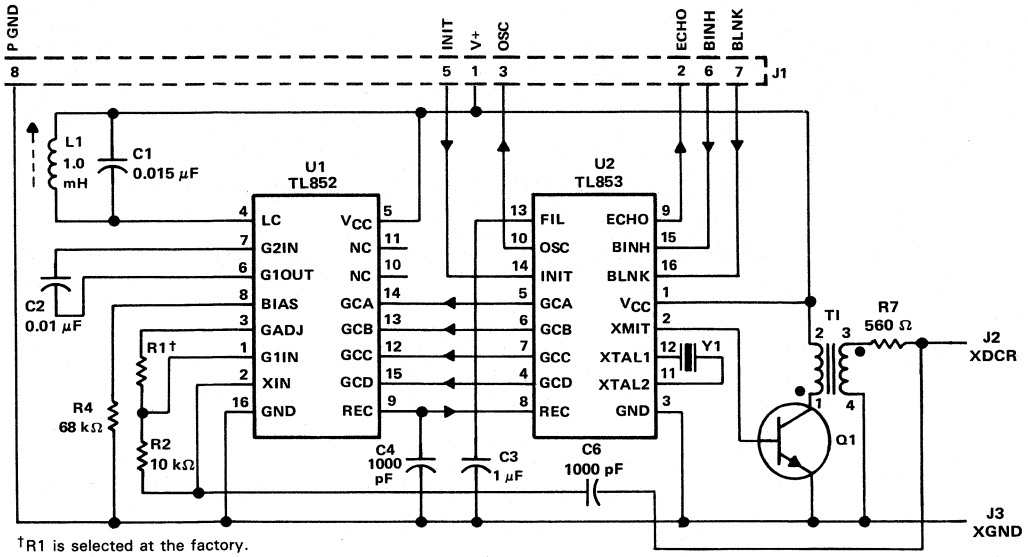
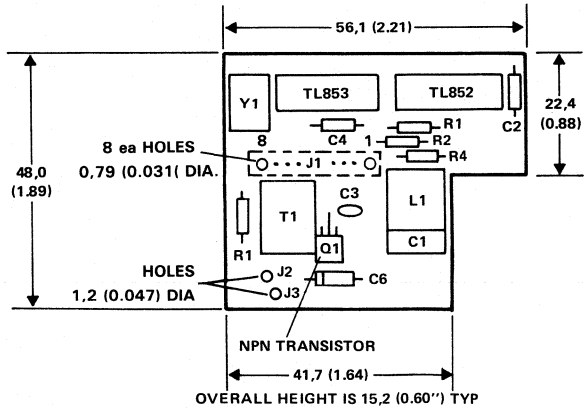
35 feet away. Although gain can be increased by varying R1 (Figure 4), there is a limit to which the gain can be increased for reliable module operation. This will vary from application to application. The modules are "kitted" prior to their final test during manufacture. This is necessary because the desired gain distribution is much narrower than the module gain distribution if all were kitted with one value resistor. As kitted, these modules will perform satisfactorily in most applications. As a rule of thumb, the gain can be increased by up to a factor of 3, if required, by increasing R1 correspondingly. Gain is directly proportional to R1.



†R1 is selected at the factory.

FIGURE 4. SCHEMATIC



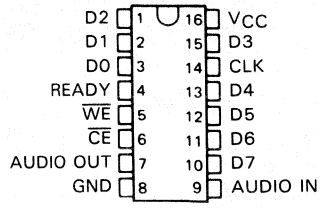
NOTE: All dimensions are in millimeters and parenthetically in inches.

FIGURE 5. COMPONENT LAYOUT AND DIMENSIONS OF MODULE

D2801, JUNE 1984 – REVISED JANUARY 1989

- **Each Circuit Contains 3 Programmable Tone Generators**
- **Programmable White-Noise Generator**
- **Programmable Attenuation**
- **Simultaneous Sounds**
- **Up to 500 kHz Clock Input for SN76494 and 4 MHz for SN76496**
- **External Audio Input for SN76496 May Be Summed with Internally Generated Tones**
- **The SN76494A and SN76496A are Interchangeable with the SN76494 and SN76496, Respectively**

N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

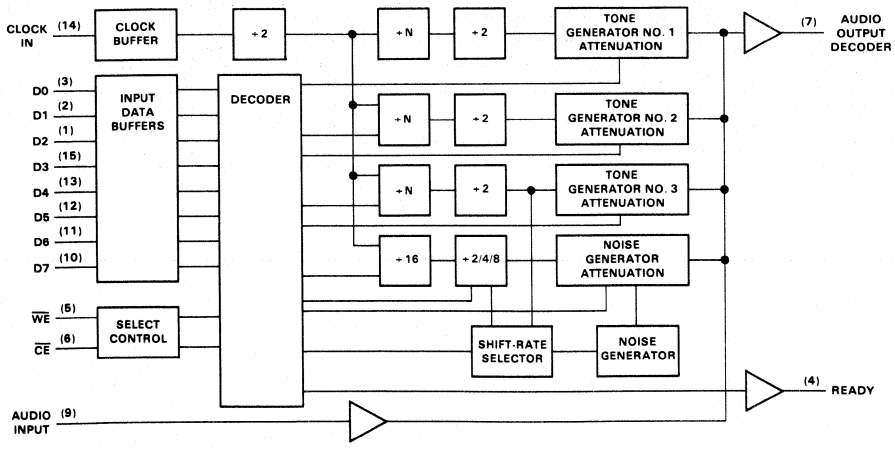
The SN76494 and SN76494A digital complex sound generators are integrated injection logic (I^2L) tone generators designed to provide low-cost tone or noise generation capability in microprocessor systems. The SN76494 and SN76494A are data-bus-based input-output peripheral devices that interface the microprocessor through 8 data lines and 3 control lines.

The SN76494 and SN76494A are identical to the SN76496 and SN76496A except that the maximum clock input frequency for SN76494 and SN76494A is 500 kHz and for SN76496 and SN76496A, it is 4 MHz. A "divide-by-eight" stage is deleted from the SN76496 and SN76496A circuitry so that only 4 clock pulses are required to load the data into the SN76494 and SN76494A, compared to 32 pulses for the SN76496 and SN76496A.

Either of these devices may also be used as a replacement for the SN76489A in all applications if pin 9 is left open or grounded. The output load must be limited to 10 mA.

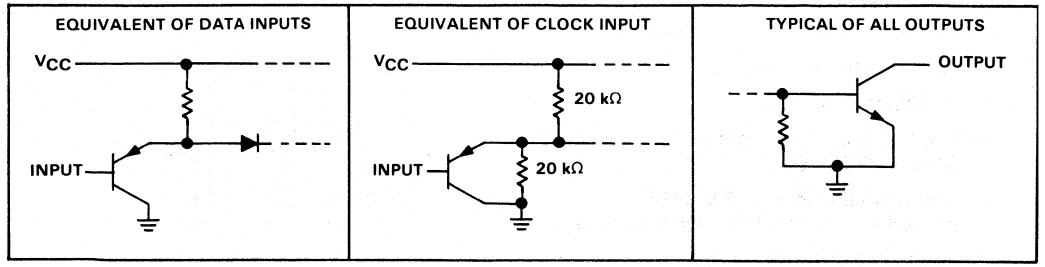
When audio input is not desired in the SN76494, SN76494A, SN76496 or SN76496A, the audio input pin should be grounded.

functional block diagram



4 Special Functions

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: Audio input . . . . . 0.9 V
All other inputs . . . . . 7 V
Output current at pin 7 . . . . . 10 mA
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		SN76494, SN76494A			SN76496, SN76496A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_I	Audio input current	0		1.8	0		1.8	mA
V_{OH}	High-level output voltage (pin 4)			5.5			5.5	V
I_{OL}	Low-level output current (pin 4)			2			2	mA
f_{clock}	Input clock frequency			0.5			4	MHz
$t_{d(WE)}$	Delay time, $\overline{CE}$ low to $\overline{WE}$ low	0			0			ns
t_{su}	Setup time, data before $\overline{WE}\downarrow$ or $\overline{CE}\downarrow$	0			0			ns
t_h	Hold time, data after READY↑	0			0			ns
T_A	Operating free-air temperature	0		70	0		70	°C

TEXAS INSTRUMENTS
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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_{OH}	High-level output current (pin 4)		V_O = 5.5 V			10	μA
I_{IH}	High-level input current (All digital inputs)		$V_I = V_{CC}$			10	μA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_I = 0		−25	−175	μA
		All other digital inputs			−10	−70	
V_{IB}	Input bias voltage, audio (pin 9)		R = 4.7 kΩ to V_{CC}	0.5	0.7	0.9	V
V_{OH}	High-level output voltage (pin 7)					5.5	V
V_{OL}	Low-level output voltage (pin 4)		I_{OL} = 2 mA		0.25	0.4	V
V_{OPP}	Peak-to-peak output voltage (pin 7)		V_{CC} = 5 V, Attenuation: Generator under test = 0 dB, All other generators = 30 dB	260			mV
I_{CC}	Supply current				30	50	mA
	Attenuation	2 dB NOM	See Table 1	1	2	3	dB
		4 dB NOM		3	4	5	
		8 dB NOM		7	8	9	
		16 dB NOM		15	16	17	
C_i	Input capacitance					15	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level RDY output from $\overline{CE}$	C_L = 225 pF, R_L = 2 kΩ to V_{CC}		90	150	ns
t_{PHL}	Propagation delay time high-to-low level, RDY output from $\overline{WE}$			90		ns
t_{PLH}	Propagation delay time low-to-high level, RDY output from CLK			90		ns

PARAMETER MEASUREMENT INFORMATION

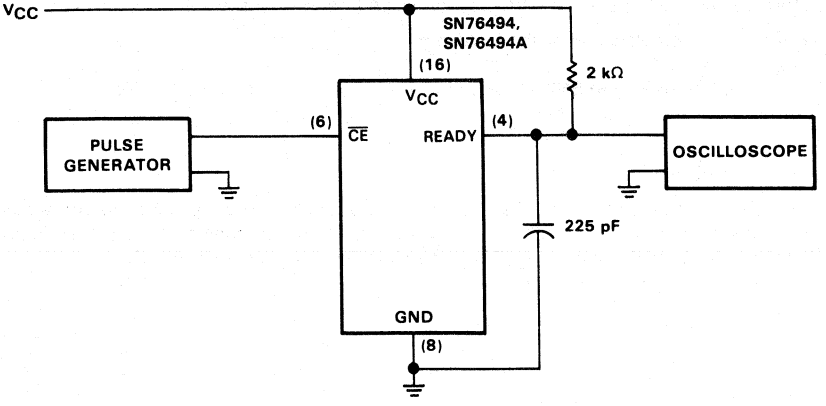

FIGURE 1. t_{PHL} TEST CIRCUIT

pin assignments and functions

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{CE}$	6	I	Chip Enable. When chip enable is low, the device is operational, input terminals are enabled, and data may be entered.
D0 (MSB)	3	I	D0 through D7 — Input data bus
D1	2	I	
D2	1	I	
D3	15	I	
D4	13	I	
D5	12	I	
D6	11	I	
D7 (LSB)	10	I	
V_{CC}	16	I	Supply voltage (5 V nom)
GND	8	O	Ground reference
CLOCK	14	I	Input Clock
$\overline{WE}$	5	I	Write Enable. When $\overline{CE}$ is enabled and $\overline{WE}$ is active (low), input on the data bus is accepted. $\overline{CE}$ and $\overline{WE}$ must be held low until READY returns high (four clock cycles for the SN76494 and SN76494A or 32 clock cycles for the SN76496 and SN76496A). If $\overline{WE}$ remains low throughout four additional clock cycles for the SN76494 and SN76494A (32 clock cycles for the SN76496 and SN76496A) a new write cycle will be initiated.
READY	4	O	When low, READY indicates that a write cycle is in progress; data on the input bus must remain valid until READY returns high.
AUDIO IN	9	I	Audio input from external source
AUDIO OUT	7	O	Audio Drive Out

PRINCIPLES OF OPERATION

tone generators

Each tone generator consists of a frequency synthesis section and an attenuation section. The frequency synthesis section requires 10 bits of information (F0-F9) to define half the period of the desired frequency (f). F0 is the most significant bit and F9 is the least significant bit. This information is loaded into a 10-stage tone counter, which counts down at an N/2 rate where N is the input clock frequency. When the tone counter counts down to zero, a borrow signal is produced. This borrow signal toggles the frequency flip-flop and also reloads the tone counter. Thus, the period of the desired frequency is twice the value of the period register.

The frequency can be calculated by the following:

$$f = \frac{N}{4n} \text{ for SN76494 and SN76494A, or } f = \frac{N}{32n} \text{ for SN76496 and SN76496A}$$

where N = clock in Hz
n = 10-bit binary number

The output level of each tone/noise generator may be selected by programming a four stage attenuator. The attenuator values, along with their bit position in the data word, are shown in Table 1. Multiple attenuation control bits may be true simultaneously. Thus, the maximum attenuation is 30 dB.

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TABLE 1. ATTENUATION CONTROL

BIT POSITION				WEIGHT
A0	A1	A2	A3	(in dB)
0	0	0	1	2
0	0	1	0	4
0	1	0	0	8
1	0	0	0	16
1	1	1	1	OFF

ıoise generator

The noise generator consists of a noise source and an attenuator. The noise source is a shift register with an exclusive OR-feedback network. The feedback network has provisions to protect the shift register from being locked in the zero state.

TABLE 2. NOISE FEEDBACK CONTROL

FEEDBACK	CONFIGURATION
0	"Periodic" noise
1	"White" noise

Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits. The fixed shift rates are derived from the input clock.

TABLE 3. NOISE GENERATOR FREQUENCY CONTROL

BITS		SHIFT RATE
NF0	NF1	
0	0	N/64
0	1	N/128
1	0	N/256
1	1	Tone generator #3 output

The output of the noise source is connected to a programmable attenuator as shown in Figure 4.

output buffer/amplifier

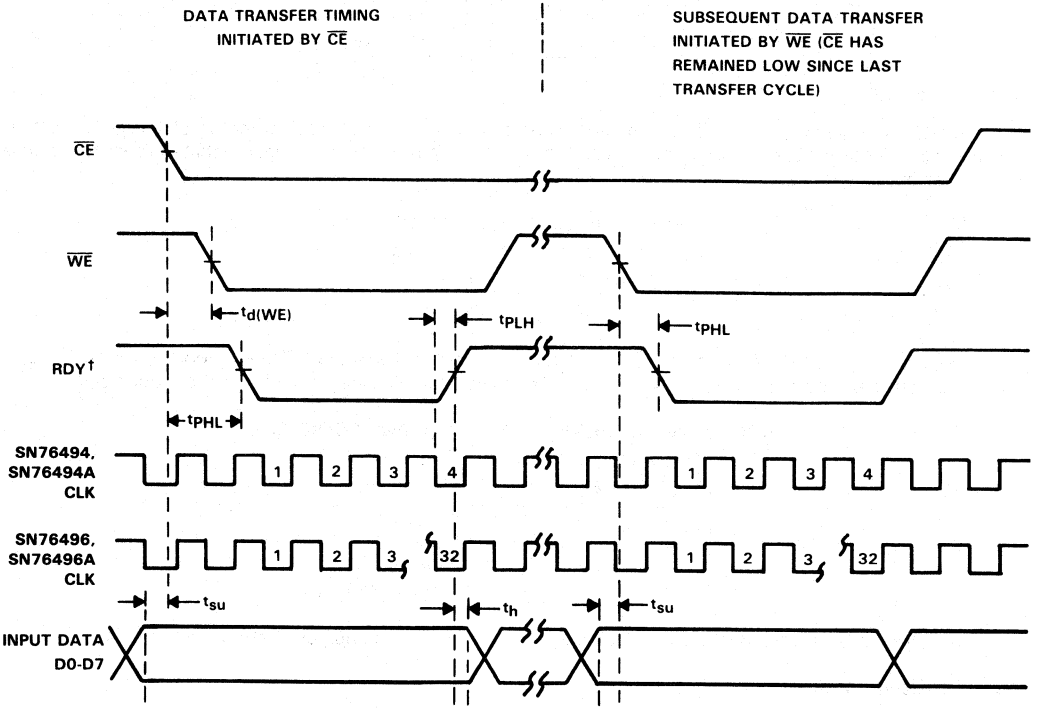
The output buffer is a conventional operational amplifier summing circuit. It sums the three tone generator outputs, the noise generator output, and any audio input through pin 9. The output buffer will generate up to 10 mA.

To prevent oscillations in the output buffer, the output (pin 7) should be decoupled. This is done by putting 10 ohms in series with 0.1 μF from pin 7 to ground (see Figure 3).

data transfer

The microprocessor selects the SN76494, SN76494A, SN76496, or SN76496A by taking $\overline{CE}$ low (low voltage). Unless $\overline{CE}$ is low, no data transfer can occur. When $\overline{CE}$ is low, the $\overline{WE}$ signal strobes the contents of the data bus to the appropriate control register. The data bus contents must be valid at this time.

The SN76494 and SN76494A require approximately 4 clock cycles to load the data into the control register The SN76496 and SN76496A require approximately 32 clock cycles. The open-collector READY output is used to synchronize the microprocessor to this transfer and is pulled to the false state (low) immediately following the falling edge of $\overline{CE}$ (or $\overline{WE}$ when data transfer is initiated by $\overline{WE}$). READY will go high upon completion of the data transfer cycle. The data transfer timing is shown below.



† $\overline{WE}$ must be returned high (inactive) within 4 clock pulses for the SN76494 and SN76494A (32 clock pulses for the SN76496 and SN76496A) after RDY returns high. Otherwise, a new data transfer cycle will be initiated.

FIGURE 2. DATA TRANSFER TIMING

TABLE 4. FUNCTION TABLE

INPUTS		OUTPUT
$\overline{CE}$	$\overline{WE}$	READY
L	L	L
L	H	L
H	L	H
H	H	H

This table is valid when the device is:
(1) not being clocked, and
(2) is initialized by pulling $\overline{WE}$ and $\overline{CE}$ high.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

CPU interface to SN76494, SN76494A, SN76496 or SN76496A

The microprocessor interfaces with the SN76494, SN76494A, SN76496, or SN76496A by means of the 8 data lines and 3 control lines ($\overline{WE}$, $\overline{CE}$ and READY). Each tone generator requires 10 bits of information to select the frequency and four bits of information to select the attenuation. A frequency selection requires a double-byte transfer, while an attenuator selection requires a single-byte transfer.

If no other control registers on the chip are accessed, a tone generator may be rapidly updated by initially sending both bytes of frequency and register data, followed by just the second byte of data for succeeding values. The register address is latched on the chip, so the data will continue going into the same register. This allows the six most significant bits to be quickly modified for frequency sweeps.

Control registers

The devices have 8 internal registers that are used to control the 3 tone generators and the noise source. During all data transfers to the devices, the first byte contains a 3-bit field that determines the destination control register. The register address codes are shown in Table 5.

TABLE 5. REGISTER ADDRESS FIELD

R0	R1	R2	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation
0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

Data formats

The formats required to transfer data are shown below.

	REG ADDR			DATA			
1	R0	R1	R2	F6	F7	F8	F9

BIT 0 FIRST BYTE BIT 7

	DATA						
0	x	F0	F1	F2	F3	F4	F5

BIT 0 SECOND BYTE BIT 7

UPDATE NOISE SOURCE (SINGLE BYTE TRANSFER)

	REG ADDR					SHIFT	
1	R0	R1	R2	x	FB	NF0	NF1

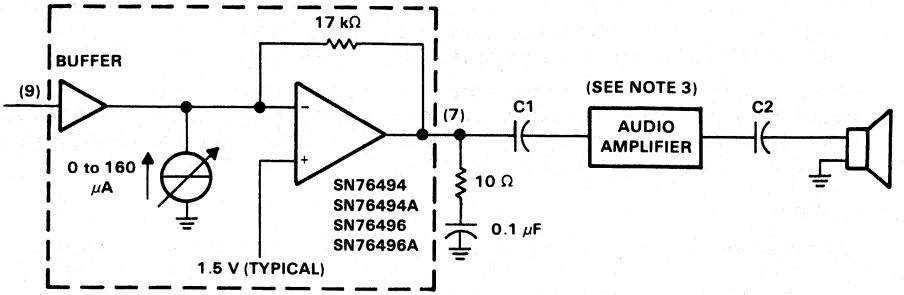
BIT 0 BIT 7

UPDATE ATTENUATOR (SINGLE BYTE TRANSFER)

	REG ADDR			DATA			
1	R0	R1	R2	A0	A1	A2	A3

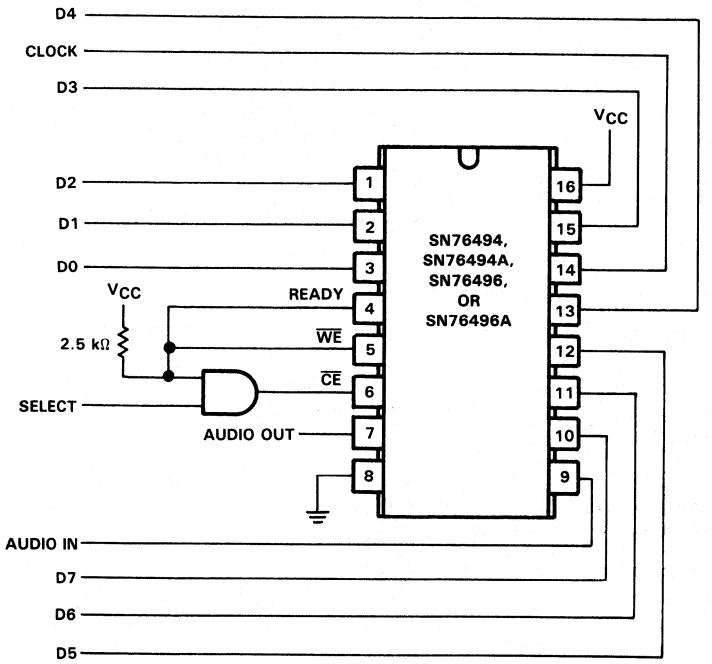
BIT 0 BIT 7

TYPICAL APPLICATION DATA



NOTE 3: The capacitance values of C1 and C2 are determined by the frequency response desired and the audio amplifier used.

FIGURE 3. EXTERNAL AUDIO OUTPUT INTERFACE



NOTES: 4. The data lines must be latched so that the data remains on them at least 32 clock cycles for the SN76496 and SN76496A or (4 clock cycles for the SN76494 and SN76494A) after the select line goes low.
5. The select pulse should be a negative-going pulse with minimum duration of 150 ns.

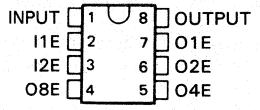
FIGURE 4. MICROCOMPUTER PARALLEL PORT INTERFACE

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2738, SEPTEMBER 1983—REVISED APRIL 1988

- **33 Distinct Input-to-Output Emitter Ratios from 3:1 to 1:15**
- **Wide Input current Range: 1 μA to 3 mA**
- **35-Volt Output Capability**
- **High Output Impedance**

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



escription

The TL010 is a Wilson current mirror that provides output current in a selectable fixed ratio to the input current. The ratio is substantially independent of changes in load, voltages, and temperature. Selecting the ratio consists of connecting appropriate input-emitter pins and output-emitter pins to ground as shown in Figure 1.

The TL010 is designed to operate with up to 3 mA input current if all three input-emitter pins are used. It will also operate at voltages up to 35 V.

The TL010I is characterized for operation from −40°C to 85°C. The TL010C is characterized for operation from 0°C to 70°C.

ypical values of current ratio at T_A = 25°C†

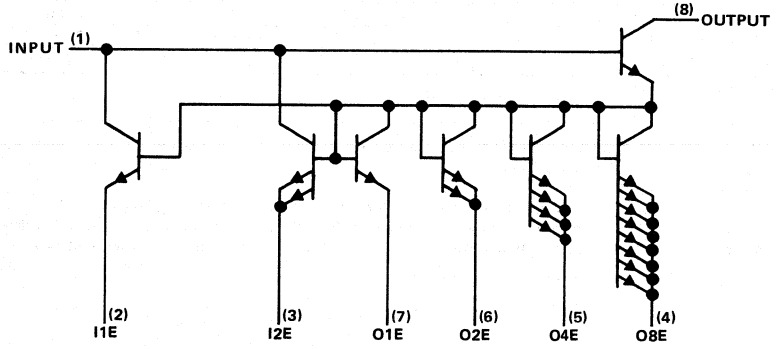
EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:15	14.1
1:14	13.2
1:13	12.3
1:12	11.4
1:11	10.5
1:10	9.55
1:9	8.62
1:8	7.72
2:15	7.23
1:7	6:71
2:13	6.29

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
1:6	5.78
2:11	5.34
1:5	4.82
3:14	4.53
2:9	4.38
3:13	4.21
1:4	3.89
3:11	3.57
2:7	3:40
3:10	3:25
1:3	2.90

EMITTER RATIO m:n†	CURRENT RATIO $h_F = I_O/I_I$
3:8	2.61
2:5	2.43
3:7	2.26
1:2	1.98
3:5	1.64
2:3	1.45
3:4	1.32
1:1	0.99
3:2	0.663
2:1	0.50
3:1	0.332

†m is the number of input emitters used, n is the number of output emitters used.

chematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 725 mW
Operating free-air temperature range: TL010I . . . . . −40°C to 85°C
TL010C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V
2. For operation above 25°C free-air temperature, derate linearly at the rate of 8.0 mW/°C.

recommended operating conditions

	TL010I		TL010C		UNIT
	MIN	MAX	MIN	MAX	
Output voltage, V_O	5	35	5	35	V
Input voltage, V_I	0.6	1.7	0.65	1.6	V
Input current per input emitter, I_I	0.001	1	0.001	1	mA
Operating free-air temperature, T_A	−40	85	0	70	°C

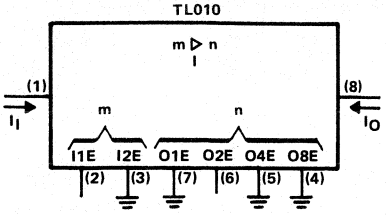
electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		TL010I			TL010C			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = m × 1 μA			1			1		V
		I_I = m × 10 μA			1.1			1.1		
		I_I = m × 100 μA			1.25			1.25		
		I_I = m × 1 mA			1.4			1.4		
h_F	Current ratio (I_O/I_I)	I_I = MIN to MAX	m:n = 1:8	6.97	7.72	8.13	7.05	7.72	8.13	
			m:n = 1:4	3.61	3.89	4.05	3.64	3.89	4.05	
			m:n = 1:2	1.84	1.98	2.07	1.88	1.98	2.07	
			m:n = 1:1	0.89	0.99	1.08	0.94	0.99	1.04	
			m:n = 2:1	0.46	0.50	0.56	0.475	0.50	0.525	
α_{hF}	Temperature coefficient of current ratio	I_I = MIN to MAX			300			300		ppm/°C
	Output-to-input isolation	I_I = MIN to MAX,	f = 1 kHz	60			60			dB
$V_{O(th)}$	Output threshold voltage§	I_I = MIN to MAX	T_A = MIN			1.1			1.05	V
			T_A = 25°C			1			1	
r_o	Output resistance¶	F = 1 kHz	I_I = m × 10 μA		200 m/n			200 m/n		MΩ
			I_I = m × 100 μA		20 m/n			20 m/n		
			I_I = m × 1 mA		2 m/n			2 m/n		
f_{max}	Maximum operating frequency#	I_I = m × 1 mA, R_L = 500 Ω			10			10		MHz

† m is the number of input emitters, n is the number of output emitters. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C.
§ Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶ The output resistance is directly proportional to the number of input emitters divided by the number of output emitters (m/n).
# Maximum operating frequency is the frequency at which the output current is down 3 dB from its low-frequency value.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION INFORMATION



See Notes 3 and 4

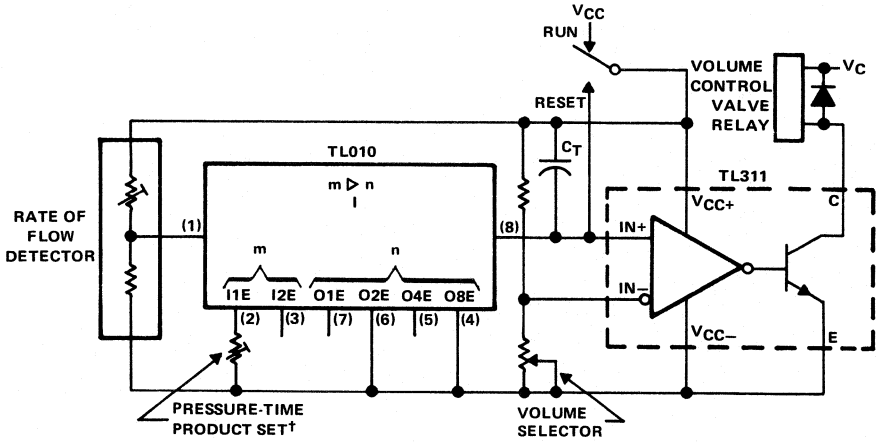
NOTES: 3. Selected emitters must be grounded as close as possible to the package to avoid unstable device behavior.
Using the fixed-Beta model, the current ratio for a current mirror of m input emitters and n output emitters may be calculated as

$$\frac{I_O}{I_I} = \frac{\beta^2 n + \beta(n + m)}{\beta^2 m + (\beta + 1)(m + n)}$$

Second-order effects, such as on-chip self-heating, may slightly perturb the observed ratio from the calculated value.

4. At high current levels, a small capacitor (270 pF) may be required between the input and output terminals to improve stability.

FIGURE 1. CURRENT MIRROR SET FOR A CURRENT RATIO OF 2:13



†Adjust for a mirror of 11.9

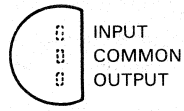
FIGURE 2. TYPICAL APPLICATION CIRCUIT

In the application shown in Figure 2, the problem is to measure a precise volume of liquid flowing through a line and shut off the flow with a relay when limit is reached. For the particular volume to be measured and the pressure detector used, a current gain of 11.9 is required. By setting the TL010 for a gain of 10 with the emitter selection, the exact gain of 11.9 may be obtained by adjusting the pressure-time product control.

D2614, FEBRUARY 1984—REVISED OCTOBER 1988

- **Wide Input Current Range:**
  1 μA to 1 mA
- **35-Volt Output Capability**
- **High Output Impedance**
- **Current-Ratio Tolerances Over Full Temperature Range;**
  ±8% for I Suffix
  ±7% for C Suffix
- **Typically Less Than ±1% Error at 25°C**

LP PACKAGE
(TOP VIEW)



TEMPERATURE RANGE	INPUT-TO-OUTPUT CURRENT RATIO			
	1:1	1:2	1:4	2:1
−40°C to 85°C	TL011I	TL012I		TL021I
0°C to 70°C	TL011C	TL012C	TL014AC	TL021C

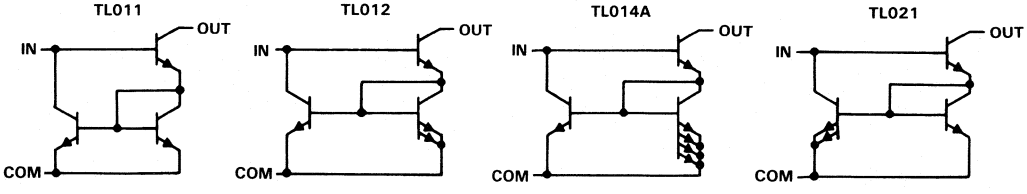
description

The TL011, TL012, TL014A, and TL021 are Wilson current mirrors with output currents in fixed proportion to the input currents and substantially independent of changes in voltage, load, and temperature. These devices make use of the tight matching properties of identical bipolar transistors on a monolithic integrated circuit chip to achieve current-ratio accuracy typically better than 98%.

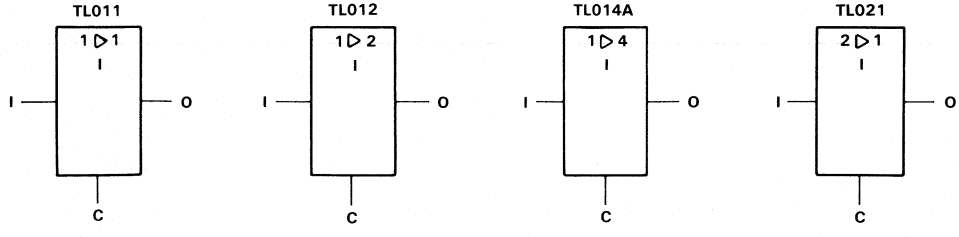
Current mirrors are used extensively in linear integrated circuit designs as active loads for operational-amplifier stages and as current sources for other stages. The TL011 family gives the designer this same capability with no sacrifice in accuracy or stability.

The TL011, TL012, and TL014A are designed to operate with input currents up to 1 mA and output voltage up to 35 V. The TL021 is designed for 2 mA and 35 V.

schematics



symbols



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Output voltage (see Note 1) . . . . . 45 V
Input current . . . . . 5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 775 mW
Operating free-air temperature range: TL011I, TL012I, TL021I . . . . . −40°C to 85°C
TL011C, TL012C, TL014AC, TL021C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Input and output voltages are with respect to the common terminal. Neither voltage should be more negative than −0.3 V
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C. The LP package dissipation rating was based on thermal resistance, $R_{\theta JA}$, measured in still air with the device mounted in an Augat socket. The bottom of the package was 10 mm (0.375 in.) above the socket.

recommended operating conditions

		TL0__I		TL0__C, AC		UNIT
		MIN	MAX	MIN	MAX	
Output voltage, V_O		5	35	5	35	V
Input current, I_O	TL021	0.002	2	0.002	2	mA
	All others	0.001	1	0.001	1	
Operating free-air temperature, T_A		−40	85	0	70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended ranges of operating free-air temperature and output voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL011			TL012			TL014A			TL021			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_I	Input voltage		I_I = 1 μA			1			1			1					V
			I_I = 2 μA												1		
			I_I = 10 μA			1.1			1.1			1.1					
			I_I = 20 μA												1.1		
			I_I = 100 μA			1.25			1.25			1.25					
			I_I = 200 μA												1.25		
			I_I = 1 mA			1.4			1.4			1.4					
			I_I = 2 mA												1.4		
h_F	Current ratio (I_O/I_I)	TLO__I	I_I = MIN to MAX‡		0.92	1	1.08	1.84	2	2.16	3.68	4	4.32	0.46	0.5	0.54	
		TLO__C, AC			0.93	1	1.07	1.86	2	2.14	3.72	4	4.28	0.465	0.5	0.535	
α_{hF}	Temperature coefficient of current ratio		I_I = MIN to MAX			50			100			200			200		ppm/°C
	Output-to-input isolation		I_I = MIN to MAX,	f = 1 kHz	80			80			80			80			dB
$V_{O(th)}$	Output threshold voltage§	TLO__I	I_I = MIN to MAX	T_A = −40°C			1.35			1.35			1.35			1.35	V
		TLO__C, AC		T_A = 0°C			1.25			1.25			1.25			1.25	
		All		T_A = 25°C			1.2			1.2			1.2			1.2	
r_o	Output resistance		f = 1 kHz	I_I = 10 μA		200			100			50					MΩ
				I_I = 20 μA											200		
				I_I = 100 μA		20			10			5					
				I_I = 200 μA											20		
				I_I = 1 mA		2			1			0.5					
				I_I = 2 mA											2		
f_{max}	Maximum operating frequency¶		I_I = MAX	R_L = 500 Ω		10			10			10			10		MHz

†All typical values are at T_A = 25°C.
‡For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§Output threshold voltage is the voltage at which the current ratio is equal to 90% of its value at V_O = 15 V.
¶Maximum operating frequency is the frequency at which the output current is down 3 dB from its low frequency value.

TYPICAL CHARACTERISTICS

TL011
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

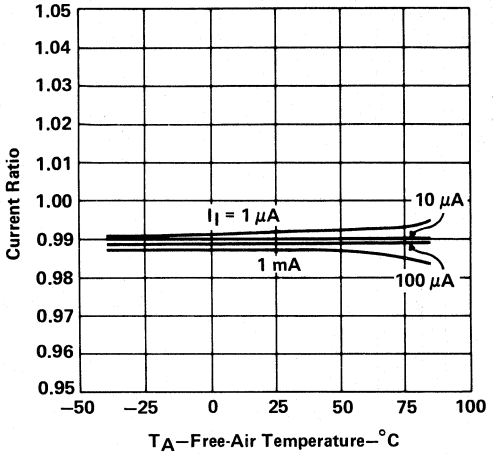


FIGURE 1

TL012
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

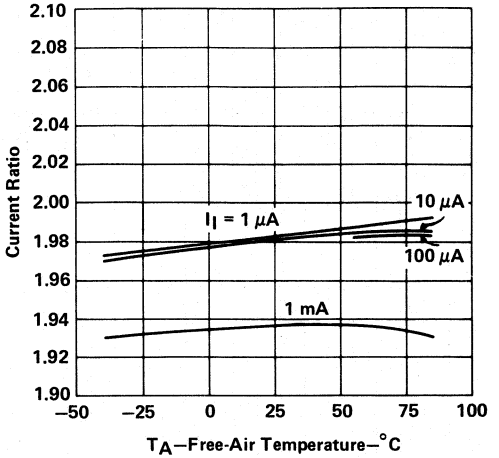


FIGURE 2

TL014A
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

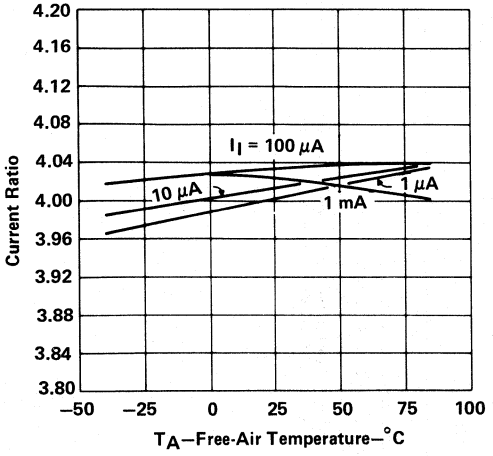


FIGURE 3

TL021
CURRENT RATIO
vs
FREE-AIR TEMPERATURE

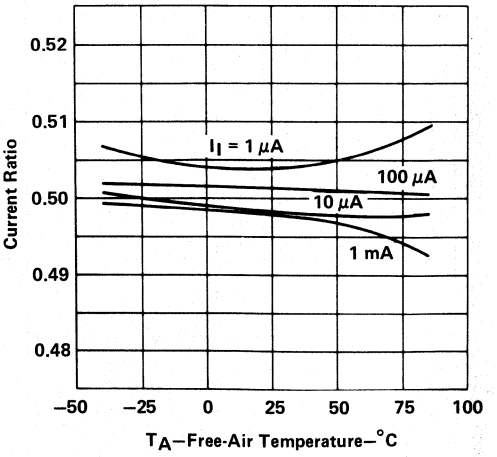


FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATIONS INFORMATION

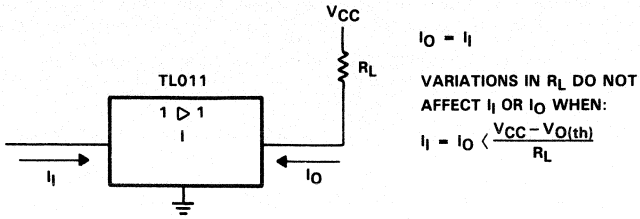
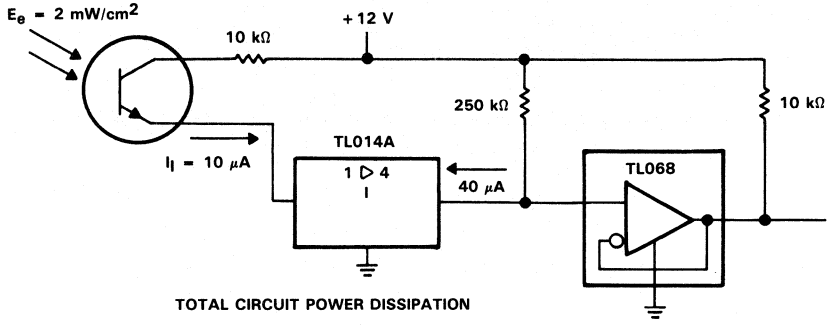


FIGURE 5. BASIC CURRENT BUFFER



TOTAL CIRCUIT POWER DISSIPATION

Idle condition: P_D = 1.5 mW typical
On condition: P_D = 12.5 mW typical
10 μA from phototransistor provides a V_O swing of 10 V at 1 mA.

FIGURE 6. PHOTOTRANSISTOR PREAMPLIFIER

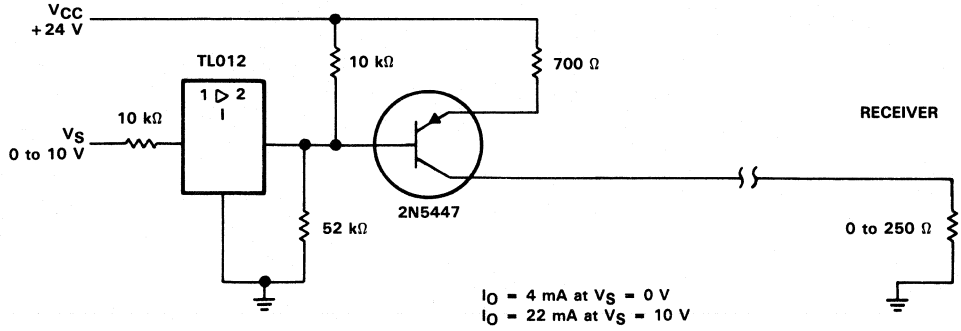
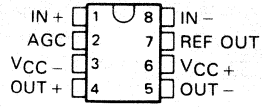


FIGURE 7. TWO-WIRE LINEAR CURRENT-MODE TRANSMITTER

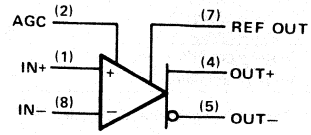
D2790, JUNE 1985—REVISED OCTOBER 1988

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Peak Gain . . . 38 dB Typ**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D OR P PACKAGE
(TOP VIEW)



symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pin. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers where a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL026C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	ABOVE $T_A = 25°C$ DERATING FACTOR	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics at 25 °C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	65	85	105	V/V
ΔA_{VD}	Change in voltage amplification	1	V_{IPP} = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = −1 mA to 100 μA	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV		50		MHz
I_{IO}	Input offset current				0.4	5	μA
I_{IB}	Input bias current				10	30	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	3	4		V
r_i	Input resistance at AGC, IN+, or IN−			10	30		kΩ
r_o	Output resistance				20		Ω
CMRR	Common-mode rejection ratio	3 3	V_{IC} = ±1 V, f = 100 kHz V_{IC} = ±1 V, f = 5 mHz	60	86 60		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50	70		dB
V_n	Broadband equivalent noise voltage	4	BW = 1 kHz to 10 MHz		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		6	10	ns
t_r	Rise time	2	ΔV_O = 1 V		4.5	12	ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	3	4		mA
I_{CC}	Supply current		No load, No signal		22	27	mA

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise specified)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	55		115	V/V
I_{IO}	Input offset current					6	μA
I_{IB}	Input bias current					40	μA
V_{ICR}	Common-mode input voltage range	3		±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	2.8			V
r_i	Input resistance at AGC, IN+, or IN−			8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f = 100 kHz	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal			30	mA

PARAMETER MEASUREMENT INFORMATION

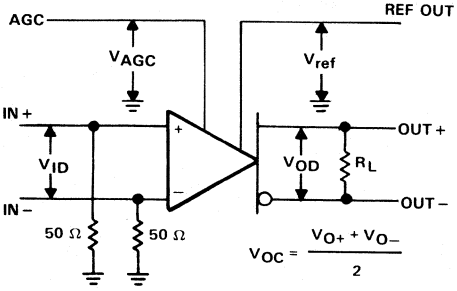


FIGURE 1

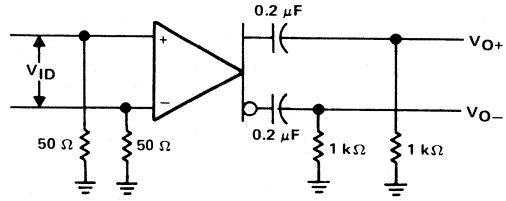


FIGURE 2

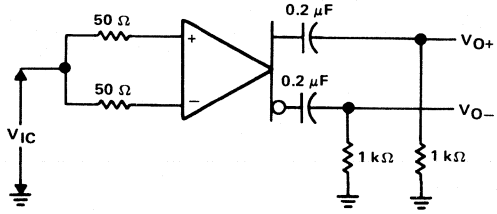


FIGURE 3

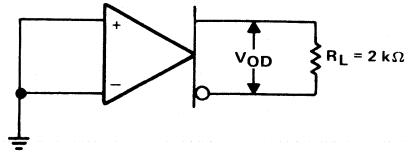


FIGURE 4

4 Special Functions

TYPICAL CHARACTERISTICS

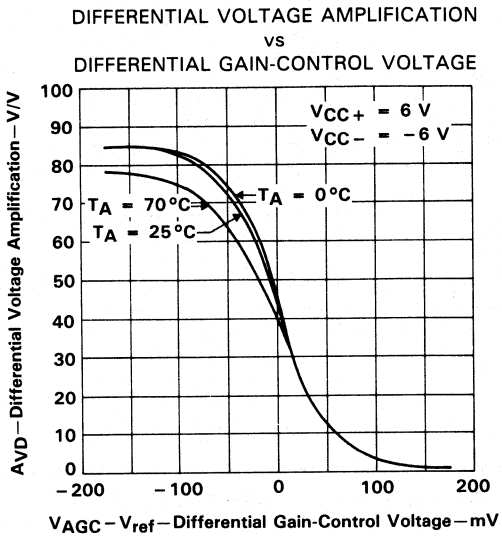


FIGURE 5

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TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 shows the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL026C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 6 and 7 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC026C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 6 and 7) from the OUT output through the feedback amplifiers to the AGC input produces the following equation:

1. AC output to diode D1, assuming sinusoidal signals

$$V_o = V_{OP}(\sin(wt)) \quad (2)$$

where:

V_{OP} = peak voltage of V_o

2. Diode D1 and capacitor C1 output

$$V_c = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_c = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_c \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_c + 2 \frac{R6}{R5 + R6} V_{ref} \quad (5)$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL026C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_c \quad (6)$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7)$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL026C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 6 and 7)

The output voltage level desired must fall within the following limits.

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_c = V_{OP} - V_d$), V_c is calculated as follows:

$$V_c = 1 \text{ V} - 0.7 \text{ V}$$

$$V_c = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL026C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_c} = \frac{\Delta V_{AGC}}{V_c} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

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TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 6 and 7 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

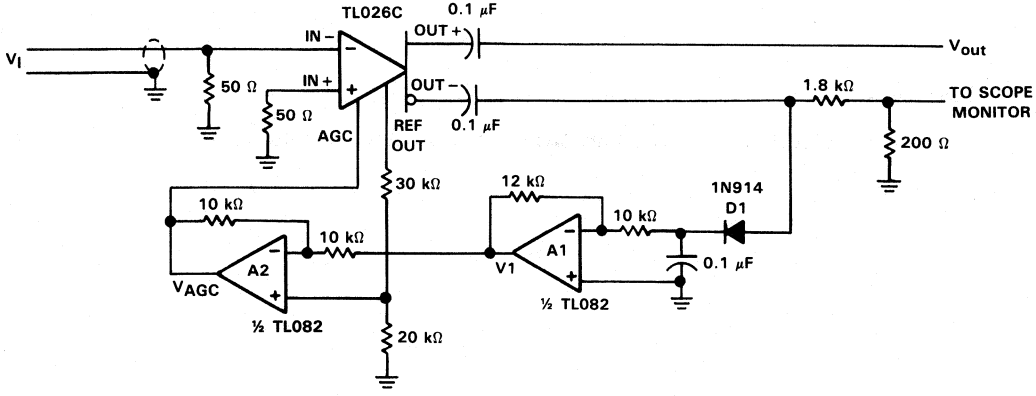
The circuit values in Figures 6 and 7 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 6 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 7 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL026C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL026C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL026C and, while the circuit is in the AGC mode, the output signal may become distorted.

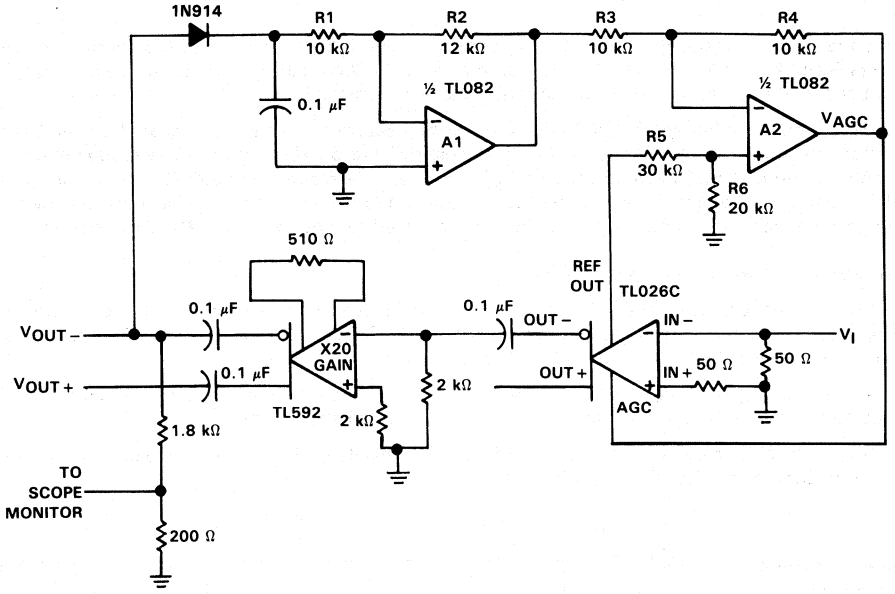
To observe the output signal of TL026C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 6 should be used.



NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 6. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



NOTE: V_{CC+} = 6 V and V_{CC-} = −6 V for TL026C and amplifiers A1 and A2.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

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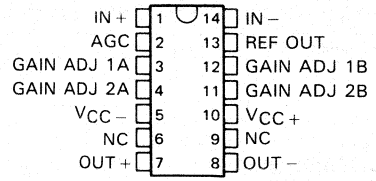
D2888, JUNE 1985—REVISED JANUARY 1989

- **Low Output Common-Mode Sensitivity to AGC Voltages**
- **Input and Output Impedances Independent of AGC Voltage**
- **Wide AGC Range . . . 50 dB Typ**
- **3-dB Bandwidth . . . 50 MHz**
- **Other Characteristics Similar to NE592 and uA733**

D, J, OR N PACKAGE
(TOP VIEW)

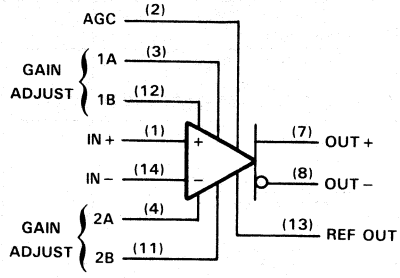


NC — No internal connection

DEVICE FEATURES

	GAIN	AGC
Gain Option 1	50 dB	50 dB
Gain Option 2	38 dB	50 dB

symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and outputs.

Internal feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Variable gain based on signal summation provides large AGC control over a wide bandwidth with low harmonic distortion. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios. The gain may be electronically attenuated by applying a control voltage to the AGC pins. No external frequency compensation components are required.

This device is particularly useful in TV and radio IF and RF AGC circuits, as well as magnetic-tape and disk-file systems where AGC is needed. Other applications include video and pulse amplifiers for which a large AGC range, wide bandwidth, low phase shift, and excellent gain stability are required.

The TL027M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL027C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Common-mode input voltage . . . . . ±6 V
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . 500 mW
Operating free-air temperature: TL027M . . . . . −55°C to 125°C
TL027C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE 1: All voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} except differential input and output voltages.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		3	6	8	V
Supply voltage, V_{CC-}		−3	−6	−8	V
Operating free-air temperature, T_A	TL027M	−55		125	°C
	TL027C	0		70	

electrical characteristics at 25°C operating free-air temperature, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	200	300	400	V/V
				2	65	85	105	
ΔA_{VD1}	Change in voltage amplification	1	$V_{I(PP)}$ = 7.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	1		−50		dB
ΔA_{VD2}	Change in voltage amplification	1	$V_{I(PP)}$ = 28.5 mV, R_L = 2 kΩ, $V_{AGC} - V_{ref}$ = ±180 mV	2		−50		dB
V_{ref}	Voltage at REF OUT		I_{ref} = 1 mA to 100 μA	1	1.3		1.5	V
BW	Bandwidth (−3 dB)	2	$V_{O(PP)}$ = 1 V, $V_{AGC} - V_{ref}$ = ±180 mV	1		20		MHz
				2		50		
I_{IO}	Input offset current			1 or 2		0.4	5	μA
I_{IB}	Input bias current			1 or 2		10	30	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OC}	Common-mode output voltage	1	R_L = ∞	1 or 2	3.25	3.75	4.25	V
ΔV_{OC}	Change in common-mode output voltage	1	V_{AGC} = 0 to 2 V, R_L = ∞	1 or 2			300	mV
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			0.75	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	3	4		V
r_i	Input resistance			1		4		kΩ
				2	10	30		
r_o	Output resistance					20		Ω
C_i	Input capacitance					2		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	60	86		dB
		3	V_{IC} = ±1 V, f = 5 MHz	2		60		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		dB
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz	1 or 2		12		μV
t_{pd}	Propagation delay time	2	ΔV_O = ±1 V	1		7.5		ns
				2		6	10	
t_r	Rise time	2	ΔV_O = ±1 V	1		10.5		ns
				2		4.5	12	
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	3	4		mA
I_{CC}	Supply current		No load, No signal	1 or 2		22	27	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm}$ = ±6 V, V_{AGC} = 0 V, REF OUT pin open (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	$V_{O(PP)}$ = 3 V, R_L = 2 kΩ	1	150		450	V/V
				2	55		115	
I_{IO}	Input offset current			1 or 2			6	μA
I_{IB}	Input bias current			1 or 2			40	μA
V_{ICR}	Common-mode input voltage range	3		2	±1			V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞	1 or 2			1.5	V
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	1	R_L = 2 kΩ	1 or 2	2.8			V
r_i	Input resistance			2	8			kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, f < 100 kHz	2	50			dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50			dB
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V, V_O = 3 V	1 or 2	2.8	4		mA
I_{CC}	Supply current	1	No load, No signal	1 or 2			30	mA

† The gain option is selected as follows:
Gain Option 1. . .Gain Adjust pin 1A is connected to pin 1B, pins 2A and 2B are open.
Gain Option 2. . .Gain Adjust pin 2A is connected to pin 2B, pins 1A and 1B are open.

PARAMETER MEASUREMENT INFORMATION

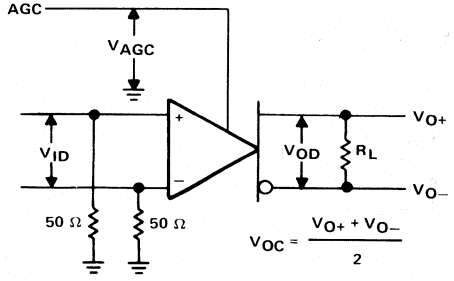


FIGURE 1

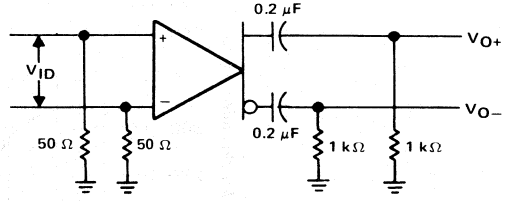


FIGURE 2

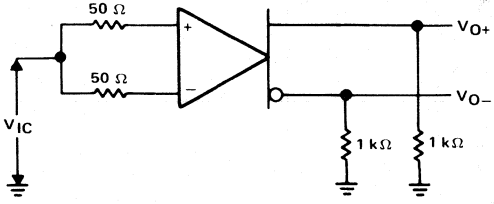


FIGURE 3

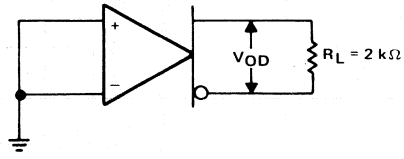


FIGURE 4

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

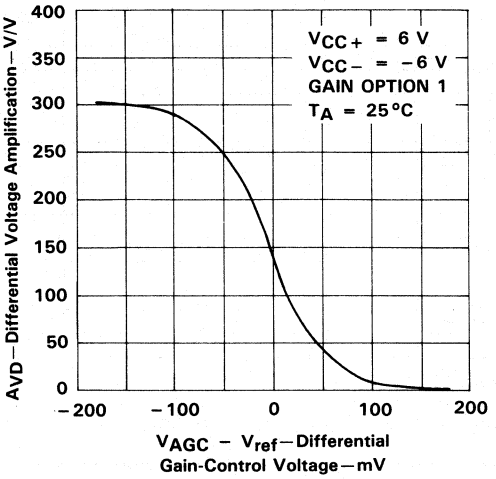


FIGURE 5

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
DIFFERENTIAL GAIN-CONTROL VOLTAGE

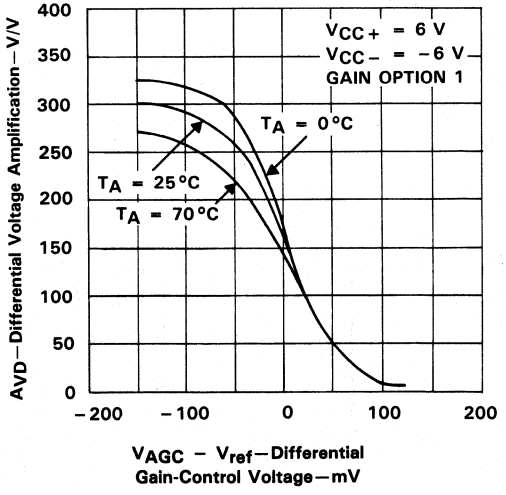


FIGURE 6

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TYPICAL APPLICATION INFORMATION

gain characteristics

Figure 5 and 6 show the differential voltage amplification versus the differential gain-control voltage ($V_{AGC} - V_{ref}$). V_{AGC} is the absolute voltage applied to the AGC input and V_{ref} is the dc voltage at the REF OUT output. As V_{AGC} increases with respect to V_{ref}, the TL027C gain changes from maximum to minimum. As shown in Figure 5 for example, V_{AGC} would have to vary from approximately 180 mV less than V_{ref} to approximately 180 mV greater than V_{ref} to change the gain from maximum to minimum. The total signal change in V_{AGC} is defined by the following equation.

$$\Delta V_{AGC} = V_{ref} + 180\ mV - (V_{ref} - 180\ mV) \quad (1)$$

$$\Delta V_{AGC} = 360\ mV$$

However, because V_{AGC} varies as the ac AGC signal varies and also differentially around V_{ref}, then V_{AGC} should have an ac signal component and a dc component. To preserve the dc and thermal tracking of the device, this dc voltage must be generated from V_{ref}. To apply proper bias to the AGC input, the external circuit used to generate V_{AGC} must combine these two voltages. Figures 7 and 8 show two circuits that will perform this operation and are easy to implement. The circuits use a standard dual operational amplifier for AGC feedback. By providing rectification and the required feedback gain, these circuits are also complete AGC systems.

circuit operation

Amplifier A1 amplifies and inverts the rectified and filtered AGC signal voltage V_C producing output voltage V1. Amplifier A2 is a differential amplifier that inverts V1 again and adds the scaled V_{ref} voltage. This conditioning makes V_{AGC} the sum of the signal plus the scaled V_{ref}. As the signal voltage increases, V_{AGC} increases and the gain of the TLC027C is reduced. This maintains a constant output level.

feedback circuit equations

Following the AGC input signal (Figures 7 and 8) from the OUT – output through the feedback amplifiers to the AGC input produces the following equations.

1. AC output to diode D1, assuming sinusoidal signals

$$V_o = V_{OP}\ (\sin\ (wt)) \quad (2)$$

where:

V_{OP} = peak voltage of V_o

2. Diode D1 and capacitor C1 output

$$V_C = V_{OP} - V_F \quad (3)$$

where:

V_F = forward voltage drop of D1
V_C = voltage across capacitor C1

3. A1 output

$$V1 = -\frac{R2}{R1} V_C \quad (4)$$

TYPICAL APPLICATION INFORMATION

4. A2 output (R3 = R4)

$$V_{AGC} = \frac{R2}{R1} V_C + 2 \frac{R1}{R5 + R6} V_{ref} \quad (5$$

Amplifier A2 inverts V1 producing a positive AGC signal voltage. Therefore, the input voltage to the TL027C AGC pin consists of an AGC signal equal to:

$$\frac{R2}{R1} V_C \quad (6$$

and a dc voltage derived from V_{ref}, defined as the quiescent value of V_{AGC}.

$$V_{AGC(q)} = 2 \frac{R6}{R5 + R6} V_{ref} \quad (7$$

For the initial resistor calculations, V_{ref} is assumed to be typically 1.4 V making quiescent V_{AGC} approximately 1.22 V ($V_{AGC(q)} = V_{ref} - 180$ mV). This voltage allows the TL027C to operate at maximum gain under no-signal and low-signal conditions. In addition, with V_{ref} used as both internal and external reference, its variation from device to device automatically adjusts the overall bias and makes AGC operation essentially independent of the absolute value of V_{ref}. The resistor divider needs to be calculated only once and is valid for the full tolerance of V_{ref}.

output voltage limits (see Figures 7 and 8)

The output voltage level desired must fall within the following limits:

1. Because the data sheet minimum output swing is 3 V peak-to-peak using a 2-kΩ load resistor, the user-selected design limit for the peak output swing should not exceed 1.5 V.
2. The voltage drop of the rectifying diode determines the lower voltage limit. When a silicon diode is used, this voltage is approximately 0.7 V. The output voltage V_O must have sufficient amplitude to exceed the rectifying diode drop. A schottky diode can be used to reduce the V_O level required.

gain calculations for a peak output voltage of 1 V

A peak output voltage of 1 V was chosen for gain calculations because it is approximately midway between the limits of conditions 1 and 2 in the preceding paragraph.

Using equation 3 ($V_C = V_{OP} - V_d$), V_C is calculated as follows:

$$V_C = 1 \text{ V} - 0.7 \text{ V}$$

$$V_C = 0.3 \text{ V}$$

Therefore, the gain of A1 must produce a voltage V1 that is equal to or greater than the total change in V_{AGC} for maximum TL027C gain change.

With a total change in V_{AGC} of 360 mV and using equation 4, the calculation is as follows:

$$-\frac{V1}{V_C} = \frac{\Delta V_{AGC}}{V_C} = \frac{R2}{R1} = \frac{0.36}{0.3} = 1.2$$

If R1 is 10 kΩ, R2 is 1.2 times R1 or 12 kΩ.

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TYPICAL APPLICATION INFORMATION

Since the output voltage for this circuit must be between 0.85 V and 1.3 V, the component values in Figures 7 and 8 provide a nominal 1-V peak output limit. This limit is the best choice to allow for temperature variations of the diode and minimum output voltage specification.

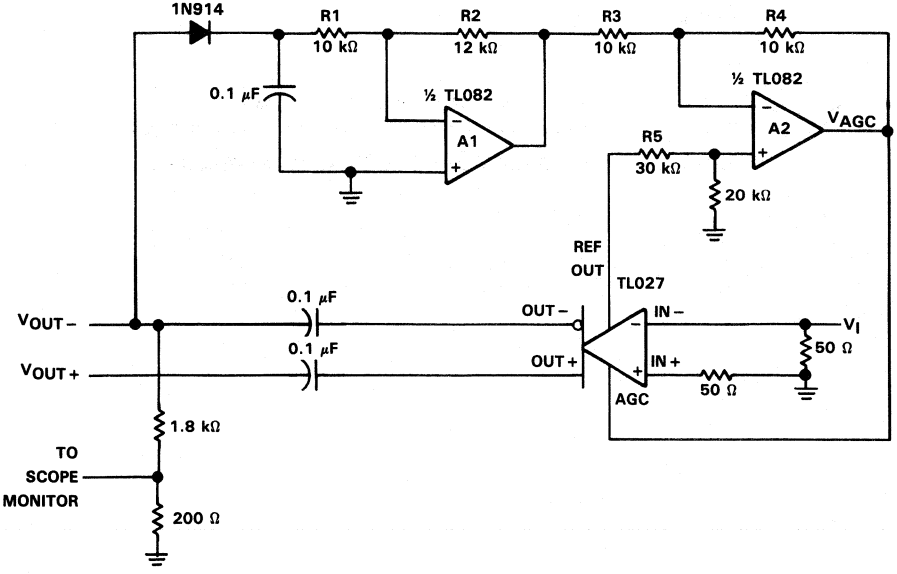
The circuit values in Figures 7 and 8 will produce the best results in this general application. Because of rectification and device input constraints, the circuit in Figure 7 will not provide attenuation and has about 32 dB of control range. The circuit shown in Figure 8 will have approximately 25% variation in the peak output voltage limit due to the variation in gain of the TL592 device to device. In addition, if a lower output voltage is desired, the output of the TL027C can be used for approximately 40 mV of controlled signal.

considerations for the use of the TL027C

To obtain the most reliable results, RF breadboarding techinques must be used. A groundplane board should be used and power supplies should be bypassed with 0.1-μF capacitors. Input leads and output leads should be as short as possible and separated from each other.

A peak input voltage greater than 200 mV will begin to saturate the input stages of the TL027C and, while the circuit is in the AGC mode, the output signal may become distorted.

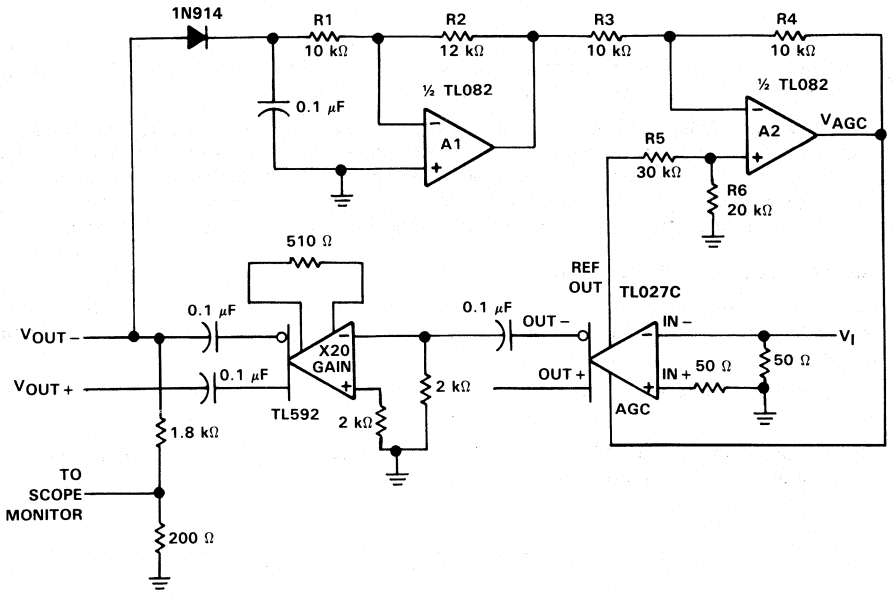
To observe the output signal of TL027C or TL592, low-capacitance FET probes or the output voltage divider technique shown in Figure 7 should be used.



NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On the TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 7. TYPICAL APPLICATION CIRCUIT WITH NO ATTENUATION

TYPICAL APPLICATION INFORMATION



NOTES: A. V_{CC+} = 6 V and V_{CC-} = −6 V for TL027C and amplifiers A1 and A2.
B. On TL027, short pin 3 to pin 12 and pin 4 to pin 11. Connect pins 6 and 9 to ground.

FIGURE 8. TYPICAL APPLICATION CIRCUIT WITH ATTENUATION

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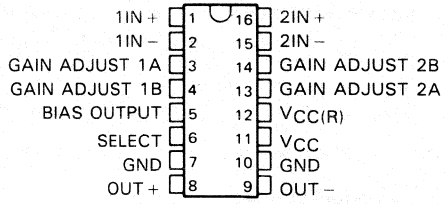
D3002, MARCH 1986—REVISED DECEMBER 1988

- **Designed for Use with the TL041 Magnetic Field Pulse Detector**
- **Wide Bandwidth . . . 20 MHz Typ**
- **Low Noise . . . Less than 8 μV Typ**
- **Independently Adjustable Channel Gains . . . Up to 450 Typ**
- **No Frequency Compensation Required**
- **Internal Voltage Source Eliminates External Components**
- **Input Channel Select Pin is Compatible with TTL and CMOS**
- **Low Power Dissipation . . . 150 mW Typ**

D OR N PACKAGE
(TOP VIEW)



CHANNEL SELECT TABLE

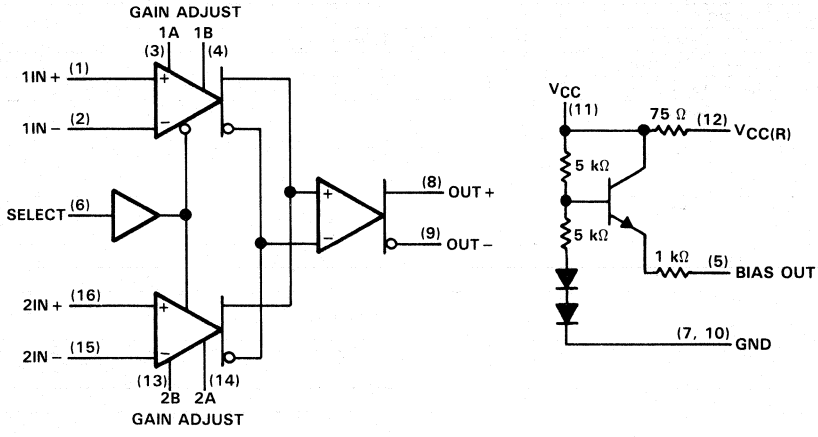
SELECT	CHANNEL
L	1
H	2

description

The TL040 is a two-channel multiplexed video amplifier designed for use with magnetic pulse detectors in streaming tape drives. The circuit design eliminates many external components, and the D package allows substantial reduction in circuit board area. The gain of each channel is a function of the resistance across its gain-adjust pins (A-B) with maximum gain occurring when the terminals are shorted.

The $V_{CC(R)}$ pin provides supply voltage decoupling required by some designs. The BIAS OUT pin provides a voltage source for other circuits that is approximately equal to 1/2 V_{CC}.

functional block diagram



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) . . . . . 14 V
Input voltage range . . . . . −0.2 V to V_{CC} + 0.2 V
Continuous total power dissipation . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltages except differential voltages are with respect to the ground terminals.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	10.8	12	13.2	V
Common-mode input voltage (diff inputs), V_{IC}	5	6	7	V
High-level input voltage, SELECT input, V_{IH}	2			V
Low-level input voltage, SELECT input, V_{IL}			0.8	V
Output sink current (diff outputs), I_{sink}			1.5	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics of selected channel at T_A = 25°C, V_{CC} = 12 V, R_{AB} = 0, R_L = 2 kΩ (unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1		300	530	600	V/V
	Channel amplification mismatch	1			1%		
	Large-signal differential voltage attenuation	1	Δ V_I = 50 mV on unselected input		60		dB
V_{OC}	Common-mode output voltage	1	R_L = ∞		8.5		V
V_{OPP}	Maximum peak-to-peak output voltage swing	1			4		V
BW	Bandwidth (−3 dB)	2			20		MHz
I_{IO}	Input offset current	1			0.1	3	μA
I_{IB}	Input bias current	1			6	17	μA
V_{OD}	Differential output voltage	1	R_L = ∞, V_{ID} = 0		0.2		V
r_i	Input resistance (differential inputs)				4		kΩ
CMRR	Common-mode rejection ratio	3	V_{IC} = 5 V to 7 V	60	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	V_{CC} = 10.8 V to 13.2 V	50	70		dB
V_n	Broadband equivalent input noise voltage	4			<5		μV
I_{IH}	High-level input current, Select input		V_{IH} = 2.7 V			−0.4	mA
I_{IL}	Low-level input current, Select input		V_{IL} = 0.4 V			20	μA
t_{pd}	Propagation delay time (differential inputs)	2	ΔV_O = 1 V		15		ns
t_r	Output rise time	2	ΔV_O = 1 V		20		ns
I_{CC}	Supply current	1			12	15	mA
	Bias output voltage	1		5	6	7	V

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PARAMETER MEASUREMENT INFORMATION

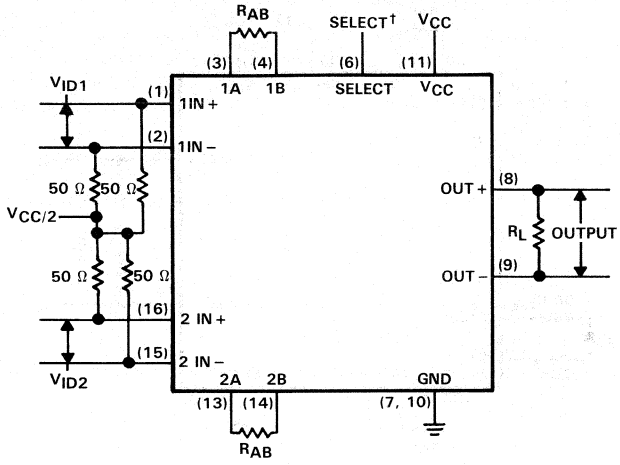

FIGURE 1

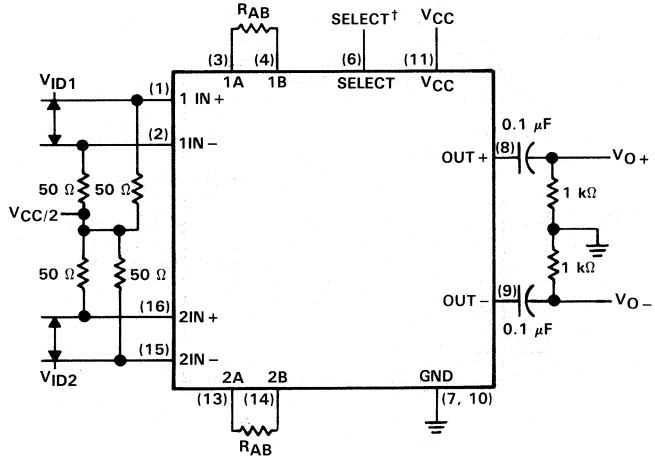

FIGURE 2

†Select input must be at proper logic level to select desired input channel.

PARAMETER MEASUREMENT INFORMATION (continued)

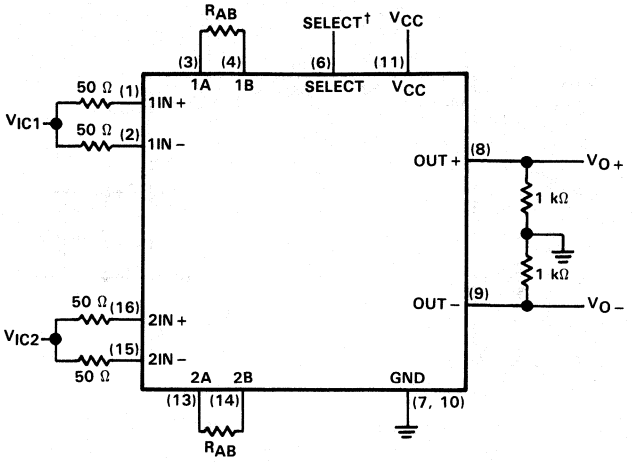

FIGURE 3

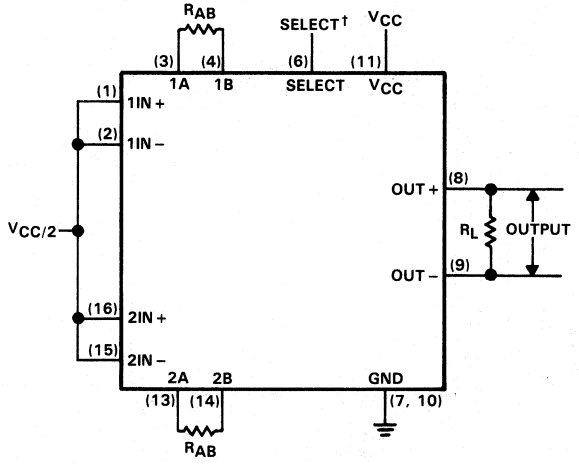

FIGURE 4

†Select input must be at proper logic level to select desired input channel.

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TYPICAL CHARACTERISTICS

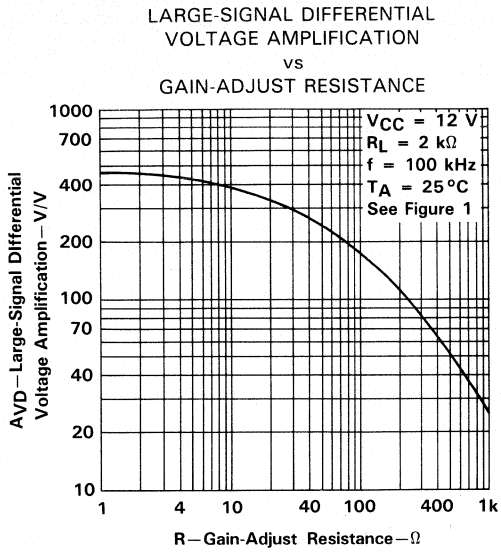


FIGURE 5

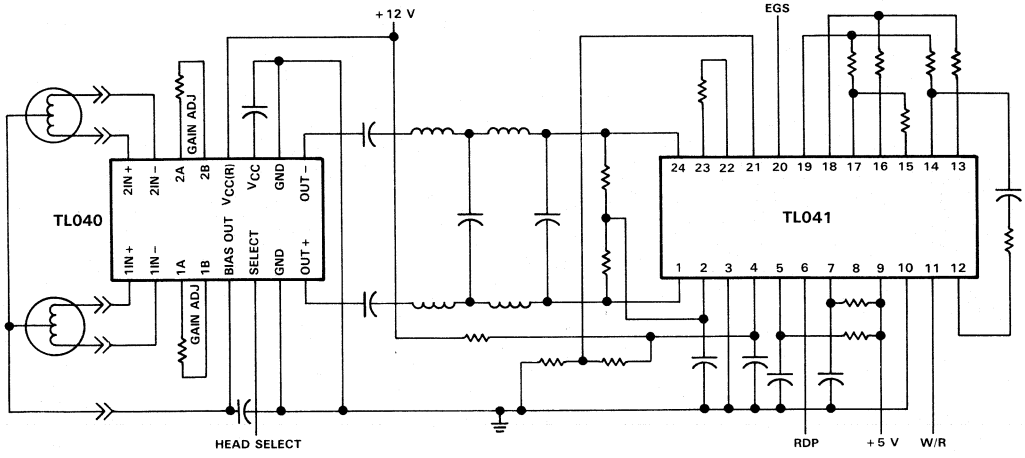


FIGURE 6. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

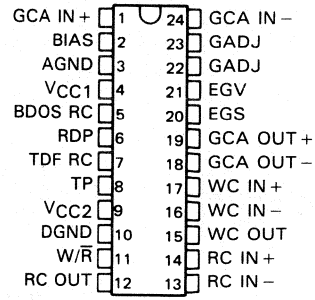
4 Special Functions

4 Special Functions

D3024, AUGUST 1987

- **Designed for Signal Processing in Streaming-Tape Memory Units in Combination with TL040 Two-Channel Video Amplifier**
- **Space-Saving LSI Circuits Include:**
  - **Two High-Speed Differential Comparators**
  - **Time-Domain Filter**
  - **Bidirectional One-Shot Multivibrator**
  - **Gain-Controlled Video Amplifier with Differential Inputs and Outputs**
- **Amplifier and Comparator Bandwidth . . . 20 MHz Typical**
- **Maximum Data Rate at Read Data Pulse (RDP) . . . 1.4 Mb/s Typical**
- **Available in 300-mil Dual-In-Line and "Small Outline" Plastic Packages**

DW OR NT . . . PACKAGE
(TOP VIEW)



Description

The TL041 is a magnetic tape read signal conditioner designed for use with the TL040 video amplifier. When combined, these devices amplify the low-signal output from a streaming-tape playback head and reconstruct the data as originally written on the tape. The TL041C includes a gain-controlled amplifier, two comparators, read/write select logic, a time-domain filter, and a bidirectional one-shot multivibrator.

The amplifier has differential inputs, differential outputs, and electronic gain control. A special feature of the electronic gain control is the Electronic Gain Select (EGS). When the EGS input is high, the Electronic Gain Voltage (EGV) input is driven low and amplifier gain is determined by the value of the resistor connected between the Gain Adjust (GADJ) pins. When the EGS input is low, the gain set by the resistor is increased by an amount determined by the voltage applied to the EGV pin.

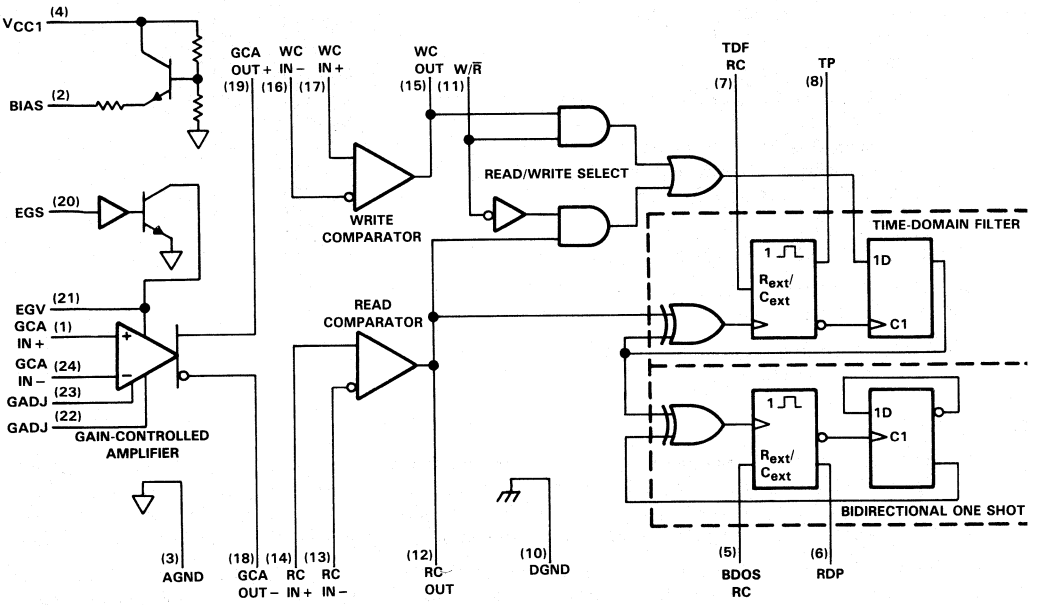
To accommodate different magnetic tape output signal levels, the amplifier gain may be switched by logic at the EGS input, controlled manually with an adjustable voltage at the EGV input, or automatically adjusted with an automatic gain control (AGC) circuit applying a control voltage to the EGV input.

The comparator functions are controlled by a logic input to the Write/Read (W/$\overline{R}$) select input. With the W/$\overline{R}$ input low, the read comparator output (usually connected as a zero-crossing detector) is sent to the time-domain filter. When W/$\overline{R}$ is high, the write comparator output is used to provide write amplitude verification in a typical read-after-write function.

The time-domain filter helps to ensure the input data is valid. A capacitor in series with a resistor, connected to the time-domain filter pin (TDF RC), begins charging at the leading edge of an input pulse from the read comparator. If the input pulse does not remain high for one RC time constant, the pulse is considered invalid and no signal is passed to the bidirectional one-shot multivibrator (BDOS). However, if the input pulse remains high for longer than one RC time constant, the pulse is considered valid and the signal is passed through the time-domain filter to trigger the BDOS. When triggered, the BDOS provides a pulse to the Read Data Pulse (RDP) output. The RDP output pulse duration is determined by a resistor-capacitor network connected to the BDOS RC pin.

The TL041C is characterized for operation from 0°C to 70°C.

functional block diagram



FUNCTION TABLE

INPUT CONDITONS			I/O NAME	I/O CONDITION
EGS	W/R	DIFFERENTIAL INPUTS WRITE OR READ COMPARATOR		
	X	RC IN+ > RC IN–	RC OUT	H
	X	RC IN– > RC IN+	RC OUT	L
	L	X	RC OUT	Input to time-domain filter
	X	WC IN+ > WC IN–	WC OUT	H
	X	WC IN– > WC IN+	WC OUT	L
	H	X	WC OUT	Input to time-domain filter
H		X	EGV	L
L		X	EGV	Input

PIN NAME	PIN NO.	DESCRIPTION
AGND	3	Analog ground
BDOS RC	5	Bidirectional one-shot resistor and capacitor
BIAS	2	Output bias voltage
DGND	10	Digital ground
EGS	20	Electronic gain select
EGV	21	Electronic gain voltage
GCA IN−	24	Gain-controlled amplifier, inverting input
GCA IN+	1	Gain-controlled amplifier, noninverting input
GADJ	22	Gain adjust
GADJ	23	Gain adjust
GCA OUT−	18	Gain-controlled amplifier, inverting output
GCA OUT+	19	Gain-controlled amplifier, noninverting output
RC IN−	13	Read comparator, inverting input
RC IN+	14	Read comparator, noninverting input
RC OUT	12	Read comparator out
RDP	6	Read data pulse
TDF RC	7	Time-domain filter resistor and capacitor
TP	8	Test point
V_{CC1}	4	Analog collector supply voltage
V_{CC2}	9	Digital collector supply voltage
WC IN−	16	Write comparator, inverting input
WC IN+	17	Write comparator, noninverting input
WC OUT	15	Write comparator out
W/$\overline{R}$	11	Write/read

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage: V_{CC1} (see Note 1) . . . . . 14 V
V_{CC2} . . . . . 7 V
Input voltage range: Amplifier and comparators . . . . . AGND − 0.2 V to V_{CC1} + 0.2 V
Multivibrators and logic . . . . . AGND − 0.2 V to V_{CC2} + 0.2 V
Input current: EGV (see Note 2) . . . . . ±2 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages except differential voltages are with respect to network ground terminals (AGND and DGND tied together).
2. Driving EGV high from a low-impedance source (> ±2 mA capability) with EGS high can result in damage to the device.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DW	1350 mW	10.8 mW/°C	864 mW/°C
NT	1700 mW	13.6 mW/°C	1088 mW/°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}		10.8	12	13.2	V
Supply voltage, V_{CC2}		4.5	5	5.5	V
High-level input voltage, V_{IH}	EGS or W/$\overline{R}$	2			V
Low-level input voltage, V_{IL}	EGS or W/$\overline{R}$			0.8	V
Input voltage, V_I	EGS	0		10	V
	EGV	0		$0.8V_{CC1}$	
Common-mode input voltage to gain-control amplifier, V_{IC}			4		V
High-level output current, I_{OH}	WC OUT, RC OUT, TP, or RDP			−400	μA
Low-level output current, I_{OL}	WC OUT, RC OUT, TP, or RDP			8	mA
Pulse duration, t_w	TP or RDP	40			ns
External timing resistance, (see Note 3)	TDF or BDOS RC	5		25	kΩ
External timing capacitance	TDF or BDOS RC)	0.01	0.1	1000	nF
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Some high resistance and capacitance combinations may produce abnormal output waveforms.

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POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at V_{CC1} = 12 V, V_{CC2} = 5 V, $V_{IC(GIC)}$ = V_{bias}, R_{ADJ} = 5 kΩ, EGS at high level, EGV at 0 V, r_i = 50 Ω, R_L = 2 kΩ, T_A = 25°C (unless otherwise noted)

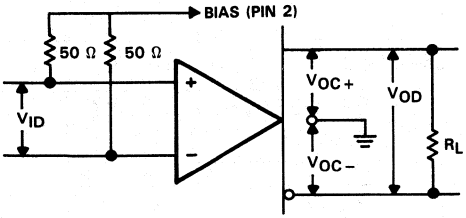
gain-controlled amplifier

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	1	V_{ID} = 0,	V_{OD} = V_O		0.35	0.75	V
V_{OPP}	Maximum differential output voltage	1	V_{ID} = 1 V,	V_{OPP} = V_O	3	4		V
A_{VD}	Large-signal differential voltage amplification	1	V_{ID} = 20 mV,	EGS high	8	14	20	V/V
			V_{id} = 20 mV, EGS low, f = 455 kHz	EGV at 4 V		19		V/V
				EGV at 9.6 V		90		
CMRR	Common-mode rejection ratio	2	V_{IC} = 2 V to 5 V		60	80		dB
V_{IC}	Common-mode input voltage	2			2		5	V
V_{OC}	Common-mode output voltage	1	V_{ID} = 0		4	5	6	V
I_{IO}	Input offset current	1	$I_{IB+} - I_{IB-}$			0.2	3	μA
I_O	Output current, sink				1.5	2		mA
I_{IB}	Input bias current	1	$(I_{IB+} + I_{IB-})/2$			5	17	μA
$V_{O(BIAS)}$	Bias output voltage	1			3	4	5	V
$z_{o(BIAS)}$	Bias output impedance					1		kΩ
z_i	Input impedance					30		kΩ
BW	Bandwidth (−3 dB)	3				20		MHz
k_{SVR}	Supply voltage rejection ratio	4	V_{CC1} = 10.8 V to 13.2 V		50	70		dB
I_{CC1}	Supply current from V_{CC1}		V_{CC1} = 13.2 V,	No signal		32	45	mA

logic section

PARAMETER			TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage			V_{CC2} = 4.5 V, I_{OH} = −400 μA	V_{ID} = 0.1 V,	2.7	3.5		V
V_{OL}	Low-level output voltage			V_{CC2} = 4.5 V, I_{OL} = 8 mA	V_{ID} = 0.1 V,		260	500	mV
V_{ICR}	Common-mode input voltage, comparators					2		7	V
I_{IH}	High-level input current	EGS		$V_{I(EGS)}$ = 2.7 V			120	200	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 2.7 V				20	
I_{IL}	Low-level input current	EGS		$V_{I(EGS)}$ = 0.4 V				−20	μA
		W/$\overline{R}$		$V_{I(W/\overline{R})}$ = 0.4 V				−400	
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 5.5 V,	No signal		22	31	mA
	Response time			100-mV step,	5-mV overdrive		50		ns
t_w	Pulse duration of one-shots (TP, RDP)			R_{ext} = 5 kΩ,	C_{ext} = 100 pF		360		ns
				R_{ext} = 20 kΩ,	C_{ext} = 33 pF		460		

PARAMETER MEASUREMENT INFORMATION



$V_{OO} = V_{OD}$ with $V_{ID} = 0$

$V_{OPP} = V_{OD}$ with $V_{ID} = 1$ V

$A_{VD} = \frac{V_{OD}}{V_{ID}}$ with $V_{ID} = 20$ mV

$V_{OC} = \frac{V_{OC+} + V_{OC-}}{2}$ with $V_{ID} = 0$

FIGURE 1

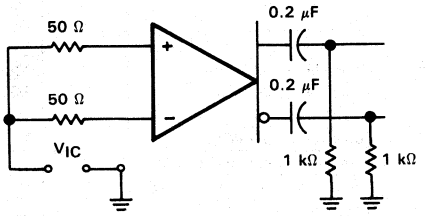


FIGURE 2

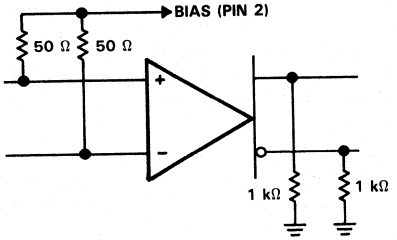


FIGURE 3

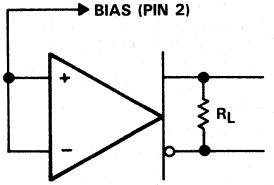


FIGURE 4

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

READ DATA PULSE DURATION
vs
CAPACITANCE

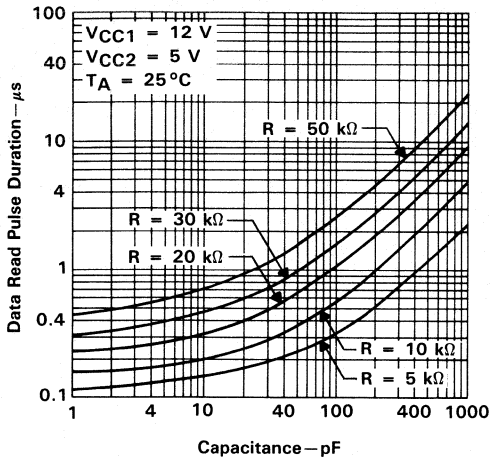


FIGURE 5

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
ELECTRONIC GAIN VOLTAGE

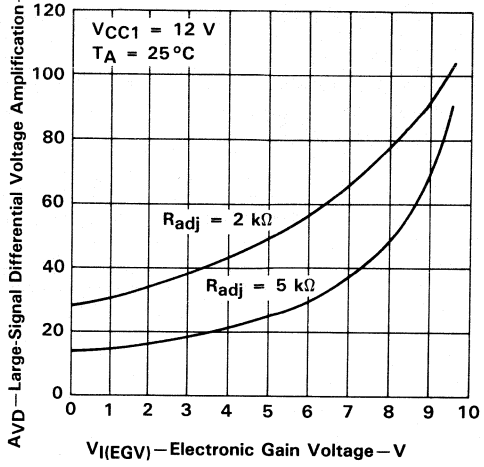


FIGURE 6

TYPICAL APPLICATION DATA

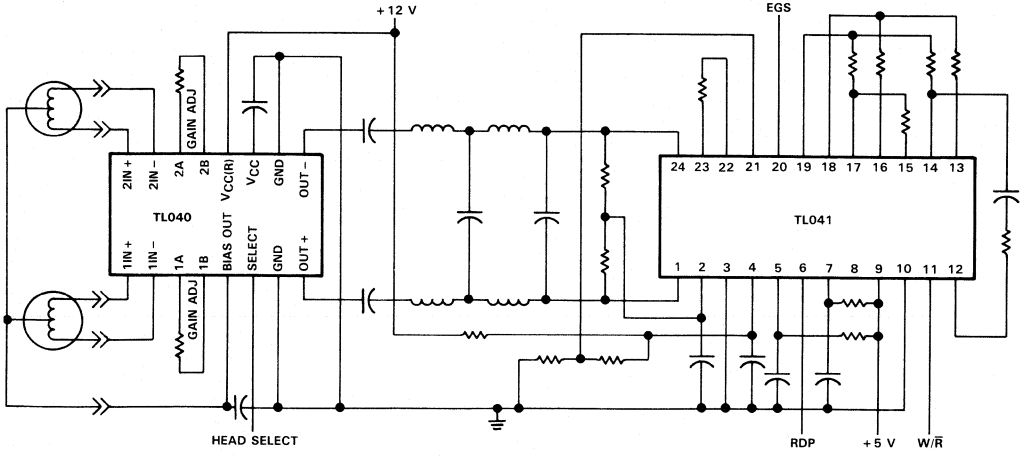
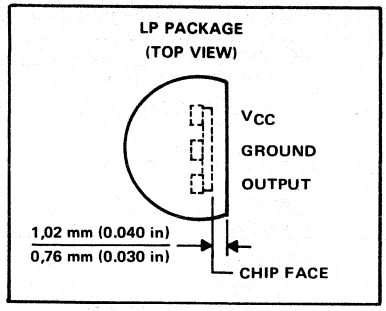


FIGURE 7. READ SIGNAL CIRCUIT FOR A STREAMING TAPE DRIVE

D2408, DECEMBER 1977, REVISED APRIL 1988

- **Magnetic-Field Sensing Hall-Effect Input**
- **On-Off Hysteresis**
- **Small Size**
- **Solid-State Technology**
- **Open-Collector Output**



description

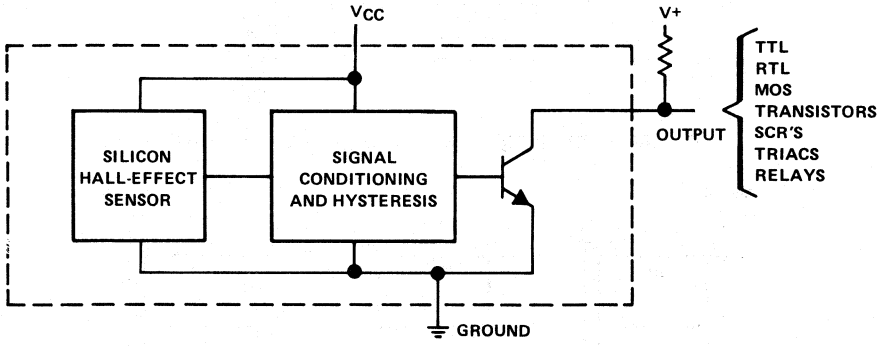
The TL170C is a low-cost magnetically operated electronic switch that utilizes the Hall Effect to sense steady-state magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

The TL170C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (T_A = 25°C)

FLUX DENSITY	OUTPUT
≤ −25 mT	Off
−25 mT < B < 25 mT	Undefined
≥ 25 mT	On

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1. Voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V ± 5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive-going magnetic flux density†			25°C			25	mT‡
				0°C to 70°C			35	
B_{T-}	Threshold of negative-going magnetic flux density†			25°C	−25§			mT‡
				0°C to 70°C	−35§			
$B_{T+} - B_{T-}$	Hysteresis			0°C to 70°C		20		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V		0°C to 70°C			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 16 mA		0°C to 70°C			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V	Output low	0°C to 70°C			6	mA
			Output high				4	

†Threshold values are those levels of magnetic flux denisity at which the output changes state. For the TL170C, a level more positive than B_{T+} causes the output to go to a low level and a level more negative than B_{T-} causes the output to go to a high level. See Figures 1 and 2.

‡The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.

§The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for flux-density threshold levels only.

The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

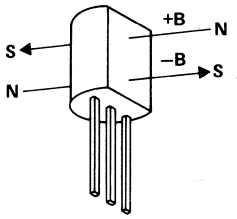
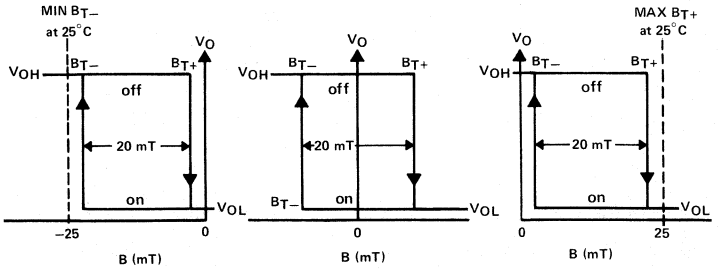


FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY



The positive-going threshold (B_{T+}) may be a negative or positive B level at which a positive-going (decreasing negative or increasing positive) flux density results in the TL170 output turn-on. The negative-going threshold is a positive or negative B level at which a negative-going (decreasing positive or increasing negative) flux density results in the TL170 turning off.

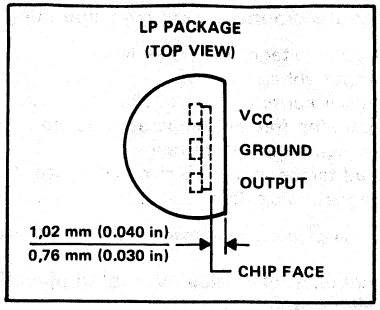
FIGURE 2. REPRESENTATIVE CURVES OF V_O vs B

4 Special Functions

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2490, AUGUST 1977—REVISED APRIL 1988

- **Magnetic-Field Sensing Hall-Effect Input**
- **On-Off Hysteresis**
- **Small Size**
- **Solid-State Technology**
- **Open-Collector Output**
- **Normally Off Switch**



description

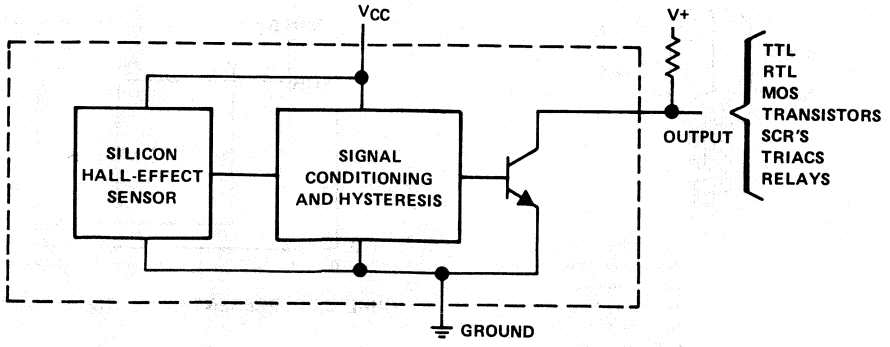
The TL172C is a low-cost magnetically operated normally off electronic switch that utilizes the Hall Effect to sense the presence of a magnetic field. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. A magnetic field of sufficient strength in the positive direction will cause the TL172C output to be in a low-impedance state. Otherwise, the output will present a high impedance. The output of this circuitry connected to many different types of electronic components.

The TL172C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE

FLUX DENSITY	OUTPUT
≤ 10 mT	Off
10 mT < B < 60 mT	Undefined
≥ 60 mT	On

functional block diagram



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

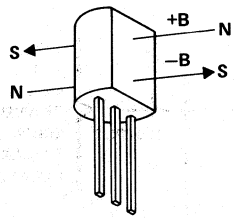
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over rated operating free-air temperature range, V_{CC} = 5 V ± 5% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive-going magnetic flux density†				60	mT‡
B_{T-}	Threshold of negative-going magnetic flux density†		10			mT‡
$B_{T+} - B_{T-}$	Hysteresis			23		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 16 mA			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V			6	mA

†Threshold values are those levels of magnetic flux density at which the output changes state. For the TL172C, a level more positi than B_{T+} causes the output to go to a low level, and a level more negative than B_{T-} causes the output to go to a high level. See Figur 1 and 2.
‡The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux amanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

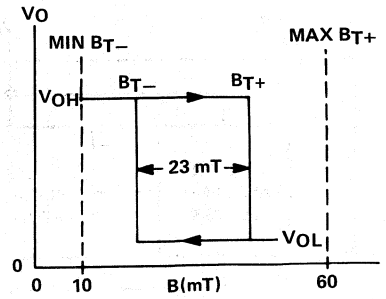
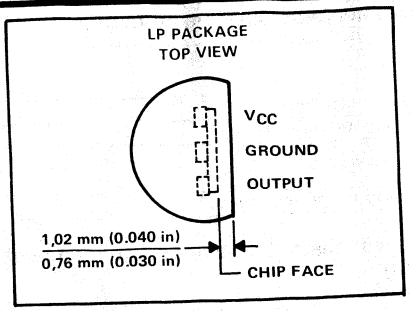


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2526, MARCH 1979—REVISED APRIL 1988

- **Output Voltage Linear with Applied Magnetic Field**
- **Sensitivity Constant Over Wide Operating Temperature Range**
- **Solid-State Technology**
- **Three-Terminal Device**
- **Senses Static or Dynamic Magnetic Fields**

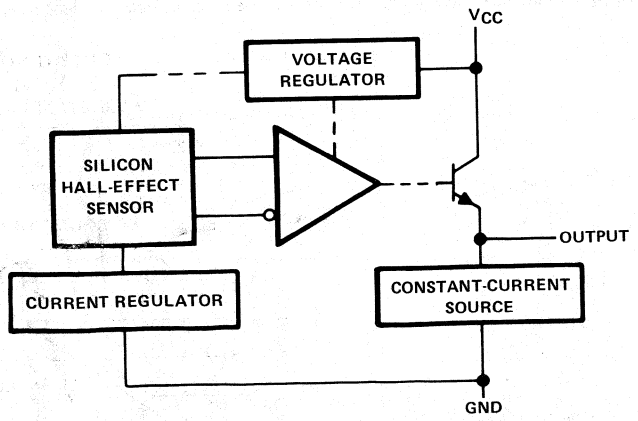


description

The TL173I and TL173C are low-cost magnetic-field sensors designed to provide a linear output voltage proportional to the magnetic field they sense. These monolothic circuits incorporate a Hall element as the primary sensor along with a voltage reference and a precision amplifier. Temperature stabilization and internal trimming circuitry yield a device that features high overall sensitivity accuracy with less then 5% error over its operating temperature range.

The TL173I is characterized for operation from −20°C to 85°C. The TL173C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range: TL173I	−20°C to 85°C
TL173C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Magnetic flux density	unlimited

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C.

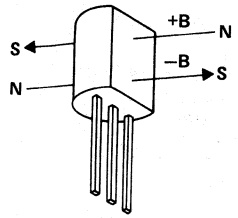
recommended operating conditions

		TL173I			TL173C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		10.8	12	13.2	10.8	12	13.2	V
Magnetic flux density, B				±50			±50	mT
Output current, I_O	Sink			0.5			0.5	mA
	Source			−2			−2	
Operating free-air temperature, T_A		−20		85	0		70	°C

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_O	Output voltage	I_O = −2 mA to 0.5 mA, B = 0 mT§,	T_A = 25°C	5.8	6	6.2	V
K_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)				18		mV/V
S	Magnetic sensitivity ($\Delta V_O/\Delta B$)	B = −50 to 50 mT§,	T_A = 25°C	13.5	15	18	V/T§
ΔS	Magnetic sensitivity change with temperature	ΔT_A = 25°C to MIN or MAX				±5	%
I_{CC}	Supply current	B = 0 mT§,	I_O = 0		8	12	mA
f_{max}	Maximum operating frequency				100		kHz

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Typical values are at V_{CC} = 12 V and T_A = 25°C.
§ The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten, e.g., 50 millitesla = 500 gauss.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

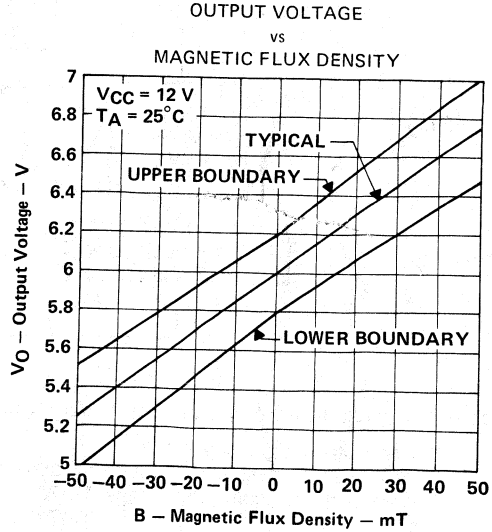


FIGURE 2

TEXAS INSTRUMENTS
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TYPICAL APPLICATION DATA

The circuit in Figure 3 may be used to set the output voltage at zero field strength to exactly 6 V (using R1), and to set the sensitivity to exactly −15 V/T (using R2), as depicted in Figure 4.

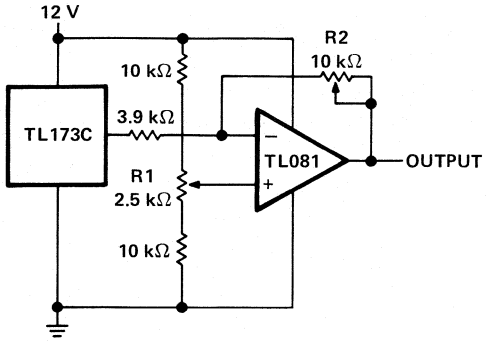


FIGURE 3. COMPENSATION CIRCUIT

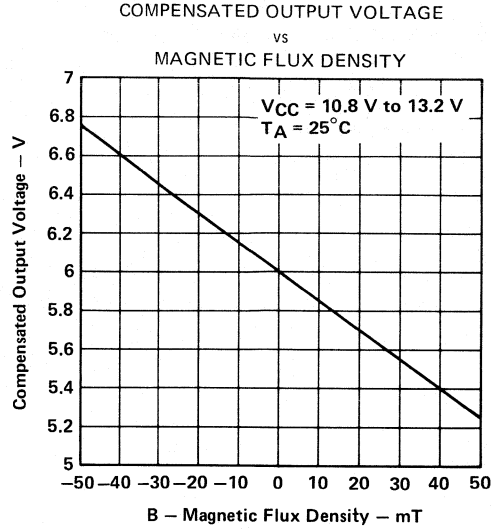


FIGURE 4

D956, JUNE 1976—REVISED FEBRUARY 1989

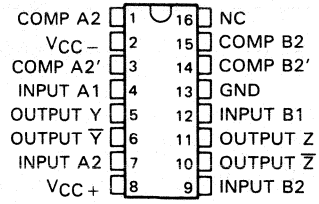
- **Excellent Dynamic Range**
- **Wide Bandwidth**
- **Built-In Temperature Compensation**
- **Log Linearity (30 dB Sections) . . . 1 dB Typ**
- **Wide Input Voltage Range**

description

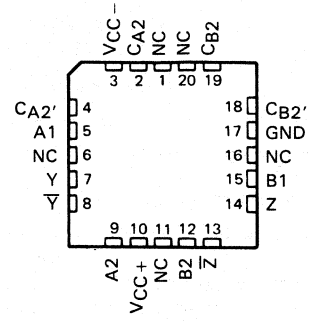
This monolithic amplifier circuit contains four 30-dB logarithmic stages. Gain in each stage is such that the output of each stage is proportional to the logarithm of the input voltage over the 30-dB input voltage range. Each half of the circuit contains two of these 30-dB stages summed together in one differential output that is proportional to the sum of the logarithms of the input voltages of the two stages. The four stages may be interconnected to obtain a theoretical input voltage range of 120 dB. In practice, this permits the input voltage range to be typically greater than 80 dB with log linearity of ± 0.5 dB (see application data). Bandwidth is from dc to 40 MHz.

This circuit is useful in military weapons systems, broadband radar, and infrared reconnaissance systems. It serves for data compression and analog compensation. This logarithmic amplifier is used in log IF circuitry as well as video and log amplifiers. The TL441AM is characterized for operation over the full military temperature range of −55°C to 125°C.

J PACKAGE
(TOP VIEW)

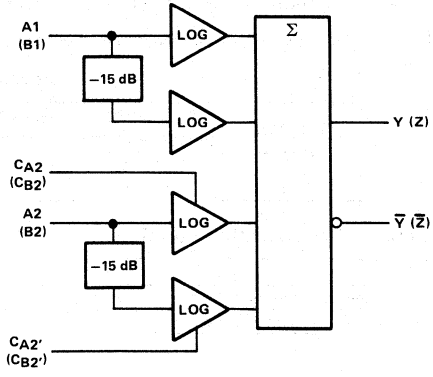


FK PACKAGE
(TOP VIEW)



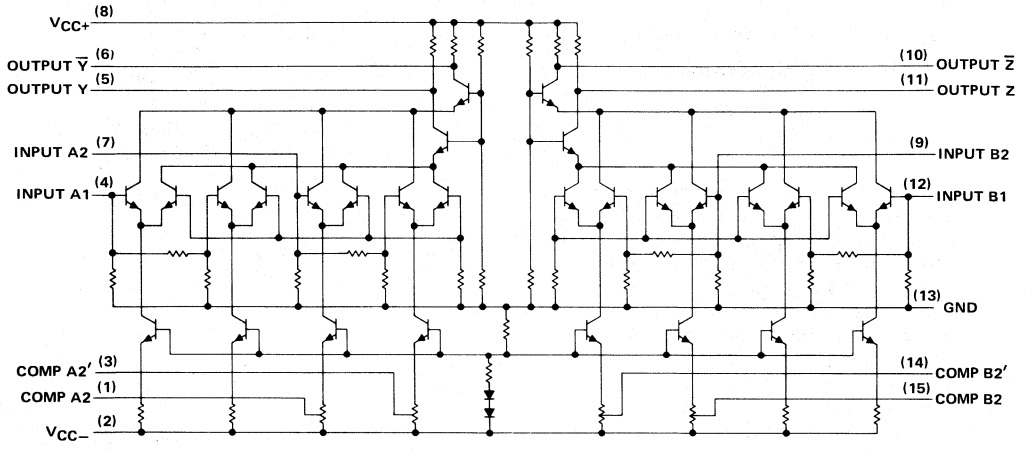
NC—No internal connection

functional block diagram (one half)



$Y \propto \log A1 + \log A2$; $Z \propto \log B1 + \log B2$
where: A1, A2, B1, and B2 are in dBV, 0 dBV = 1 V.
C_{A2}, $C_{A2'}$, C_{B2}, and $C_{B2'}$ are detector compensation inputs.

schematic



Pin numbers shown are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltages (see Note 1): V_{CC+} . . . . . 8 V
V_{CC-} . . . . . −8 V
Input voltage (see Note 1) . . . . . 6 V
Output sink current (any one output) . . . . . 30 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C

NOTE: 1. All voltages, except differential output voltages, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
J	500 mW	11.0 mW/°C	104°C	500 mW	275 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Peak-to-peak input voltage for each 30-dB stage	0.01		1	V
Operating free-air temperature, T_A	−55		125	°C

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electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = 25°C

PARAMETER	TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage	1		±25	±70	mV
Quiescent output voltage	2	5.45	5.6	5.85	V
DC scale factor (differential output), each 3-dB stage, −35 dBV to −5 dBV	3	7	8	11	mV/dB
AC scale factor (differential output)			8		mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	3		1	2.6	dB
Input impedance			500		Ω
Output impedance			200		Ω
Rise time, 10% to 90% points, C_L = 24 pF	4		20	35	ns
Supply current from V_{CC+}	2	14.5	18.5	23	mA
Supply current from V_{CC-}	2	−6	−8.5	−10.5	mA
Power dissipation	2	123	162	201	mW

electrical characteristics over operating free-air temperature range, V_{CC+} = 6 V, V_{CC-} = −6 V (unless otherwise noted)

PARAMETER		TEST FIGURE	MIN	TYP	MAX	UNIT
Differential output offset voltage		1			±100	mV
Quiescent output voltage		2	5.3		5.85	V
DC scale factor (differential output) each 30-dB stage, −35 dBV to −5 dBV		3	7		11	mV/dB
DC error at −20 dBV (midpoint of −35 dBV to −5 dBV range)	T_A = −55°C	3			4	dB
	T_A = 125°C				3	
Supply current from V_{CC+}		2	10		31	mA
Supply current from V_{CC-}		2	−4.5		−15	mA
Power dissipation		2	87		276	mW

PARAMETER MEASUREMENT INFORMATION

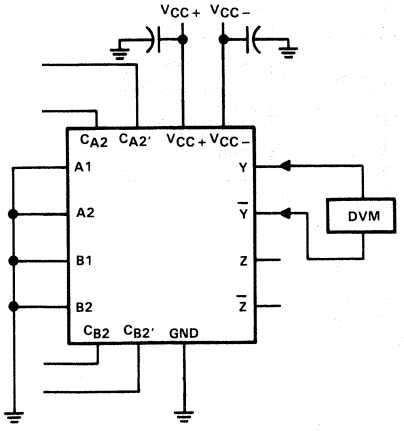


FIGURE 1

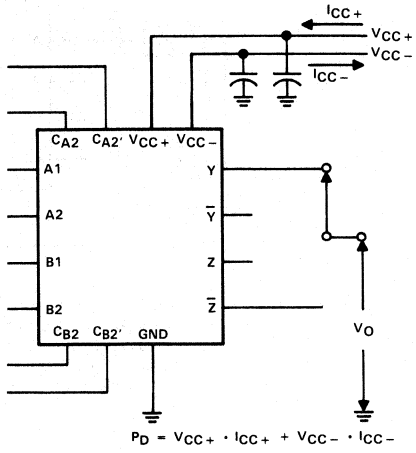
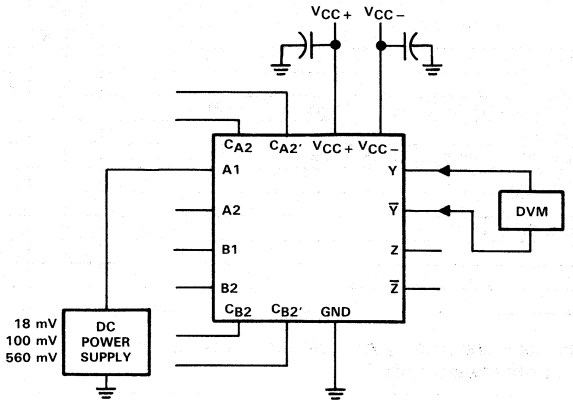


FIGURE 2

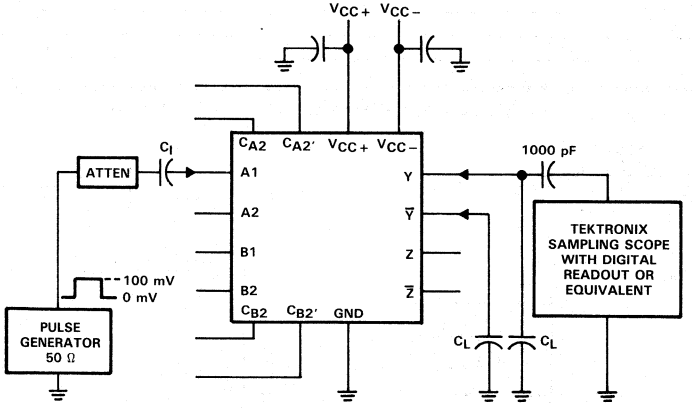
PARAMETER MEASUREMENT INFORMATION



$$\text{Scale Factor} = \frac{[V_{out(560\ mV)} - V_{out(18\ mV)}]\ mV}{30\ dB}$$

$$\text{Error} = \frac{|V_{out(100\ mV)} - 0.5\ V_{out(560\ mV)} - 0.5\ V_{out(18\ mV)}|}{\text{Scale Factor}}$$

FIGURE 3



NOTES: A. The input pulse has the following characteristics: t_w = 200 ns, $t_r \leq 2$ ns, $t_f \leq 2$ ns, PRR ≤ 10 MHz.
B. Capacitor C_I consists of three capacitors in parallel: 1 μF, 0.1 μF, and 0.01 μF.
C. C_L includes probe and jig capacitance.

FIGURE 4

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TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

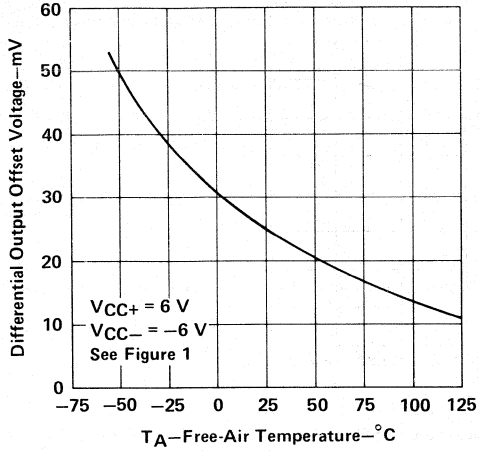

FIGURE 5

QUIESCENT OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

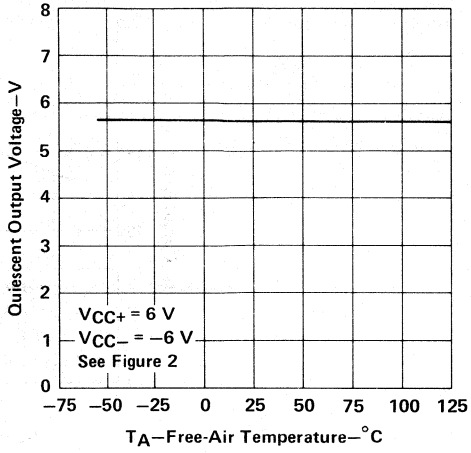

FIGURE 6

DC SCALE FACTOR
vs
FREE-AIR TEMPERATURE

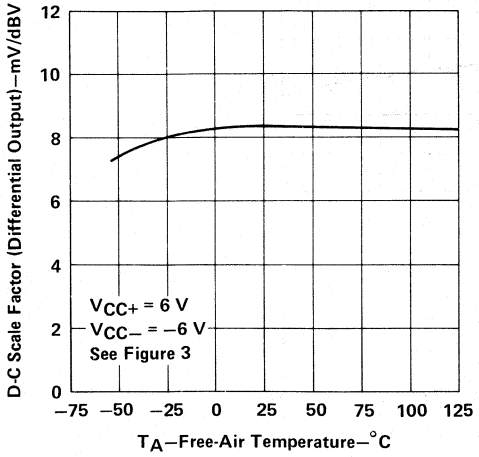

FIGURE 7

DC ERROR
vs
FREE-AIR TEMPERATURE

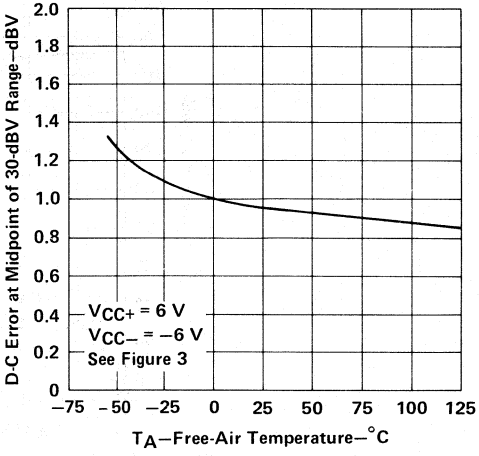

FIGURE 8

TYPICAL CHARACTERISTICS

OUTPUT RISE TIME
vs
LOAD CAPACITANCE

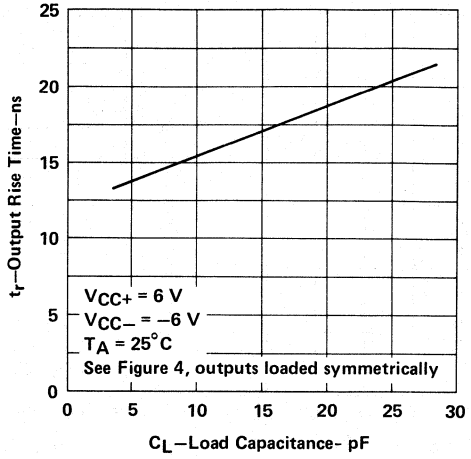

FIGURE 9

POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

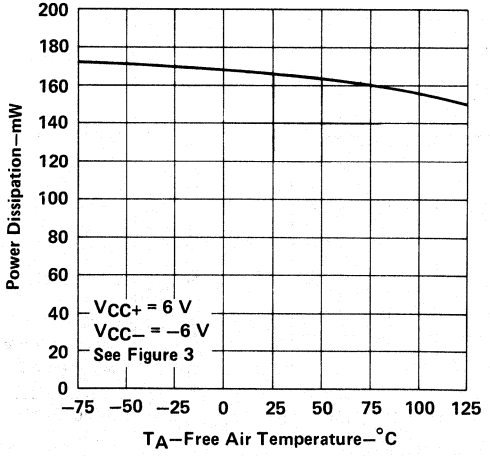

FIGURE 10

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TYPICAL APPLICATION DATA

Although designed for high-performance applications such as broadband radar infrared detection and weapons systems, this device has a wide range of applications in data compression and analog computation.

basic logarithmic function

The basic logarithmic response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. This relationship is given in the equation:

$$m \cdot V_{BE} = \ln [(I_C + I_{CES})/I_{CES}]$$

where:

I_C = collector current
I_{CES} = collector current at $V_{BE} = 0$
$m = q/kT$ (in V^{-1})
V_{BE} = base-emitter voltage

The differential input amplifier allows dual-polarity inputs, is self-compensating for temperature variations, and is relatively insensitive to common-mode noise.

functional block diagram

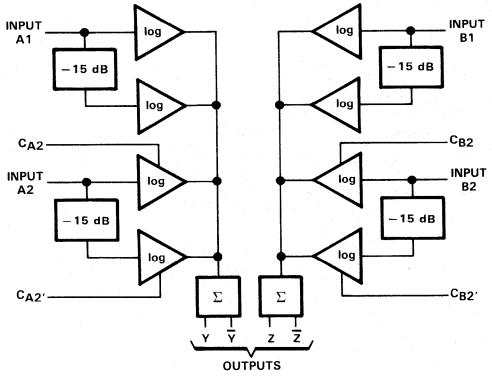


FIGURE 11

logarithmic sections

As can be seen from the schematic, there are eight differential pairs. Each pair is a 15-dB log subsection, and each input feeds two pairs for a range of 30-dB per stage.

Four compensation points are made available to allow slight variations in the gain (slope) of the two individual 15-dB stages of input A2 and B2. By slightly changing the voltage on any of the compensation pins from its quiescent value, the gain of that particular 15-dB stage can be adjusted to match the other 15-dB stage in the pair. The compensation pins may also be used to match the transfer characteristics of input A2 to A1 or B2 to B1.

The log stages in each half of the circuit are summed by directly connecting their collectors together and summing through a common-base output stage. The two sets of output collectors are used to give two log outputs, Y and $\overline{Y}$ (or Z and $\overline{Z}$) which are equal in amplitude but opposite in polarity. This increases the versatility of the device.

By proper choice of external connections, linear amplification, linear attentuation, and many different applications requiring logarithmic signal processing are possible.

input levels

The recommended input voltage range of any one stage is given as 0.01 V to 1 V. Input levels in excess of 1 V may result in a distorted output. When several log sections are summed together, the distorted area of one section overlaps with the next section and the resulting distortion is insignificant. However, there is a limit to the amount of overdrive that may be applied. As the input drive reaches ±3.5 V, saturation occurs, clamping the collector-summing line and severely distorting the output. Therefore, the signal to any input must be limited to approximately ±3 V to ensure a clean output.

output levels

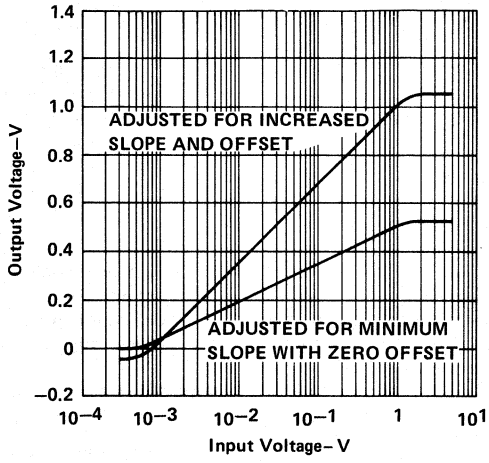
Differential-output-voltage levels are low, generally less than 0.6 V. As demonstrated in Figure 12, the output swing and the slope of the output response can be adjusted by varying the gain by means of the slope control. The coordinate origin may also be adjusted by positioning the offset of the output buffer.

TYPICAL APPLICATION DATA

circuits

Figures 12 through 19 show typical circuits using this logarithmic amplifier. Operational amplifiers not otherwise designated are TLC271. For operation at higher frequencies, the TL592 is recommended instead of the TLC271.

TYPICAL TRANSFER
CHARACTERISTICS



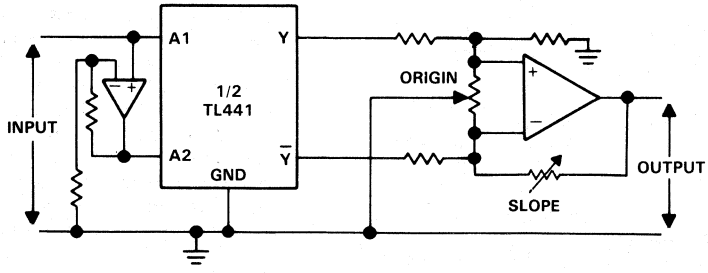


FIGURE 12. OUTPUT SLOPE AND ORIGIN ADJUSTMENT

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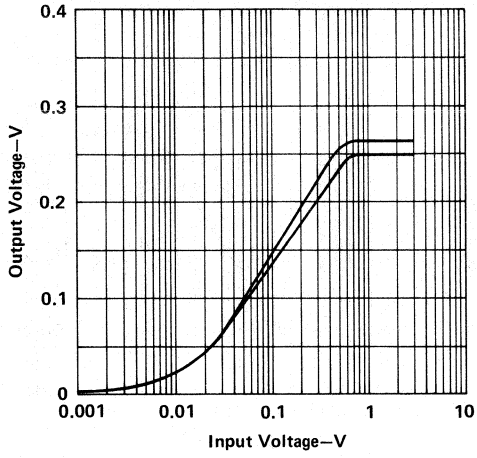
TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
OF TWO TYPICAL INPUT STAGES



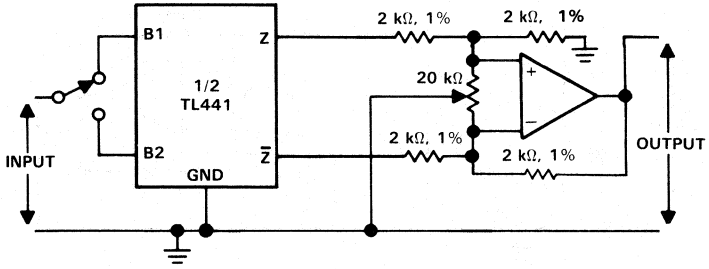
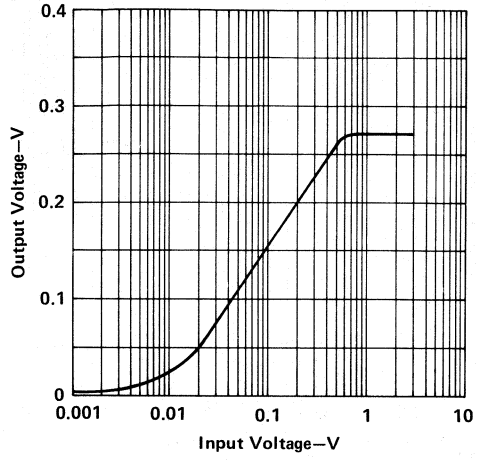


FIGURE 13. UTILIZATION OF SEPARATE STAGES

TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS
WITH BOTH SIDES PARALLELED



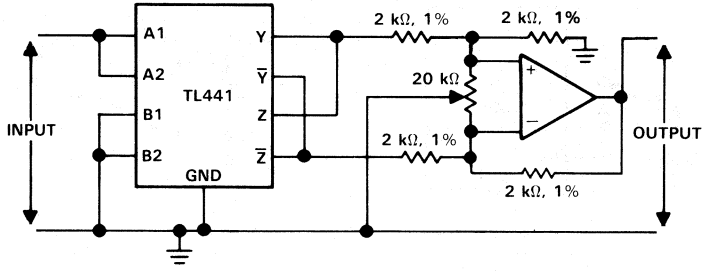


FIGURE 14. UTILIZATION OF PARALLELED INPUTS

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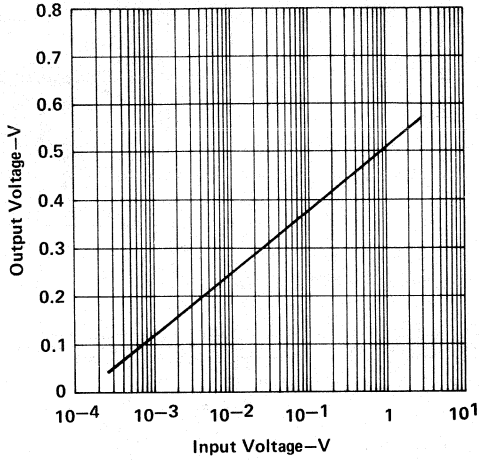
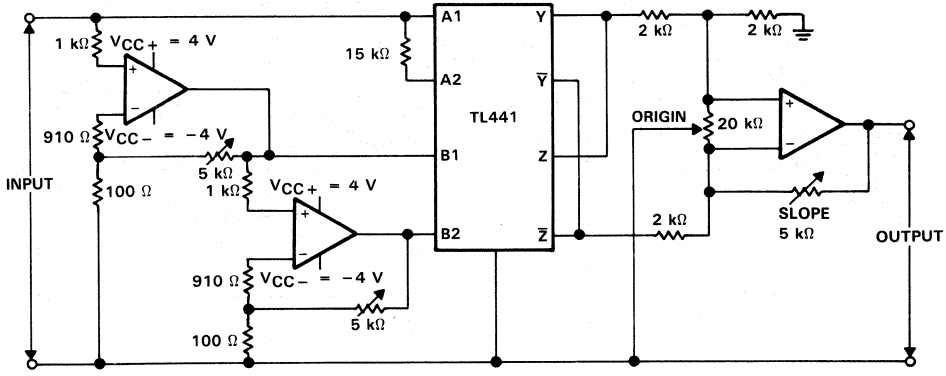
TYPICAL APPLICATION DATA

TRANSFER CHARACTERISTICS

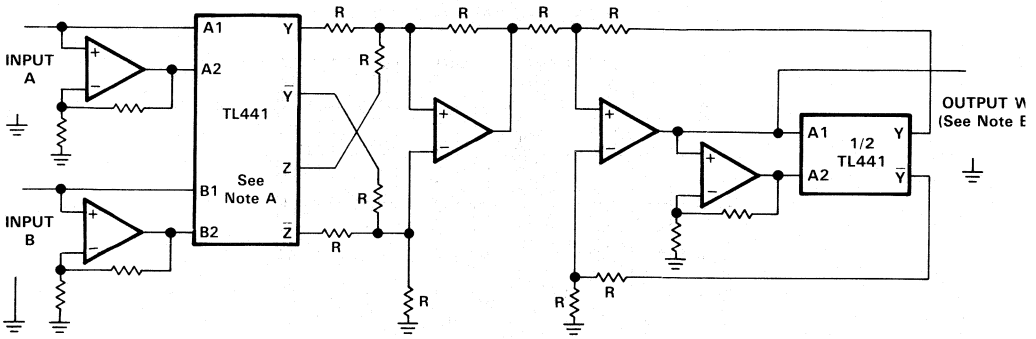




NOTES: A. Inputs are limited by reducing the supply voltages for the input amplifiers to ±4 V.
B. The gains of the input amplifiers are adjusted to achieve smooth transistions.

Figure 15. LOGARITHMIC AMPLIFIER WITH INPUT VOLTAGE RANGE GREATER THAN 80 dB

TYPICAL APPLICATION DATA

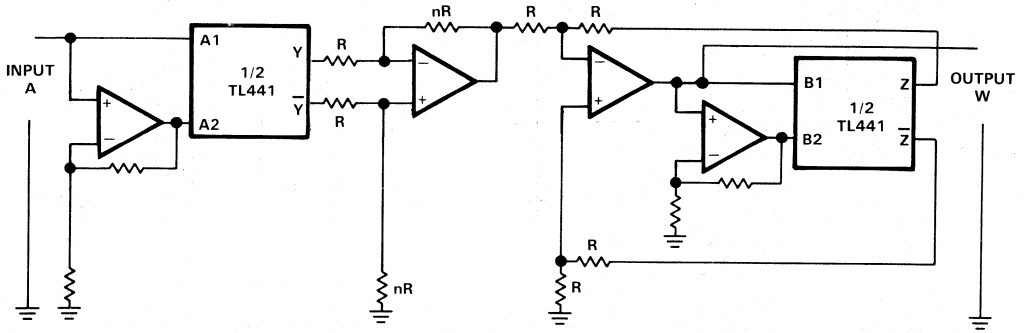


NOTES: A. Connections shown are for multiplication. For division, Z and $\bar{Z}$ connections are reversed.
B. Output W may need to be amplified to give actual product or quotient of A and B.
C. R designates resistors of equal value, typically 2 kΩ to 10 kΩ.

Multiplication: $W = A \cdot B \Rightarrow \log W = \log A + \log B$, or $W = a^{(\log_a A + \log_a B)}$

Division: $W = A/B \Rightarrow \log W = \log A - \log B$, or $W = a^{(\log_a A + \log_a B)}$

FIGURE 16. MULTIPLICATION OR DIVISION



NOTE: R designates resistors of equal value, typically 2 kΩ to 10 kΩ. The power to which the input variable is raised is fixed by setting nR. Output W may need to be amplified to give the correct value.

Exponential: $W = A^n \Rightarrow \log W = n \log A$, or $W = a^{(n \log_a A)}$

FIGURE 17. RAISING A VARIABLE TO A FIXED POWER

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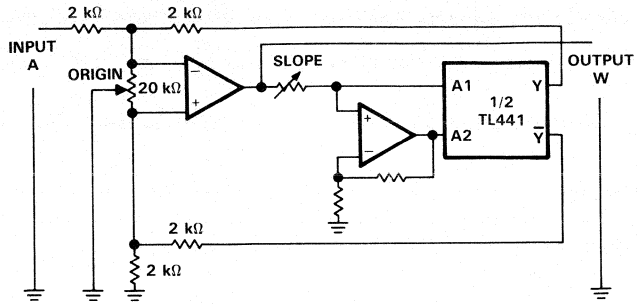
TYPICAL APPLICATION DATA



NOTE: Adjust the slope to correspond to the base "a".
Exponential to any base: W = a

FIGURE 18. RAISING A FIXED NUMBER TO A VARIABLE POWER

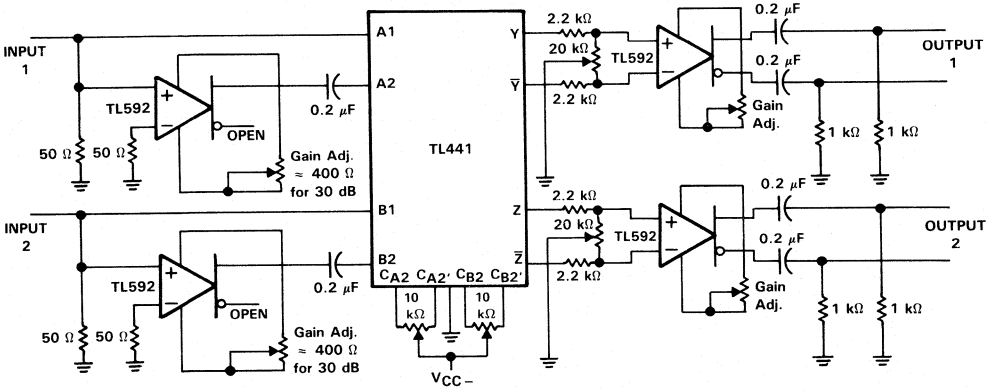
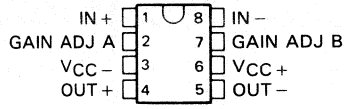


FIGURE 19. DUAL-CHANNEL RF LOGARITHMIC AMPLIFIER WITH 50-dB INPUT RANGE PER CHANNEL AT 10 MHz

D2668, NOVEMBER 1983—REVISED MAY 1988

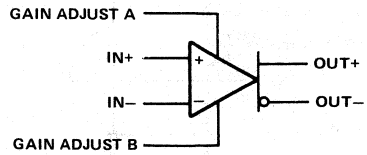
- **8-Pin Version of NE592 . . . Saves Printed Circuit Board Space**
- **Adjustable Gain to 400**
- **No Frequency Compensation Required**
- **Adjustable Passband**

D OR P PACKAGE
(TOP VIEW)



DEVICE TYPE	TEMPERATURE RANGE	A_{VD} RANGE (GAIN OPTION 1)
TL592	0°C to 70°C	250—600
TL592A	0°C to 70°C	400—600

symbol



description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs.

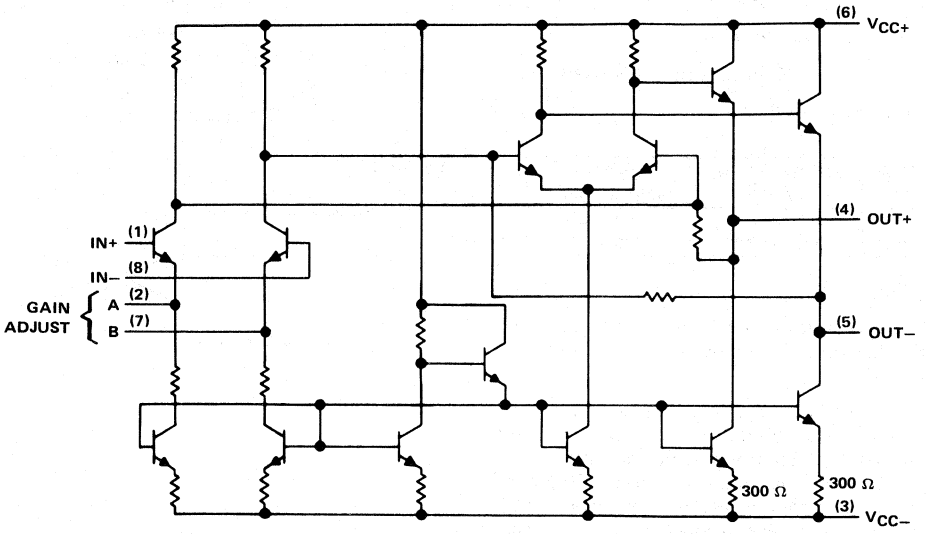
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of nominally 400 may be selected without external components, or amplification may be adjusted from 0 to approximately 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The TL592 and TL592A are characterized for operation from 0°C to 70°C.

schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} (see Note 1) . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation at 70°C . . . . . 500 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

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electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			GAIN OPTION†	TL592			TL592A			UNIT
							MIN	TYP	MAX	MIN	TYP	MAX	
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_L = 2 kΩ		25°C	1	250	400	600	400	440	600	V/V
					0°C to 70°C		250		600	400		600	
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V		25°C	1		50			50		MHz
I_{IO}	Input offset current		V_{IC} = 0		25°C	1 or 2		0.4	5		0.4	5	μA
					0°C to 70°C				6			6	
I_{IB}	Input bias current		V_{IC} = 0		25°C	1 or 2		9	30		10	30	μA
					0°C to 70°C				40			40	
V_{ICR}	Common-mode input voltage range	3			25°C	1 or 2	±1			±1			V
					0°C to 70°C		±1			±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_L = ∞		25°C	2		0.35	0.75		0.35	0.75	V
					0°C to 70°C				1.5			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ		25°C	1	3	4		3	4		V
					0°C to 70°C		2.8			2.8			
z_i	Input impedance		V_{OD} = 1 V, f = 1 kHz to 10 MHz		25°C	1		4			3.6		kΩ
					0°C to 70°C			3.6			3.3		
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V	f = 100 kHz	25°C	1	60	86		60	86		dB
				f = 5 MHz				60			60		
				f = 100 kHz	0°C to 70°C		50			50			
				f = 5 MHz				60			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V		25°C	1	50	70		50	70		dB
					0°C to 70°C		50			50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C	1 or 2		12			12		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C	2		7.5			7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C	2		10.5			10.5		ns
$I_{sink(max)}$	Maximum output sink current					1, 2, or 3	3	4		3	4		mA
I_{CC}	Supply current		No load, No signal		25°C	1 or 2		18	24		19	24	mA
					0°C to 70°C				27			27	

†The gain option is selected as follows:
Gain Option 1 . . . Gain adjust pin A is connected to pin B.
Gain Option 2 . . . Gain adjust pins A and B are open.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

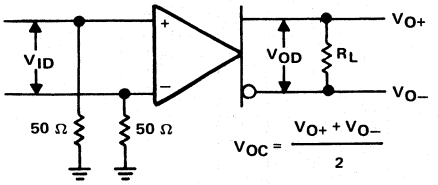


FIGURE 1

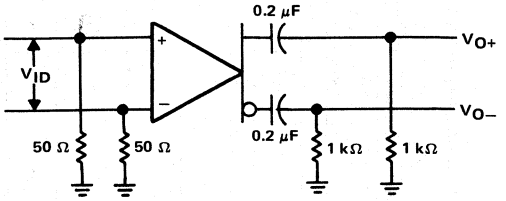


FIGURE 2

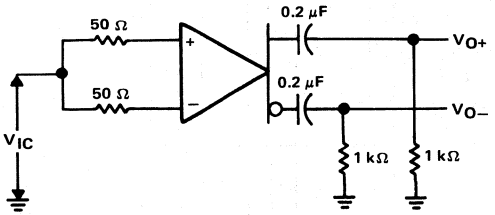


FIGURE 3

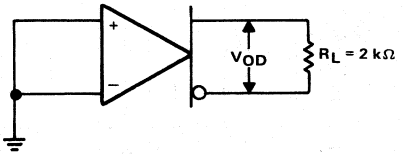


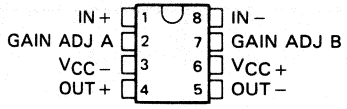
FIGURE 4

4 Special Functions

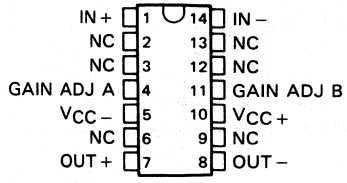
D2668, JUNE 1985—REVISED APRIL 1988

- **Adjustable Gain to 400 Typ**
- **No Frequency Compensation Required**
- **Low Noise . . . 3 μV Typ V_n**

D8† OR P PACKAGE
(TOP VIEW)



D14† OR N PACKAGE
(TOP VIEW)



NC—No internal connection

†D8 and D14 are the codes used to differentiate the 8-pin and 14-pin versions, respectively.

description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs. It features internal series-shunt feedback that provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

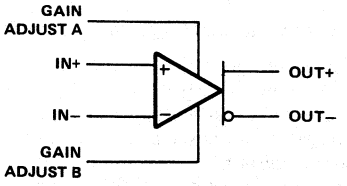
The differential gain is typically 400 when the gain adjust pins are connected together, or amplification may be adjusted from near 0 to 400 by the use of a single external resistor connected between the gain adjustment pins A and B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disk-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general-purpose video and pulse amplifiers.

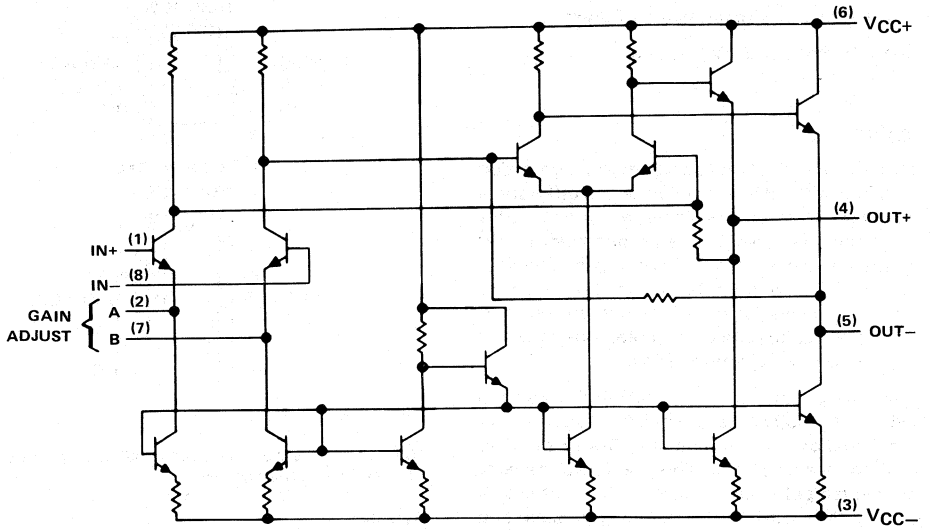
The device achieves low equivalent noise voltage through special processing and a new circuit layout incorporating input transistors with low base resistance.

The TL592B is characterized for operation from 0°C to 70°C.

symbol



schematic



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 8 V
Supply voltage, V_{CC-} . . . . . −8 V
Differential input voltage . . . . . ±5 V
Voltage range, any input . . . . . V_{CC+} to V_{CC-}
Output current . . . . . 10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values except differential input voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING
D8	530 mW	5.8 mW/°C	59°C	464 mW
D14	530 mW	N/A	N/A	530 mW
N	530 mW	N/A	N/A	530 mW
P	530 mW	N/A	N/A	530 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	3	6	8	V
Supply voltage, V_{CC-}	−3	−6	−8	V
Operating free-air temperature, T_A	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC+} = 6 V, V_{CC-} = −6 V, R_L = 2 kΩ (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 0	R_L = 2 kΩ,	25°C	300	400	500	V/V
					0°C to 70°C	250		600	
A_{VD2}	Large-signal differential voltage amplification	1	V_{OPP} = 3 V, R_{AB} = 1 kΩ	R_L = 2 kΩ,	25°C		13		V/V
BW	Bandwidth (−3 dB)	2	V_{OPP} = 1 V,	R_{AB} = 0	25°C		50		MHz
I_{IO}	Input offset current				25°C		0.4	5	μA
					0°C to 70°C			6	
I_{IB}	Input bias current				25°C		9	30	μA
					0°C to 70°C			40	
V_{ICR}	Common-mode input voltage range	3			25°C	±1			V
					0°C to 70°C	±1			
V_{OC}	Common-mode output voltage	1	R_L = ∞		25°C	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1	V_{ID} = 0, R_{AB} = ∞, R_L = ∞		25°C		0.35	0.75	V
					0°C to 70°C			1.5	
V_{OPP}	Peak-to-peak output voltage swing	1	R_L = 2 kΩ	R_{AB} = 0	25°C	3	4		V
					0°C to 70°C	2.8			
r_i	Input resistance		V_{OD} = 1 V,	R_{AB} = 0	25°C		4		kΩ
					0°C to 70°C		3.6		
r_o	Output resistance				0°C to 70°C			30	Ω
C_i	Input capacitance				25°C		5		pF
CMRR	Common-mode rejection ratio	3	V_{IC} = ±1 V, R_{AB} = 0	f = 100 kHz	25°C	60	86		dB
				f = 5 MHz			60		
				f = 100 kHz	0°C to 70°C	50			
				f = 5 MHz			60		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	4	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V, R_{AB} = 0		25°C	50	70		dB
					0°C to 70°C	50			
V_n	Broadband equivalent input noise voltage	4	BW = 1 kHz to 10 MHz		25°C		3		μV
t_{pd}	Propagation delay time	2	ΔV_O = 1 V		25°C		7.5		ns
t_r	Rise time	2	ΔV_O = 1 V		25°C		10.5		ns
$I_{sink(max)}$	Maximum output sink current		V_{ID} = 1 V,	V_O = 3 V		3	4		mA
I_{CC}	Supply current		No load,	No signal	25°C		18	24	mA
					0°C to 70°C			27	

†R_{AB} is the gain-adjustment resistor connected between gain-adjust pins A and B. If not specified for a particular parameter, its value is irrelevant to that parameter.

PARAMETER MEASUREMENT INFORMATION

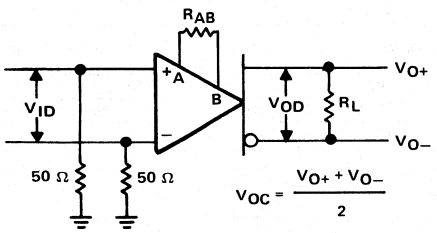


FIGURE 1

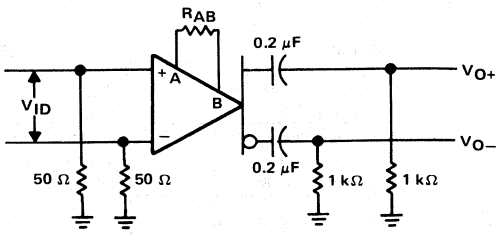


FIGURE 2

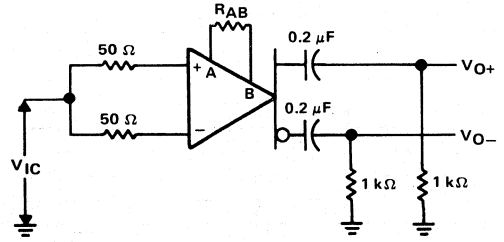


FIGURE 3

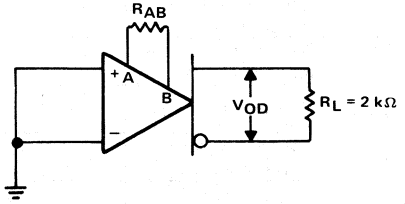


FIGURE 4

TYPICAL CHARACTERISTICS

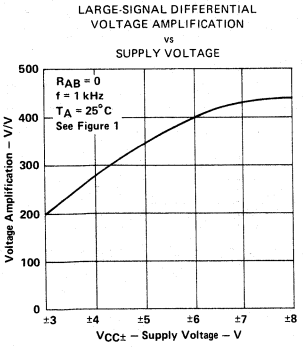


FIGURE 5

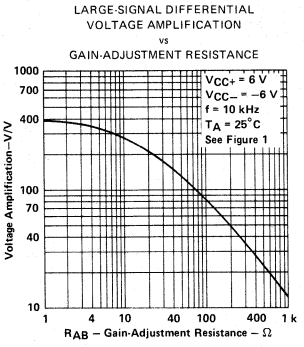


FIGURE 6

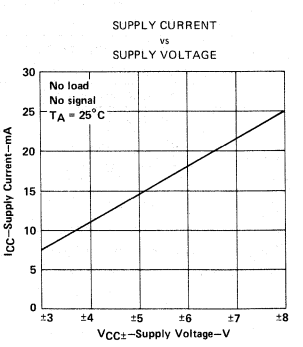


FIGURE 7

TEXAS INSTRUMENTS
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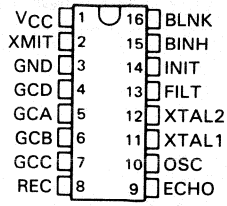
D2760, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28827**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interfaces to Electrostatic or Piezoelectric Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



lescription

The TL851 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL851 is designed for distance measurement from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 50-kHz electrostatic transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 8.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420 kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 3.8 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.3 feet from the transducer. If it is necessary to detect objects closer than 1.3 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

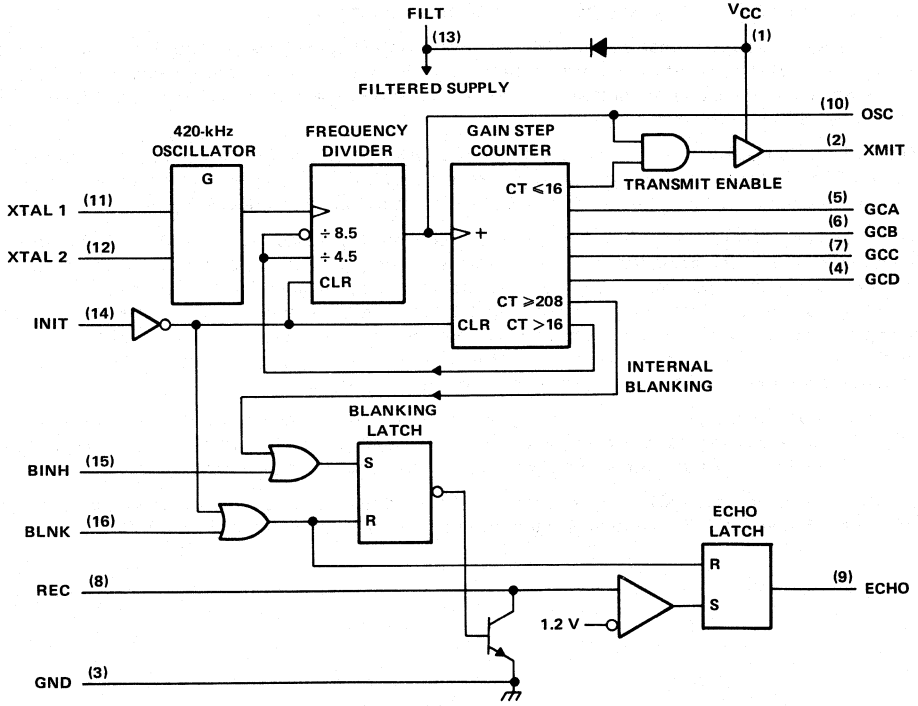
The threshold of the internal receive level detector is 1.2 volts. The TL851 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	GCD	GCC	GCB	GCA	TIME (ms) FROM INITIATE ↑†
0	L	L	L	L	2.38 ms
1	L	L	L	H	5.12 ms
2	L	L	L	L	7.87 ms
3	L	L	H	H	10.61 ms
4	L	H	L	L	13.35 ms
5	L	H	L	H	16.09 ms
6	L	H	H	L	18.84 ms
7	L	H	H	H	21.58 ms
8	H	L	L	L	27.07 ms
9	H	L	L	H	32.55 ms
10	H	L	H	L	38.04 ms
11	H	L	H	H	INIT ↓

† This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

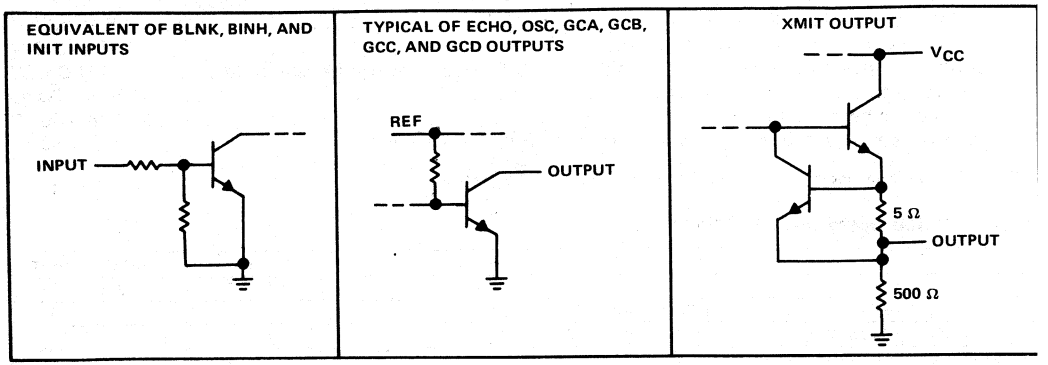
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to INIT high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current	BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}	ECHO, OSC, GCA, GCB, GCC, GCD	V_{OH} = 5.5 V			100	μA
Low-level output voltage, V_{OL}	ECHO, OSC, GCA, GCB, GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current	SMIT output	V_O = 1 V		−140		mA
Internal blanking interval	REC input			2.38‡		ms
Frequency during 16-pulse transmit period	OSC output			49.4‡		kHz
	XMIT output			49.4‡		
Frequency after 16-pulse transmit period	OSC output			93.3‡		kHz
	XMIT output			0		
Supply current, I_{CC}	During transmit period				260	mA
	After transmit period				55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



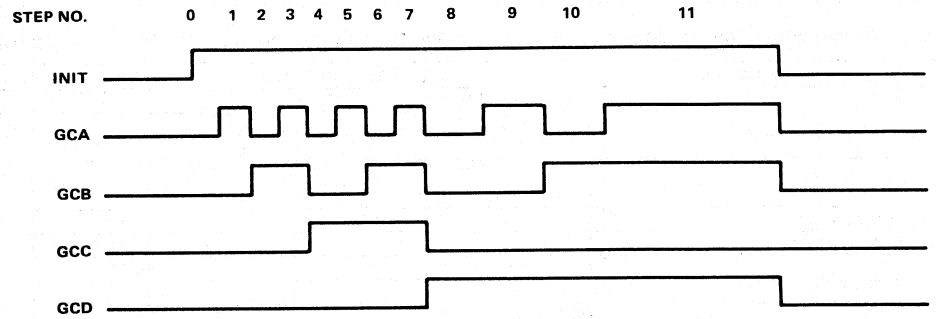


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

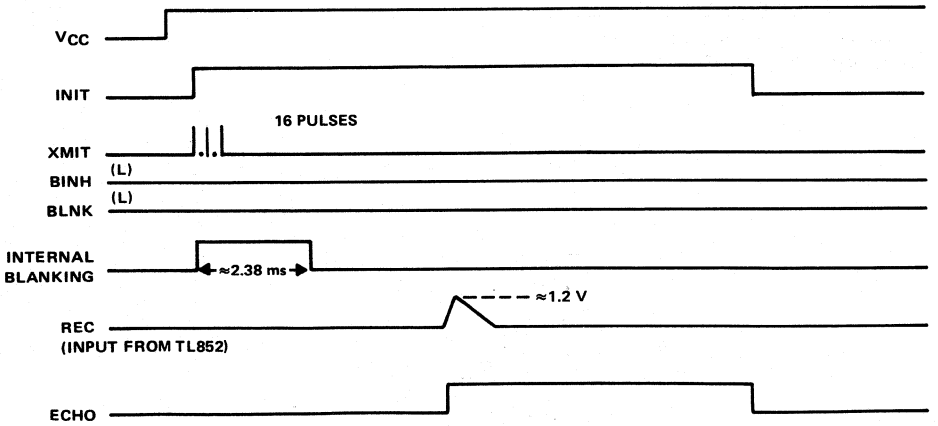


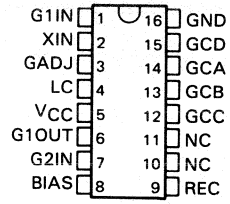
FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2779, SEPTEMBER 1983—REVISED MARCH 1988

- **Designed for Use with the TL851 in Sonar Ranging Modules Like the SN28827**
- **Digitally Controlled Variable-Gain Variable-Bandwidth Amplifier**
- **Operational Frequency Range of 20 kHz to 90 kHz**
- **TTL-Compatible**
- **Operates from Power Sources of 4.5 V to 6.8 V**
- **Interfaces to Electrostatic or Piezoelectric Transducers**
- **Overall Gain Adjustable with One External Resistor**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TL852 is an economical sonar ranging receiver integrated circuit for use with the TL851 control integrated circuit. A minimum of external components is required for operation, and this amplifier easily interfaces to Polaroid's 50-kilohertz electrostatic transducer. An external 68-kilohm ±5% resistor from pin 8 (Bias) to pin 16 (GND) provides the internal biasing reference. Amplifier gain can be set with a resistor from pin 1 (G1IN) to pin 3 (GADJ). Required amplifier gain will vary for different applications. Using the detect-level measurement circuit of Figure 1, a nominal peak-to-peak value of 230 millivolts input during gain step 2 is recommended for most applications. For reliable operation, a level no lower than 50 millivolts should be used. The recommended detect level of 230 millivolts can be obtained for most amplifiers with an R1 value between 5 kilohms and 20 kilohms.

Digital control of amplifier gain is provided with gain control inputs on pins 12 through 15. These inputs must be driven synchronously (all inputs stable within 0.1 microsecond) to avoid false receive output signals due to invalid logic counts. This can be done easily with the TL851 control IC. A plot showing relative gain for the various gain steps versus time can be seen in Figure 2. To dampen ringing of the 50-kilohertz electrostatic transducer, a 5-kilohm resistor from pin 1 (GAIN) to pin 2 (XIN) is recommended.

An external parallel combination of inductance and capacitance between pin 4 (LC) and pin 5 (V_{CC}) provides an amplifier with an externally controlled gain and Q. This not only allows control of gain to compensate for attenuation of signal with distance, but also maximizes noise and sidelobe rejection. Care must be taken to accurately tune the L-C combination at operating frequency or gain and Q will be greatly reduced at higher gain steps.

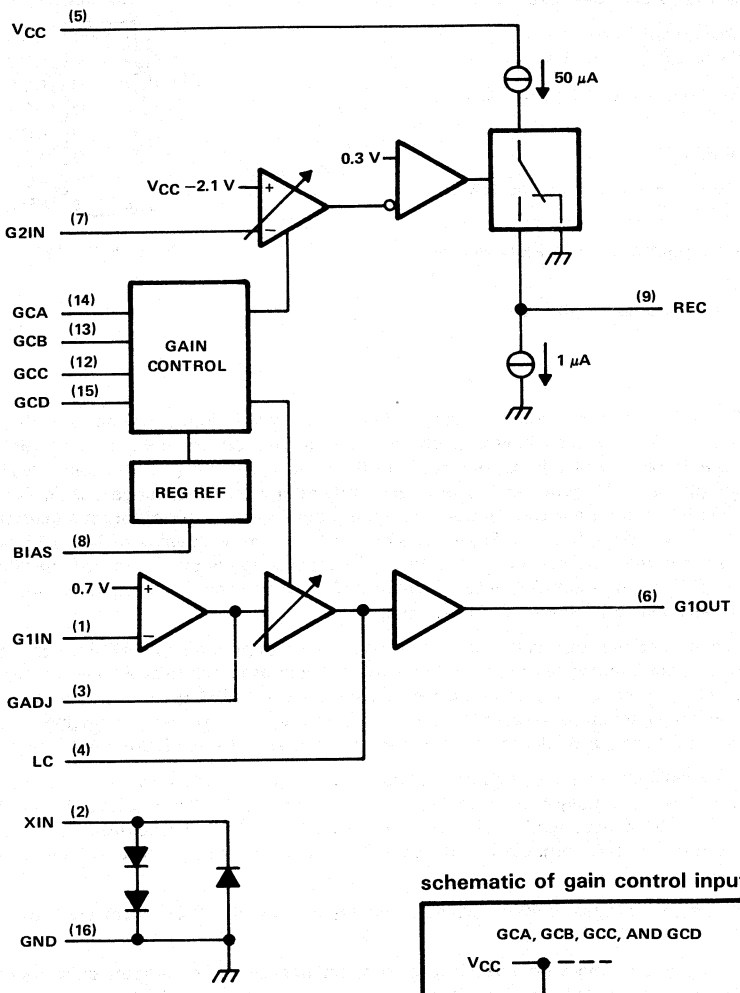
AC coupling between stages of the amplifier is accomplished with a 0.01-microfarad capacitor for proper biasing.

The receive output is normally held at a low level by an internal 1-microampere current source. When an input of sufficient amplitude is received, the output is driven alternately by the 1-microampere discharge current and a 50-microampere charging current. A 1000-picofarad capacitor is required from the receive output (pin 9) to ground (pin 16) to integrate the received signal so that one or two noise pulses will not be recognized.

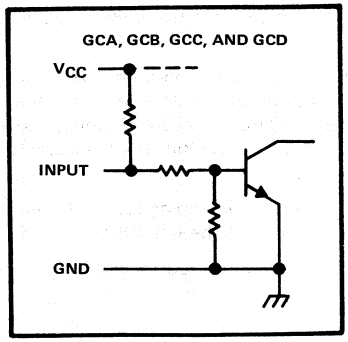
Pin 2 (XIN) provides clamping for the transformer secondary when used for transducer transmit drive as shown in Figure 4 of the SN28827 data sheet.

The TL852 is characterized for operation from 0°C to 40°C

functional block diagram



schematic of gain control inputs



TEXAS INSTRUMENTS
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bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
XIN input current (50% duty cycle) . . . . . ±60 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

OTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

ecommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	GCA, GCB, GCC, GCD	2.1		V
Low-level input voltage, V_{IL}			0.6	V
Bias resistor between pins 8 and 16		64	72	kΩ
Operating free-air temperature, T_A		0	40	°C

lectrical characteristics over recommended ranges of supply voltage and operating free-air temperature

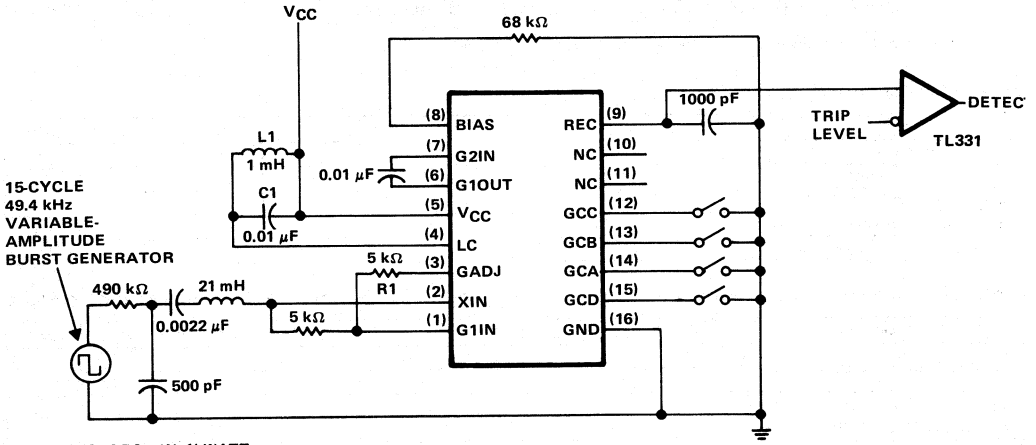
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Input clamp voltage at XIN	I_I = 40 mA				2.5	V
	I_I = −40 mA				−1.5	
Open-circuit input voltage at GCA, GCB, GCC, GCD	V_{CC} = 5 V,	I_I = 0		2.5		V
High-level input current, I_{IH}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IH} = 2 V		−0.5		mA
Low-level input current, I_{IL}, into GCA, GCB, GCC, GCD	V_{CC} = 5 V,	V_{IL} = 0			−3	mA
Receive output current	I_{G2IN} = −100 μA,	V_O = 0.3 V		1		μA
	I_{G2IN} = 100 μA,	V_O = 0.1 V		−50		
Supply current, I_{CC}					45	mA

Typical values are at V_{CC} = 5 V and T_A = 25°C.

TYPICAL APPLICATION INFORMATION

detect level vs gain step

Detect level is measured by applying a 15-cycle burst of 49.4 kilohertz square wave just after the beginning of the gain step to be tested. The least burst amplitude that makes the REC pin reach the trip level is defined to be the detect level. System gain is then inversely proportional to detect level. See the test circuit in Figure 1.



ALL RESISTORS ±1%, ¼ WATT
ALL CAPACITORS ±1%, FILM
L1 Q > 60 at 50 kHz
C1 Q > 500 at 50 kHz

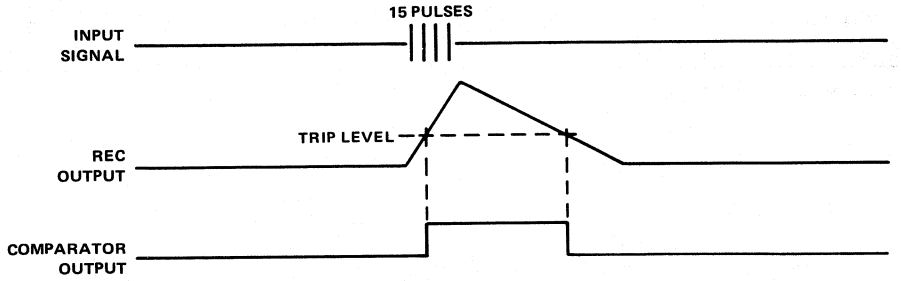


FIGURE 1. DETECT-LEVEL MEASUREMENT CIRCUIT AND WAVEFORMS

TEXAS INSTRUMENTS
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TYPICAL APPLICATION INFORMATION

GAIN STEP TABLE

GCD	GCC	GCB	GCA	STEP NUMBER
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11

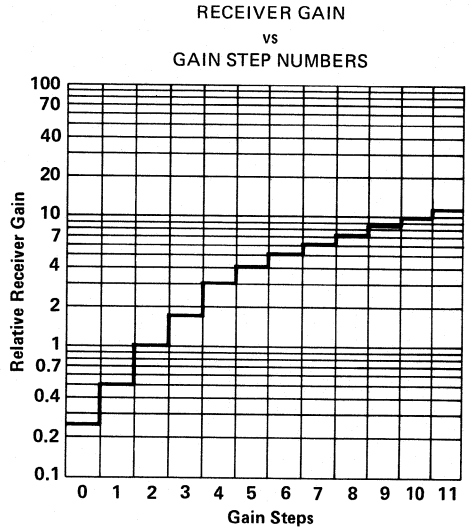
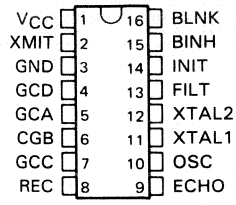


FIGURE 2

D2843, DECEMBER 1984—REVISED MARCH 1988

- **Designed for Use with the TL852 in Sonar Ranging Modules Like the SN28828**
- **Operates with Single Supply**
- **Accurate Clock Output for External Use**
- **Synchronous 4-Bit Gain Control Output**
- **Internal 1.2-V Level Detector for Receive**
- **TTL-Compatible**
- **Interface to 40-kHz Piezoelectric or Electrostatic Transducers**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL853 is an economical digital I^2L ranging control integrated circuit designed for use with the Texas Instruments TL852 Sonar ranging receiver integrated circuit.

The TL853 is designed for distance measurement ranging from six inches to 35 feet. The device has an internal oscillator that uses a low-cost external ceramic resonator. With a simple interface and a 420-kHz ceramic resonator, the device will drive a 40-kHz piezoelectric transducer.

The device cycle begins when Initiate (INIT) is taken to the high logic level. There must be at least 5 ms from initial power up (V_{CC}) to the first initiate signal in order for all the device internal latches to reset and for the ceramic-resonator-controlled oscillator to stabilize. The device will transmit a burst of 16 pulses each time INIT is taken high.

The oscillator output (OSC) is enabled by INIT. The oscillator frequency is the ceramic resonator frequency divided by 10.5 for the first 16 cycles (during transmit) and then the oscillator frequency changes to the ceramic resonator frequency divided by 4.5 for the remainder of the device cycle.

When used with an external 420-kilohertz ceramic resonator, the device internal blanking disables the receive input (REC) for 2.46 ms after initiate to exclude false receive inputs that may be caused by transducer ringing. The internal blanking feature also eliminates echos from objects closer than 1.37 feet from the transducer. If it is necessary to detect objects closer than 1.37 feet, then the internal blanking may be shortened by taking the blanking inhibit (BINH) high, enabling the receive input. The blanking input (BLNK) may be used to disable the receive input and reset ECHO to a low logic level at any time during the device cycle for selective echo exclusion or for a multiple-echo mode of operation.

The device provides a synchronous 4-bit gain control output (12 steps) designed to control the gain of the TL852 sonar ranging receiver integrated circuit. The digital gain control waveforms are shown in Figure 2 with the nominal transition times from INIT listed in the Gain Control Output Table.

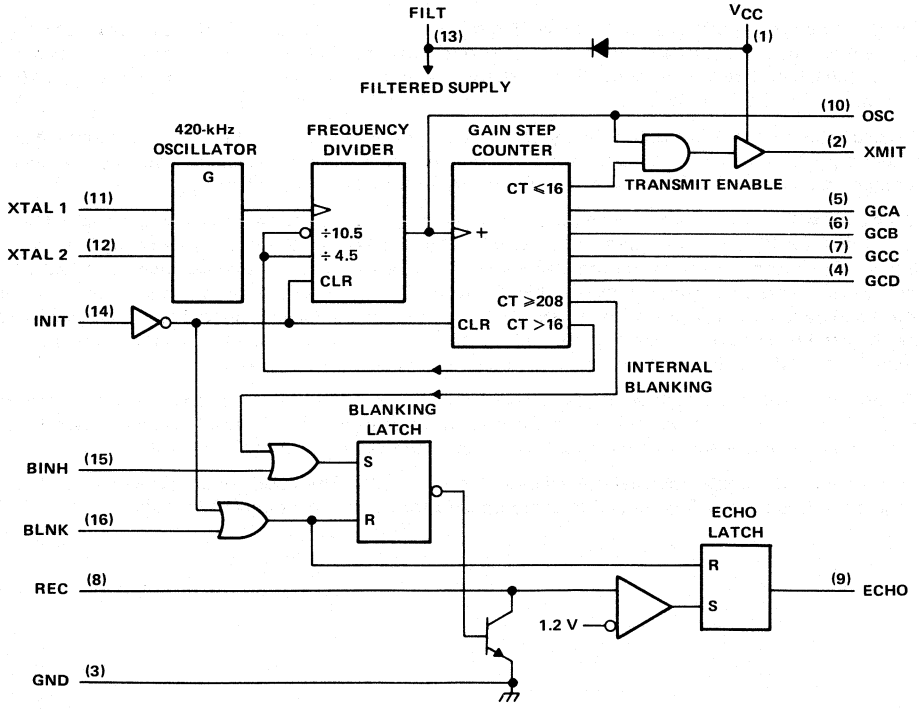
The threshold of the internal receive level detector is 1.2 volts. The TL853 operates over a supply voltage range of 4.5 volts to 6.8 volts and is characterized for operation from 0°C to 40°C.

GAIN CONTROL OUTPUT TABLE

STEP NUMBER	CGD	GCC	GCB	GCA	TIME (ms) FROM INITIATE↑†
0	L	L	L	L	2.46 ms
1	L	L	L	H	5.2 ms
2	L	L	H	L	7.94 ms
3	L	L	H	H	10.69 ms
4	L	H	L	L	13.43 ms
5	L	H	L	H	16.17 ms
6	L	H	H	L	18.91 ms
7	L	H	H	H	21.66 ms
8	H	L	L	L	27.14 ms
9	H	L	L	H	32.63 ms
10	H	L	H	L	38.11 ms
11	H	L	H	H	INIT ↓

†This is the time to the end of the indicated step and assumes a nominal 420-kHz ceramic resonator.

functional block diagram



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Voltage at any pin with respect to GND . . . . . −0.5 V to 7 V
Voltage at any pin with respect to V_{CC} . . . . . −7 V to 0.5 V
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 1) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: For operation above 25°C, derate linearly at the rate of 9.2 mW/°C.

recommended operating conditions

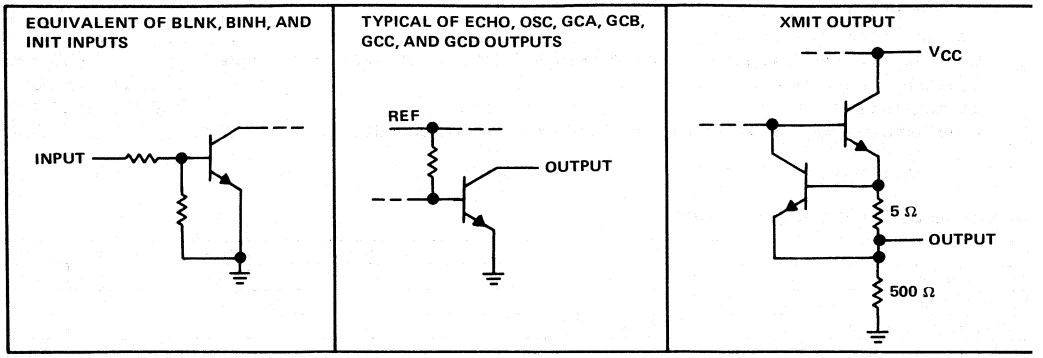
		MIN	MAX	UNIT
Supply voltage, V_{CC}		4.5	6.8	V
High-level input voltage, V_{IH}	BLNK, BINH, INIT	2.1		V
Low-level input voltage, V_{IL}	BLNK, BINH, INIT		0.6	V
Delay time, power up to INIT high		5		ms
Operating free-air temperature, T_A		0	40	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input current		BLNK, BINH, INIT	V_I = 2.1 V			1	mA
High-level output current, I_{OH}		ECHO, OSC, GCA, GCB, GCC, GCD	V_{OH} = 5.5 mA			100	μA
Low-level output voltage, V_{OL}		ECHO, OSC, GCA, GCB, GCC, GCD	I_{OL} = 1.6 mA			0.4	V
On-state output current		XMIT output	V_O = 1 V	−140			mA
Internal blanking interval		REC input			2.46‡		ms
Frequency during 16-pulse transmit period		OSC output			40‡		kHz
		XMIT output			40‡		
Frequency after 16-pulse transmit period		OSC output			93.3‡		kHz
		XMIT output			0		
Supply current, I_{CC}	During transmit period					260	mA
	After transmit period					55	

†Typical values are at V_{CC} = 5 V and T_A = 25°C.
‡These typical values apply for a 420-kHz ceramic resonator.

schematics of inputs and outputs



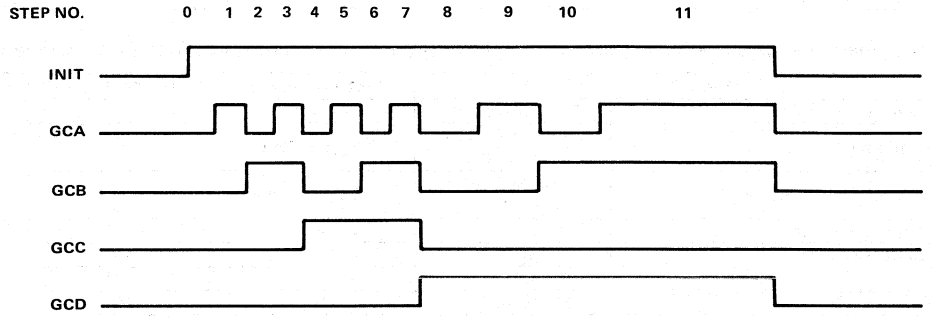


FIGURE 1. DIGITAL GAIN CONTROL WAVEFORMS

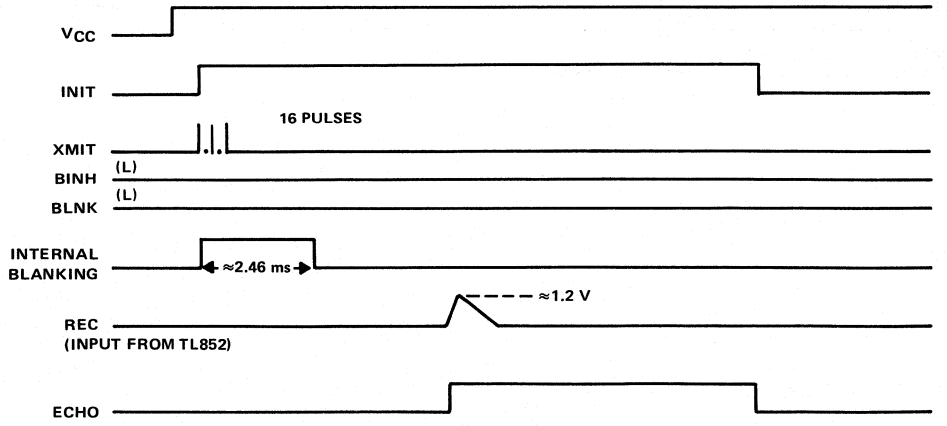


FIGURE 2. EXAMPLE OF SINGLE-ECHO-MODE CYCLE WHEN USED WITH THE TL852 RECEIVER AND 420-kHz CERAMIC RESONATOR

TEXAS INSTRUMENTS
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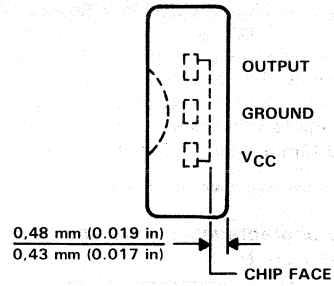
D2903, SEPTEMBER 1985—REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Standard Bipolar Technology Minimizes ESD Susceptibility
- I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V
- I_{OH} . . . 1 μA Max at V_{OH} = 24 V
- Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging
- Direct Replacement for the Sprague UGN3013

LU PACKAGE
(TOP VIEW)



FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 2.5 mT (25 G)	Off
2.5 mT (25 G) < B < 45 mT (450 G)	Undefined
B ≥ 45 mT (450 G)	On

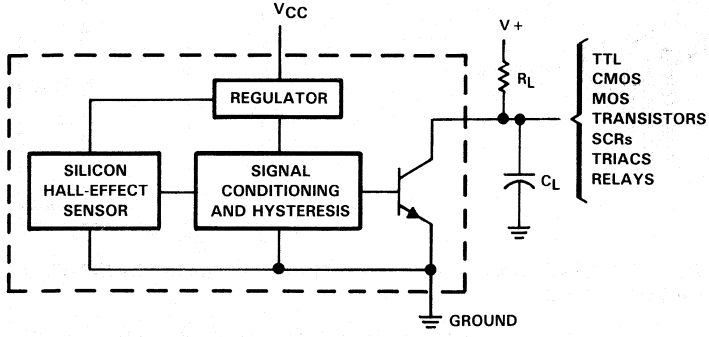
The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

description

The TL3013C is a low-cost magnetically operated electronic switch that utilizes the Hall effect to sense magnetic fields. Each circuit consists of a Hall-effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

The TL3013C is characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			30	45	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		2.5	22.5		mT†
B_{hys}	Hysteresis ($B_{OP} - B_{RP}$)		3	7.5		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

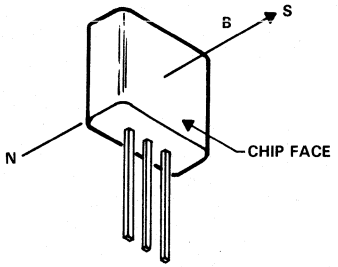


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

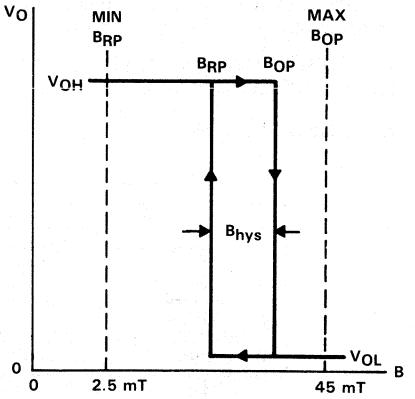


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF		350		ns
t_f	Output fall time			85		

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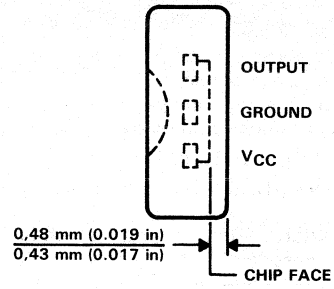
D2903, JULY 1985—REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Standard Bipolar Technology Minimizes ESD Susceptibility
- I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V
- I_{OH} . . . 1 μA Max at V_{OH} = 24 V
- Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging
- Direct Replacement for the Sprague UGN3019

LU PACKAGE
(TOP VIEW)



description

The TL3019C is a low-cost magnetically operated electronic switch that utilizes the Hall Effect to sense magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

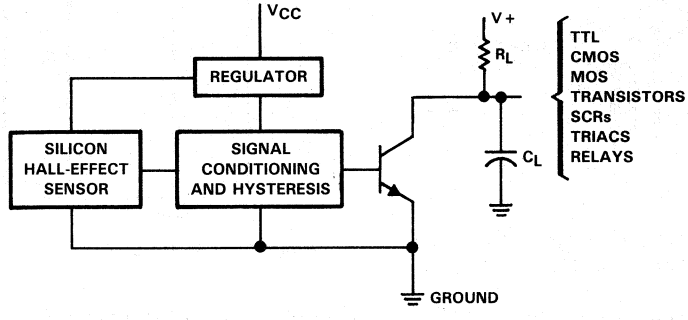
The TL3019C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 12.5 mT (125 G)	Off
12.5 mT (125 G) < B < 50 mT (500 G)	Undefined
B ≥ 50 mT (500 G)	On

The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in millitesla may be converted to gauss (G) by multiplying by ten.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			42	50	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		12.5	30		mT†
B_{hys}	Hysteresis ($B_{OP} - B_{RP}$)		5	12		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

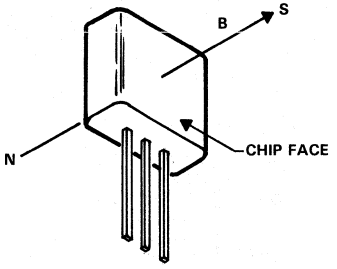


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

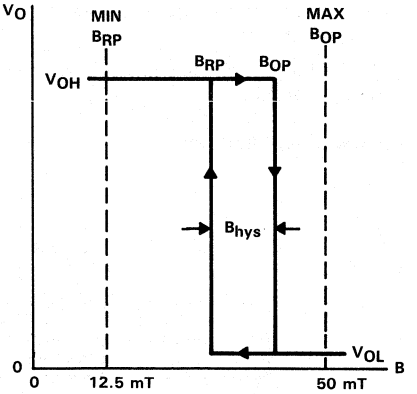


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

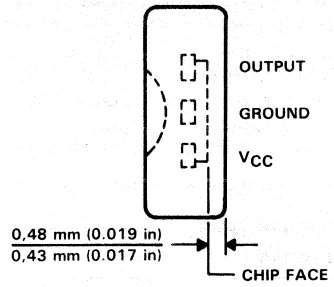
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF		350		ns
t_f	Output fall time			85		

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D2903, OCTOBER 1985—REVISED APRIL 1988

- **Magnetic-Field Sensing Hall-Effect Input**
- **On-Off Hysteresis**
- **Small Size**
- **Standard Bipolar Technology Minimizes ESD Susceptibility**
- **I_{OL} . . . 20 mA Min at V_{OL} = 0.4 V**
- **I_{OH} . . . 1 μA Max at V_{OH} = 24 V**
- **Buried Hall-Effect Cell Reduces Threshold Drift Caused by Temperature Variation and Aging**
- **Direct Replacement for the Sprague UGN3020**

LU PACKAGE
(TOP VIEW)



description

The TL3020C is a low-cost magnetically operated electronic switch that utilizes the Hall effect to sense magnetic fields. Each circuit consists of a Hall-effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

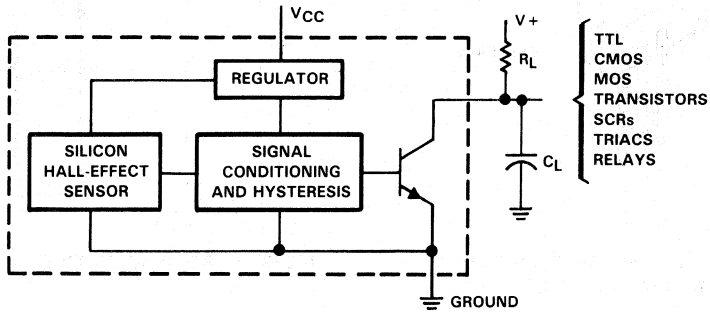
The TL3020C is characterized for operation over the temperature range of 0°C to 70°C.

FUNCTION TABLE (0°C ≤ T_A ≤ 70°C)

FLUX DENSITY	OUTPUT
B ≤ 5 mT (50 G)	Off
5 mT (50 G) < B < 35 mT (350 G)	Undefined
B ≥ 35 mT (350 G)	On

The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

functional block diagram



4 Special Functions

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 40 V
Output voltage . . . . . 40 V
Output current . . . . . 30 mA
Magnetic flux density . . . . . unlimited
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1. Voltage values are with respect to the network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{OP}	Operate-point magnetic flux density (see Figure 2)			22	35	mT†
B_{RP}	Release-point magnetic flux density (see Figure 2)		5	16.5		mT†
B_{hys}	Hysteresis ($B_{OP} - B_{RP}$)		2	5.5		mT†
α_B	Temperature coefficient of B_{OP} and B_{RP}			±0.25		%/°C
V_{OL}	Low-level output voltage	I_{OL} = 20 mA			0.4	V
I_{OH}	High-level output current	V_{OH} = 24 V			1	μA
I_{CC}	Supply current			3	7	mA

†The unit of magnetic density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss (G) by multiplying by ten.

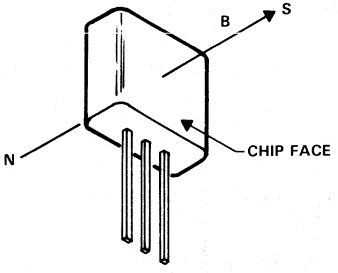


FIGURE 1. DEVICE ORIENTATION IN A MAGNETIC FIELD

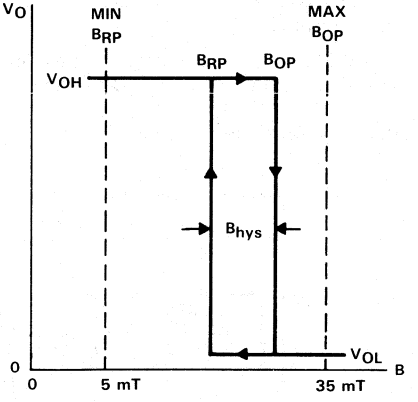


FIGURE 2. REPRESENTATIVE CURVE OF V_O vs B

switching characteristics at V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

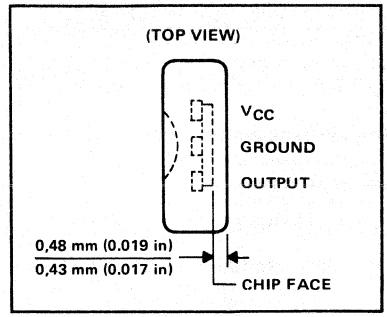
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	R_L = 820 Ω, C_L = 20 pF		350		ns
t_f	Output fall time			85		

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

APRIL 1985—REVISED APRIL 1988

- Magnetic-Field Sensing Hall-Effect Input
- On-Off Hysteresis
- Small Size
- Solid-State Technology
- Open-Collector Output
- Buried Hall-Effect Cell Reduces Threshold Drift Caused By Temperature Variation and Aging

LU PACKAGE



description

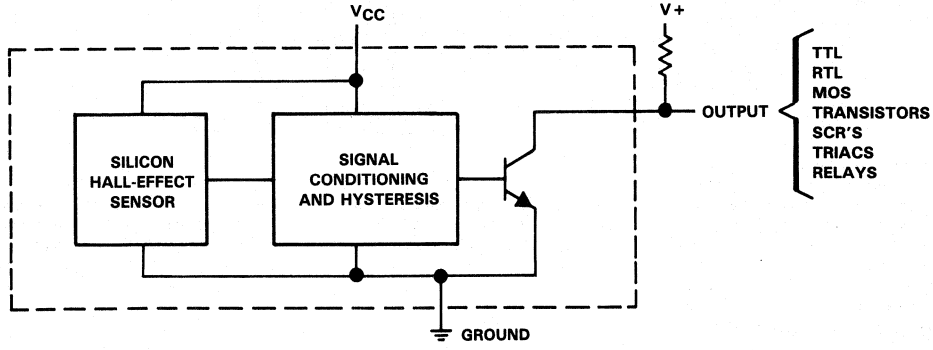
The TL3101I and TL3101C are low-cost magnetically operated electronic switches that utilize the Hall Effect to sense steady-state magnetic fields. Each circuit consists of a Hall-Effect sensor, signal conditioning and hysteresis functions, and an output transistor integrated into a monolithic chip. The outputs of these circuits can be directly connected to many different types of electronic components.

The TL3101C is characterized for operation over the temperature range of 0°C to 70°C. The TL3101I is characterized for operation over the range of −20°C to 85°C.

FUNCTION TABLE 0°C ≥ T_A ≤ 70°C

FLUX DENSITY	OUTPUT
≤ −25 mT	Off
−25 mT < B < 25 mT	Undefined
≥ 25 mT	On

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

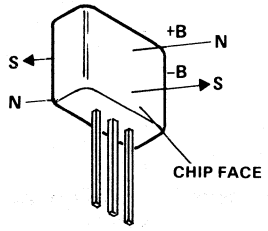
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Output voltage . . . . . 30 V
Output current . . . . . 20 mA
Operating free-air temperature range: TL3101C . . . . . 0°C to 70°C
TL3101I . . . . . −20°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Magnetic flux density . . . . . unlimited

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{CC} = 5 V ± 5% (unless otherwise noted)

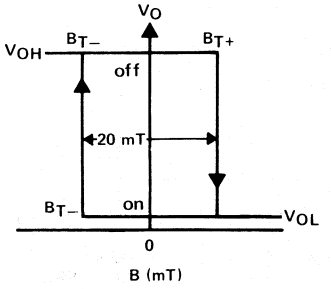
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
B_{T+}	Threshold of positive going magnetic flux density†			0°C to 70°C	0		25	mT§
				−20°C to 85°C	0		35	
B_{T-}	Threshold of negative going magnetic flux density†			0°C to 70°C	−25‡		0	mT§
				−20°C to 85°C	−35‡		0	
$B_{T+} - B_{T-}$	Hysteresis			0°C to 70°C	5	20		mT‡
I_{OH}	High-level output current	V_{OH} = 20 V		0°C to 70°C			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75, I_{OL} = 16 mA		0°C to 70°C			0.4	V
I_{CC}	Supply current	V_{CC} = 5.25 V	Output low	0°C to 70°C			6	mA
			Output high				4	

†Threshold values are those levels of magnetic flux density at which the output changes state. For the TL3101, a level more positive than B_{T+} causes the output to a low level and a level more negative than B_{T-} causes the output to go to a high level. See Figures 1 and 2.
‡The algebraic convention, where the most negative limit is designated as minimum, is used in this data sheet for flux density threshold levels only.
§The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY



The positive-going threshold (B_{T+}) is a positive B level at which a positive-going flux density results in the TL3101 output turning on. The negative-going threshold is negative B level at which a negative-going flux density results in the TL3101 turning off.

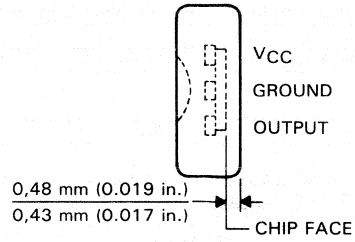
FIGURE 2. REPRESENTATIVE CURVES OF V_O vs B

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

D3184, MAY 1985—REVISED FEBRUARY 1989

- **Output Voltage Linear with Applied Magnetic Field**
- **Sensitivity Stable Over Wide Operating Temperature Range**
- **Buried Hall Cell Reduces Changes Due to Temperature Variation and Aging**
- **Solid-State Technology**
- **Three-Terminal Device**
- **Senses Static or Dynamic Magnetic Fields**

LU PACKAGE
(TOP VIEW)

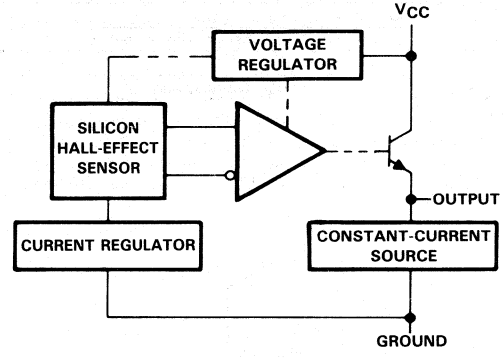


description

The TL3103I and TL3103C are low-cost magnetic-field sensors designed to provide a linear output voltage proportional to the magnetic field they sense. These monolithic circuits incorporate a Hall element as the primary sensor along with a voltage reference and a precision amplifier. Temperature stabilization and internal trimming circuitry yield a device that features high overall sensitivity accuracy with less then 5% error over its operating temperature range.

The TL3103I is characterized for operation from −20°C to 85°C. The TL3103C is characterized for operation from 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	775 mW
Operating free-air temperature range: TL3103I	−20°C to 85°C
TL3103C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Magnetic flux density	unlimited

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 6.2 mW/°C.

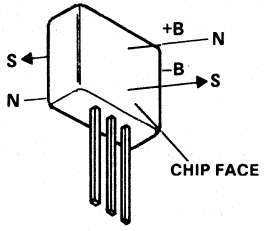
recommended operating conditions

		TL3103I			TL3103C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		9	12	15	9	12	15	V
Magnetic flux density, B				±50			±50	mT
Output current, I_O	Sink			0.5			0.5	mA
	Source			−2			−2	
Operating free-air temperature, T_A		−20		85	0		70	°C

electrical characteristics over recommended ranges of supply voltage and magnetic flux density, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_O	Output voltage	I_O = −2 mA to 0.5 mA, B = 0 mT§	5.8	6	6.2	V
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)			18		mV/V
S	Magnetic sensitivity ($\Delta V_O/\Delta B$)	B = −50 to 50 mT§	14	16	18	V/T§
ΔS	Magnetic sensitivity change with temperature	ΔT_A = 25°C to MIN or MAX			±5	%
I_{CC}	Supply current	B = 0 mT§, I_O = 0		8	12	mA
f_{max}	Maximum operating frequency			100		kHz

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Typical values are at V_{CC} = 12 V at T_A = 25°C.
§The unit of magnetic flux density in the International System of Units (SI) is the tesla (T). The tesla is equal to one weber per square meter. Values expressed in milliteslas may be converted to gauss by multiplying by ten, e.g., 50 millitesla = 500 gauss.



The north pole of a magnet is the pole that is attracted by the geographical north pole. The north pole of a magnet repels the north-seeking pole of a compass. By accepted magnetic convention, lines of flux emanate from the north pole of a magnet and enter the south pole.

FIGURE 1. DEFINITION OF MAGNETIC FLUX POLARITY

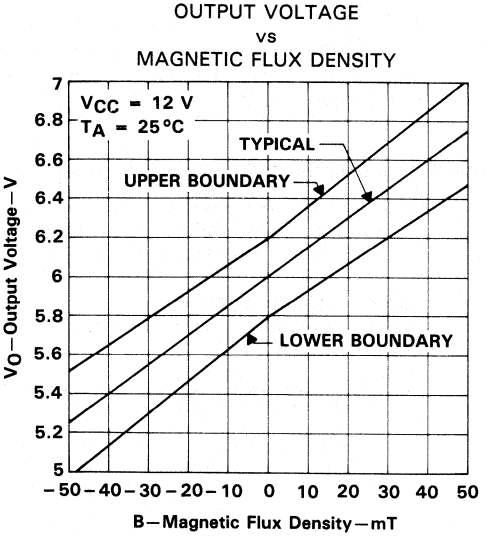


FIGURE 2

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA

The circuit in Figure 3 may be used to set the output voltage at zero field strength to exactly 6 V (using R1) and to set the sensitivity to exactly −15 V/T (using R2) as depicted in Figure 4.

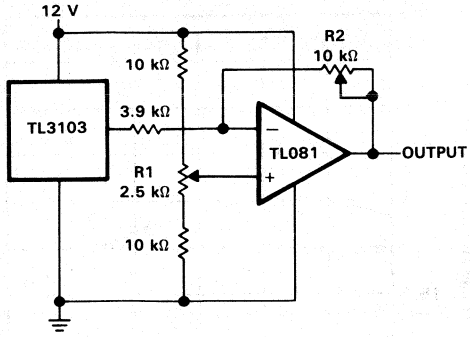


FIGURE 3. COMPENSATION CIRCUIT

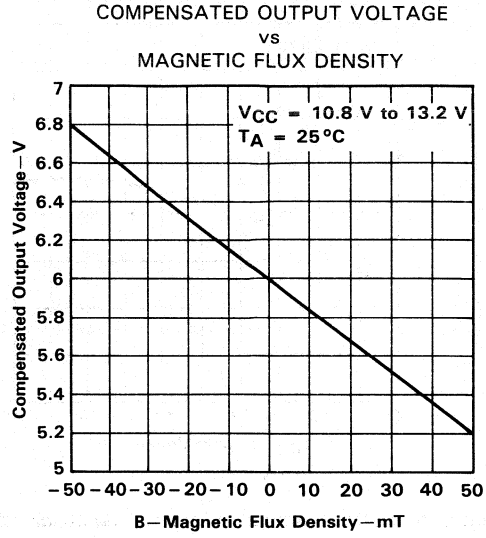


FIGURE 4

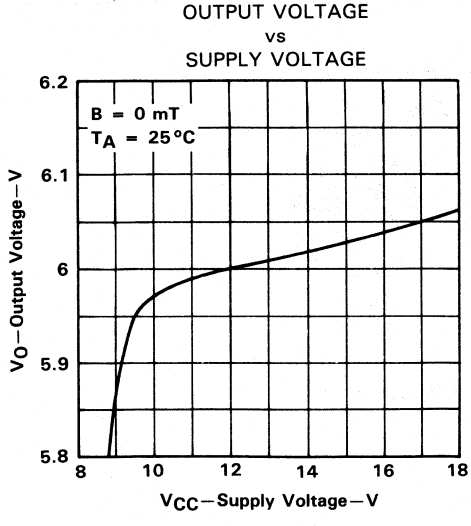


FIGURE 5

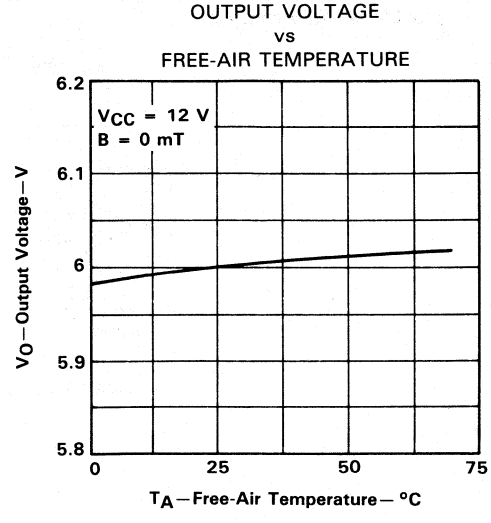


FIGURE 6

TYPICAL APPLICATION DATA

MAGNETIC SENSITIVITY
vs
SUPPLY VOLTAGE

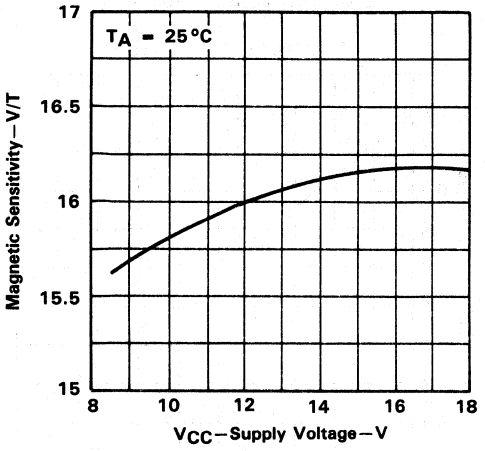


FIGURE 7

MAGNETIC SENSITIVITY
vs
FREE-AIR TEMPERATURE

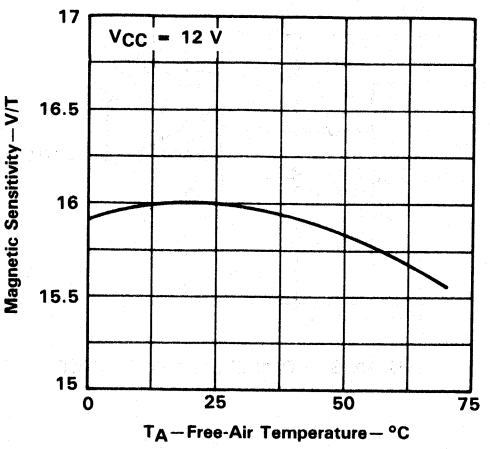


FIGURE 8

linear hall-effect sensor in isolated feedback applications

purpose

The purpose of the circuit in Figure 9 is to demonstrate the capability of the linear hall-effect sensor to provide isolated sensing.

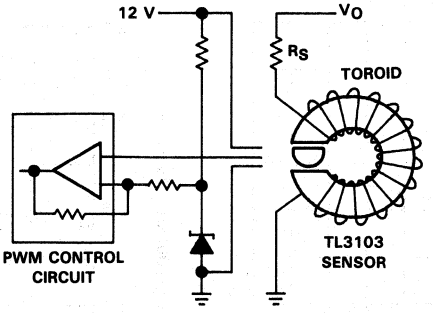


FIGURE 9. ISOLATE FEEDBACK

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

linear sensor

The TL3103 senses the presence of a magnetic field. In the absence of a magnetic field, the TL3103 output voltage is 6 V. As the sensor senses the presence of a magnetic field, its output varies proportionally at 16 V/T.

toroid

The permeability (μ) of any given material is the relationship of the magnetic flux density (B) to the magnetic field intensity (H). The magnetic field intensity of a toroid is given by the expression:

$$H = \frac{NI}{L} \tag{1}$$

Where: NI is number of turns times the current.
L is mean length of the toroid.

The expression for the magnetic flux density then becomes:

$$B = \mu \frac{NI}{L} \tag{2}$$

With an air gap, the basic expression is altered to the following:

$$B_{gap} = \mu_o \frac{NI}{L + Kg} K \tag{3}$$

Where: μ_o is the permeability of air $= 12.57 \times 10^{-7}$.
K is the relative permeability of the toroid (μ/μ_o).
g is the length of the air gap in mils.

If the relative permeability of the toroid is large (Kg > K), the mean length of the toroid becomes insignificant and the expression for flux density reduces to:

$$B_{gap} = \mu_o \frac{NI}{g} \tag{4}$$

circuit

As previously discussed, the output of the TL3103 is:

$$V_{sense} = 6\ V + (16\ V/T)\ (\mu_o \frac{NI}{g}) \tag{5}$$

This shows how the output of the TL3103 varies with the ampere turns of the toroid. For some relative numbers, Figure 9 uses an Arnold toroid #A393163-2 with a 156-mil air gap. The magnetic field created in the air gap is:

$$B\ (gauss) = 1.92\ NI\ (ampere\ turns) \tag{6}$$

Therefore, the variation in the output of the TL3103 is:

$$\Delta V_{sense}\ (mV) = (1.6)\ (1.92NI) \tag{7}$$

The sensitivity of the TL3103 to the current in the windings can therefore be altered by the number of turns composing the windings.

ΔV_{sense}	N	ΔI
614 mV	20	10 mA
614 mV	200	1 mA
614 mV	2000	100 μA

power supply application

Since the output of the TL3103 varies proportionally to the current flow in the toroid, this leads to the obvious application of current sensing. The features presented by this approach are as follows:

1. Minimum power loss in the sensing element:

$$P_{loss} = I^2R_{toroid} \quad (R < 0.01\ \Omega \text{ for 20 turns}) \tag{8}$$

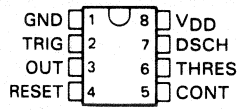
2. Isolated feedback, no passive connection required.

Another application of this concept provides a linear isolated feedback of the output voltage. This is accomplished by connecting a resistor in series with the toroid terminated to ground. In this configuration, the current in the toroid is determined by the output voltage ($I_S = V_O/R_S$), therefore, the output variation of the TL3103 is proportional to the output voltage.

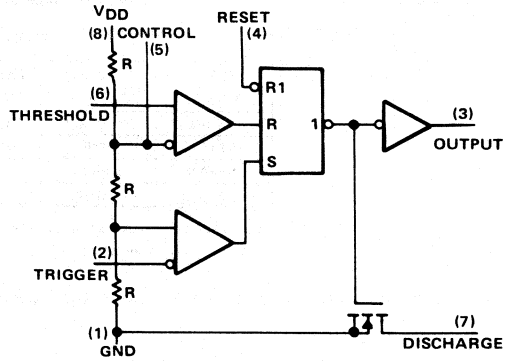
D2791, FEBRUARY 1984—REVISED MAY 1988

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 1 V to 18 V**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

D OR P PACKAGE
(TOP VIEW)



functional block diagram



Reset can override Trigger, which can override Threshold.

description

The TLC551 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE555, the TLC551 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC551 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC551C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	V_T MAX AT 25°C	PACKAGE	
		SMALL-OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	3.8 V	TLC551CD	TLC551CP

D package is available taped-and-reeled. Add "R" suffix to device type when ordering (i.e. TLC551CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation at (or below) 25°C free-air temperature . . . . . 460 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		0.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		15	100	μA
		Full range			150	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		65	250	μA
		Full range			400	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		170	350	μA
		Full range			500	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		360	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		420	600	μA
		Full range			800	

†Full range (MIN to MAX) is 0°C to 70°C.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V, $R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 2		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 2	1.2	1.8		MHz

‡Timing interval error is defined as the difference between the measured value and the nominal value of a random sample.
NOTE 2: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA

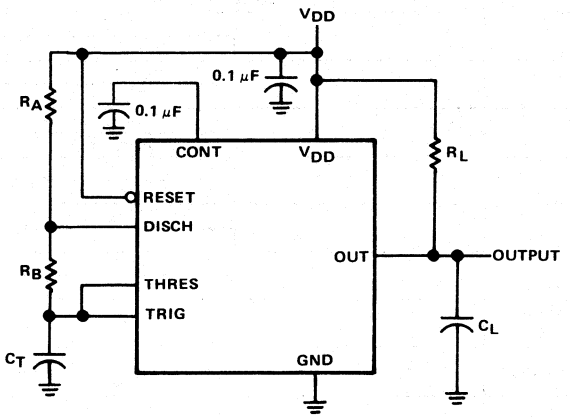
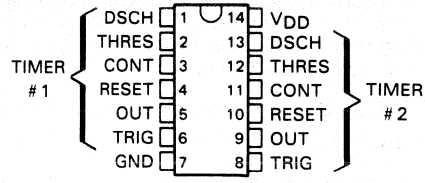


FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

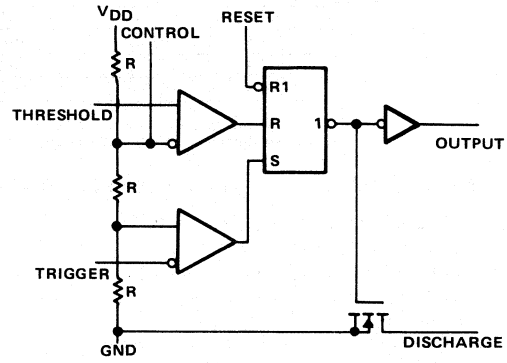
D2796, FEBRUARY 1984—REVISED MAY 1988

- Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High Output-Current Capability
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- Output Fully Compatible with CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During Output Transitions
- High-Impedance Inputs . . . 10^{12} Ω Typ
- Single-Supply Operation from 1 V to 18 V
- Functionally Interchangeable with the NE556; Has Same Pinout

D OR N PACKAGE
(TOP VIEW)



functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

description

The TLC552 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC552 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 milliamperes and sourcing over 10 milliamperes, the TLC552 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
TLC552C	D,N	0°C to 70°C	3.8 mV

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e. TLC552CDR)

LinCMOS is a trademark of Texas Instruments.

description (continued)

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 volts as tested under MIL-STD-883C, Method 3015.2. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC552C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Input voltage range (any input) . . . . . −0.3 V to V_{DD}
Sink current, discharge or output . . . . . 150 mA
Source current, output . . . . . 15 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
D	950 mW	7.6 mW/°C	25°C
N	1150 mW	9.2 mW/°C	25°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1	18	V
Operating free-air temperature, T_A	0	70	°C

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lectrical characteristics at specified free-air temperature, V_{DD} = 1 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.475	0.67	0.85	V
		Full range	0.45		0.875	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.15	0.33	0.425	V
		Full range	0.1		1.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	0.7	1	V
		Full range	0.3		1	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 μA	25°C		0.02	0.15	V
		Full range			0.2	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 μA	25°C		0.03	0.2	V
		Full range			0.25	
High-level output voltage	I_{OH} = −10 μA	25°C	0.6	0.98		V
		Full range	0.6			
Supply current		25°C		30	200	μA
		Full range			300	

Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 2 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	0.95	1.33	1.65	V
		Full range	0.85		1.75	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	0.4	0.67	0.95	V
		Full range	0.3		1.05	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2	V
		Full range			0.25	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		V
		Full range	1.5			
Supply current		25°C		130	500	μA
		Full range			800	

† Full range (MIN to MAX) is 0°C to 70°C.

lectrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	2.8	3.3	3.8	V
		Full range	2.7		3.9	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	1.36	1.66	1.96	V
		Full range	1.26		2.06	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5	V
		Full range			0.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4	V
		Full range			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3	
		Full range			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3	
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		V
		Full range	4.1			
Supply current		25°C		340	700	μA
		Full range			1000	

† Full range (MIN to MAX) is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	9.45	10	10.55	V
		Full range	9.35		10.65	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	4.65	5	5.35	V
		Full range	4.55		5.45	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7	V
		Full range			1.8	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2	V
		Full range			3.6	
	I_{OL} = 50 mA	25°C		0.63	1	
		Full range			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3	
		Full range			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		V
		Full range	12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		
		Full range	13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		
		Full range	14.2			
Supply current		25°C		0.72	1.2	mA
		Full range			1.6	

† Full range (MIN to MAX) is 0°C to 70°C.

ectrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Threshold voltage level		25°C	11.4	12	12.6	V
		Full range	10.9		12.7	
Threshold current		25°C		10		pA
		MAX		75		
Trigger voltage level		25°C	5.6	6	6.4	V
		Full range	5.5		6.5	
Trigger current		25°C		10		pA
		MAX		75		
Reset voltage level		25°C	0.4	1.1	1.5	V
		Full range	0.3		1.8	
Reset current		25°C		10		pA
		MAX		75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5	V
		Full range			1.6	
Discharge switch off-state current		25°C		0.1		nA
		MAX		0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3	V
		Full range			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		V
		Full range	17.3			
Supply current		25°C		0.84	1.2	mA
		Full range			1.6	

Full range (MIN to MAX) is 0°C to 70°C.

perating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,			1%	3%	
Supply voltage sensitivity of timing interval	$R_A = R_B$ = 1 kΩ to 100 kΩ, C_T = 0.1 μF,	See Note 2		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ,	C_L = 10 pF		20	75	ns
Output pulse fall time				15	60	
Maximum frequency in astable mode	R_A = 470 Ω, C_T = 200 pF,	R_B = 200 Ω, See Note 2	1.2	2.8		MHz

OTE 2: R_A, R_B, and C_T are as defined in Figure 1.
Timing interval error is defined as the difference between the measured value and the nominal value of a random sample.

TYPICAL APPLICATION DATA

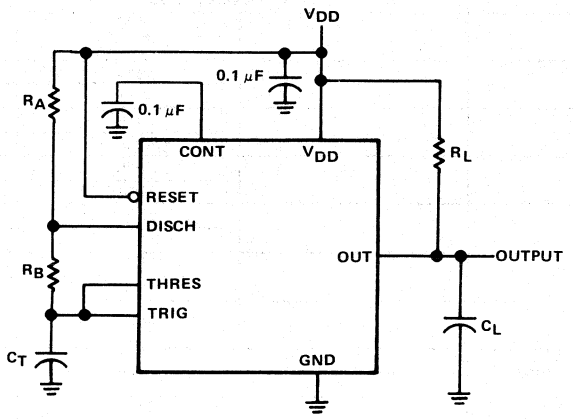


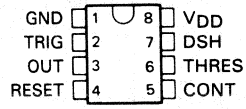
FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

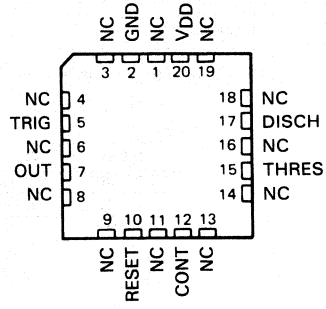
D2784, SEPTEMBER 1983—REVISED OCTOBER 1988

- **Very Low Power Consumption . . . 1 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE555; Has Same Pinout**

TLC555M . . . JG PACKAGE
TLC555I, TLC555C . . . D OR P PACKAGE
(TOP VIEW)



TLC555M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

lescription

The TLC555 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE555 because of the high input impedance. Power consumption is low across the full range of power supply voltage.

Like the NE555, the TLC555 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC555 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE555.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC555M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC555I is characterized for operation from −40°C to 85°C. The TLC555C is characterized for operation from 0°C to 70°C.

4 Special Functions

LinCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A RANGE	V_{CC} RANGE	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	2 V to 18 V	TLC555CD			TLC555CP
−40°C to 85°C	3 V to 18 V	TLC555ID			TLC555IP
−55°C to 125°C	5 V to 18 V		TLC555MFK	TLC555MJG	

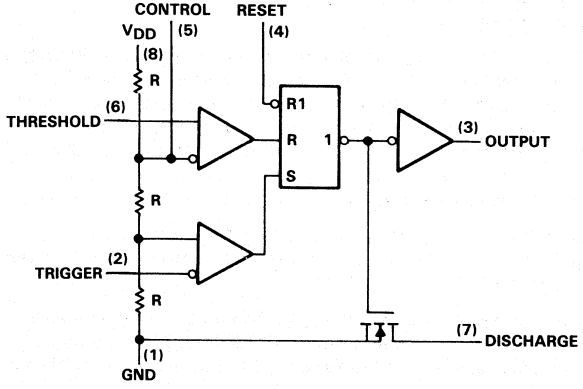
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC555CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram



Pin numbers are for all packages except FK.
Reset can override Trigger, which can override Threshold.

TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC555M	TLC555I	TLC555C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		-0.3 to V_{DD}	-0.3 to V_{DD}	-0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		-55 to 125	-40 to 85	0 to 70	°C
Storage temperature range		-65 to 150	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300			
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	260	

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A

electrical characteristics at specified free-air temperature, V_{DD} = 3 V for TLC555I, V_{DD} = 2 V for TLC555C

PARAMETER	TEST CONDITIONS†		TLC555I			TLC555C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	1.6		2.4	0.95	1.33	1.65	V
		Full range	1.5		2.5	0.85		1.75	
Threshold current		25°C		10			10		pA
		MAX		150			75		
Trigger voltage level		25°C	0.71	1.0	1.29	0.4	0.67	0.95	V
		Full range	0.61		1.39	0.3		1.05	
Trigger current		25°C		10			10		pA
		MAX		150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		2	
Reset current		25°C		10			10		pA
		MAX		150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2		0.03	0.2	V
		Full range			0.375			0.25	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		1.5	1.9		V
		Full range	2.5			1.5			
Supply current		25°C			250			250	μA
		Full range			500			400	

†Full range (MIN to MAX) is −40°C to 85°C for TLC555I and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
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Electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.14	0.5		0.14	0.5		0.14	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			120			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 2	25°C		170	350		170	350		170	350	μA
		Full range			700			600			500	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.77	1.7		0.77	1.7		0.77	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			120			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current	See Note 2	25°C		360	600		360	600		360	600	μA
		Full range			1000			900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

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Electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.72	1.5		0.72	1.5		0.72	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			120			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 2	25°C			600			600			600	μA
		Full range			1000			900			800	

†Full range (MIN to MAX) is −55°C to 125°C for TLC555M, −40°C to 85°C for TLC555I, and 0°C to 70°C for TLC555C.

NOTE 2: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

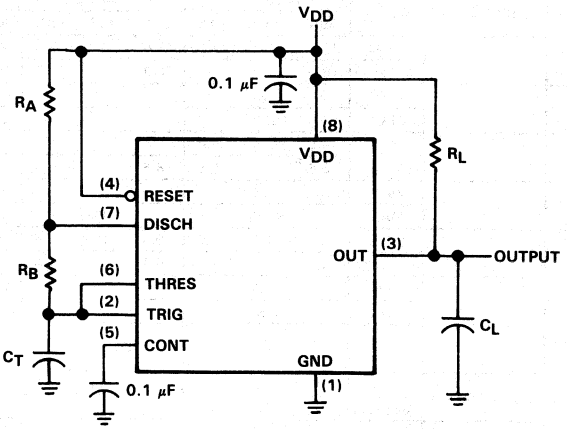
Operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval‡	V_{DD} = 5 V to 15 V,		1%	3%	
Supply voltage sensitivity of timing interval	R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

‡Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 1.

TYPICAL APPLICATION DATA



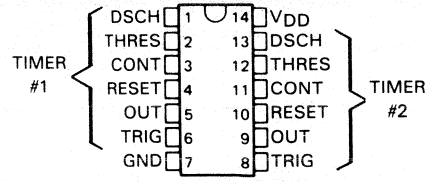
Pin numbers are for all packages except FK.

FIGURE 1. CIRCUIT FOR ASTABLE OPERATION

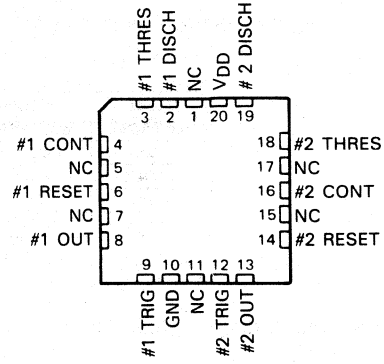
D2796, FEBRUARY 1984—REVISED OCTOBER 1988

- **Very Low Power Consumption . . . 2 mW Typ at V_{DD} = 5 V**
- **Capable of Operation in Astable Mode**
- **CMOS Output Capable of Swinging Rail to Rail**
- **High Output-Current Capability**
  . . . Sink 100 mA Typ
  . . . Source 10 mA Typ
- **Output Fully Compatible with CMOS, TTL, and MOS**
- **Low Supply Current Reduces Spikes During Output Transitions**
- **High-Impedance Inputs . . . 10^{12} Ω Typ**
- **Single-Supply Operation from 2 V to 18 V**
- **Functionally Interchangeable with the NE556; Has Same Pinout**

TLC556M . . . J PACKAGE
TLC556I, TLC556C . . . D OR N PACKAGE
(TOP VIEW)



TLC0556M . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The TLC556 is a monolithic timing circuit fabricated using TI's LinCMOS™ process, which provides full compatibility with CMOS, TTL, and MOS logic and operation at frequencies up to 2 MHz. Accurate time delays and oscillations are possible with smaller, less-expensive timing capacitors than the NE556 because of the high input impedance. Power consumption is low across the full range of power supply voltages.

Like the NE556, the TLC556 has a trigger level approximately one-third of the supply voltage and a threshold level approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset input can override all other inputs and can be used to initiate a new timing cycle. If the reset input is low, the flip-flop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal and ground.

While the CMOS output is capable of sinking over 100 mA and sourcing over 10 mA, the TLC556 exhibits greatly reduced supply-current spikes during output transitions. This minimizes the need for the large decoupling capacitors required by the NE556.

These devices have internal electrostatic discharge (ESD) protection circuits that will prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015. However, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

All unused inputs should be tied to an appropriate logic level to prevent false triggering.

The TLC556M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC556I is characterized for operation from −40°C to 85°C. The TLC556C is characterized for operation from 0°C to 70°C.

LinCMOS is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A RANGE	V_{CC} RANGE	PACKAGE			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)
0°C to 70°C	2 V to 18 V	TLC556CD			TLC556CN
−40°C to 85°C	3 V to 18 V	TLC556ID			TLC556IN
−55°C to 125°C	5 V to 18 V		TLC556MFK	TLC556MJ	

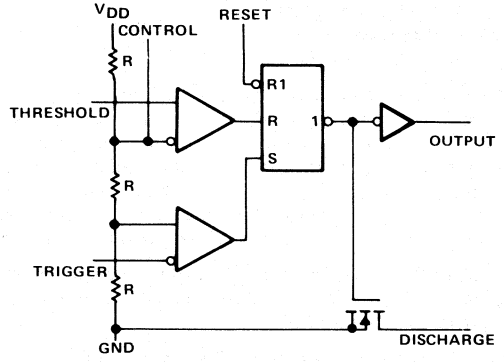
The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC556CDR).

FUNCTION TABLE

RESET VOLTAGE†	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
<MIN	Irrelevant	Irrelevant	Low	On
>MAX	<MIN	Irrelevant	High	Off
>MAX	>MAX	>MAX	Low	On
>MAX	>MAX	<MIN	As previously established	

†For conditions shown as MIN or MAX, use the appropriate value specified under electrical characteristics.

functional block diagram (each timer)



Reset can override Trigger and Threshold.
Trigger can override Threshold.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TLC556M	TLC556I	TLC556C	UNIT
Supply voltage (see Note 1)		18	18	18	V
Input voltage		−0.3 to V_{DD}	−0.3 to V_{DD}	−0.3 to V_{DD}	V
Sink current, discharge or output		150	150	150	mA
Source current, output		15	15	15	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range		−55 to 125	−40 to 85	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package	260			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J package	300			
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	260	

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW	N/A
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	N/A

electrical characteristics at specified free-air temperature, V_{DD} = 3 V for TLC556I, V_{DD} = 2 V for TLC556C

PARAMETER	TEST CONDITIONS†		TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	1.6	2.0	2.4	0.95	1.33	1.65	V
		Full range	1.5		2.5	0.85		1.75	
Threshold current		25°C		10			10		pA
		MAX		150			75		
Trigger voltage level		25°C	0.71	1.0	1.29	0.4	0.67	0.95	V
		Full range	0.61		1.39	0.3		1.05	
Trigger current		25°C		10			10		pA
		MAX		150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10		pA
		MAX		150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 1 mA	25°C		0.03	0.2		0.04	0.2	V
		Full range			0.375			0.25	
Discharge switch off-state current		25°C		0.1			0.1		nA
		MAX		120			0.5		
Low-level output voltage	I_{OL} = 1 mA	25°C		0.07	0.3		0.07	0.3	V
		Full range			0.4			0.35	
High-level output voltage	I_{OH} = −300 μA	25°C	1.5	1.9		1.5	1.9		V
		Full range	2.5			1.5			
Supply current		25°C		130	500		130	500	μA
		Full range			1000			800	

†Full range (MIN to MAX) is −40°C to 85°C for TLC556I and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	2.8	3.3	3.8	2.8	3.3	3.8	2.8	3.3	3.8	V
		Full range	2.7		3.9	2.7		3.9	2.7		3.9	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	1.36	1.66	1.96	1.36	1.66	1.96	1.36	1.66	1.96	V
		Full range	1.26		2.06	1.26		2.06	1.26		2.06	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 10 mA	25°C		0.15	0.5		0.15	0.5		0.15	0.5	V
		Full range			0.6			0.6			0.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 8 mA	25°C		0.21	0.4		0.21	0.4		0.21	0.4	V
		Full range			0.6			0.5			0.5	
	I_{OL} = 5 mA	25°C		0.13	0.3		0.13	0.3		0.13	0.3	
		Full range			0.45			0.4			0.4	
	I_{OL} = 3.2 mA	25°C		0.08	0.3		0.08	0.3		0.08	0.3	
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	4.1	4.8		4.1	4.8		4.1	4.8		V
		Full range	4.1			4.1			4.1			
Supply current	See Note 2	25°C		340	700		340	700		340	700	μA
		Full range			1400			1200			1000	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

electrical characteristics at specified free-air temperature, V_{DD} = 15 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	9.45	10	10.55	9.45	10	10.55	9.45	10	10.55	V
		Full range	9.35		10.65	9.35		10.65	9.35		10.65	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	4.65	5	5.35	4.65	5	5.35	4.65	5	5.35	V
		Full range	4.55		5.45	4.55		5.45	4.55		5.45	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.8	1.7		0.8	1.7		0.8	1.7	V
		Full range			1.8			1.8			1.8	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 100 mA	25°C		1.28	3.2		1.28	3.2		1.28	3.2	V
		Full range			3.8			3.7			3.6	
	I_{OL} = 50 mA	25°C		0.63	1		0.63	1		0.63	1	
		Full range			1.5			1.4			1.3	
	I_{OL} = 10 mA	25°C		0.12	0.3		0.12	0.3		0.12	0.3	
		Full range			0.45			0.4			0.4	
High-level output voltage	I_{OH} = −10 mA	25°C	12.5	14.2		12.5	14.2		12.5	14.2		V
		Full range	12.5			12.5			12.5			
	I_{OH} = −5 mA	25°C	13.5	14.6		13.5	14.6		13.5	14.6		
		Full range	13.5			13.5			13.5			
	I_{OH} = −1 mA	25°C	14.2	14.9		14.2	14.9		14.2	14.9		
		Full range	14.2			14.2			14.2			
Supply current	See Note 2	25°C		0.72	1.2		0.72	1.2		0.72	1.2	mA
		Full range			2			1.8			1.6	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configurations in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 18 V

PARAMETER	TEST CONDITIONS†		TLC556M			TLC556I			TLC556C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level		25°C	11.4	12	12.6	11.4	12	12.6	11.4	12	12.6	V
		Full range	10.9		12.7	10.9		12.7	10.9		12.7	
Threshold current		25°C		10			10			10		pA
		MAX		5000			150			75		
Trigger voltage level		25°C	5.6	6	6.4	5.6	6	6.4	5.6	6	6.4	V
		Full range	5.5		6.5	5.5		6.5	5.5		6.5	
Trigger current		25°C		10			10			10		pA
		MAX		5000			150			75		
Reset voltage level		25°C	0.4	1.1	1.5	0.4	1.1	1.5	0.4	1.1	1.5	V
		Full range	0.3		1.8	0.3		1.8	0.3		1.8	
Reset current		25°C		10			10			10		pA
		MAX		5000			150			75		
Control voltage (open-circuit) as a percentage of supply voltage		MAX		66.7%			66.7%			66.7%		
Discharge switch on-state voltage	I_{OL} = 100 mA	25°C		0.73	1.5		0.73	1.5		0.73	1.5	V
		Full range			1.6			1.6			1.6	
Discharge switch off-state current		25°C		0.1			0.1			0.1		nA
		MAX		120			2			0.5		
Low-level output voltage	I_{OL} = 3.2 mA	25°C		0.04	0.3		0.04	0.3		0.04	0.3	V
		Full range			0.4			0.35			0.35	
High-level output voltage	I_{OH} = −1 mA	25°C	17.3	17.9		17.3	17.9		17.3	17.9		V
		Full range	17.3			17.3			17.3			
Supply current	See Note 2	25°C			1.2			1.2			1.2	mA
		Full range			2			1.8			1.6	

†Full range (MIN to MAX) is −55°C to 125°C for TLC556M, −40°C to 85°C for TLC556I, and 0°C to 70°C for TLC556C.

NOTE 2: These values apply for the expected operating configuration in which the Threshold terminal is connected directly to the Discharge terminal or to the Trigger terminal.

operating characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Initial error of timing interval†	V_{DD} = 5 V to 15 V, R_A = R_B = 1 kΩ to 100 kΩ, C_T = 0.1 μF, See Note 3		1%	3%	
Supply voltage sensitivity of timing interval			0.1	0.5	%/V
Output pulse rise time	R_L = 10 MΩ, C_L = 10 pF		20	75	ns
Output pulse fall time			15	60	
Maximum frequency in astable mode	R_A = 470 Ω, R_B = 200 Ω, C_T = 200 pF, See Note 3	1.2	2.1		MHz

†Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

NOTE 3: R_A, R_B, and C_T are as defined in Figure 3.

TYPICAL CHARACTERISTICS

DISCHARGE SWITCH ON-STATE RESISTANCE
vs
FREE-AIR TEMPERATURE

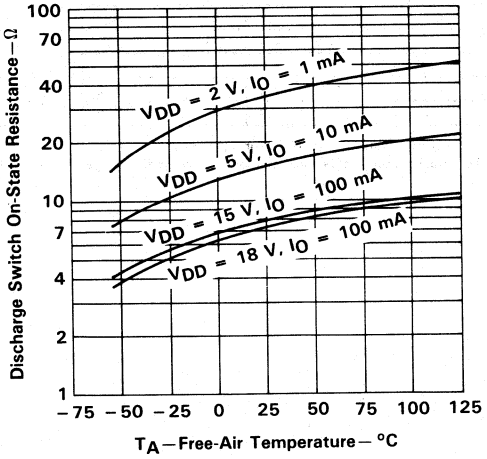
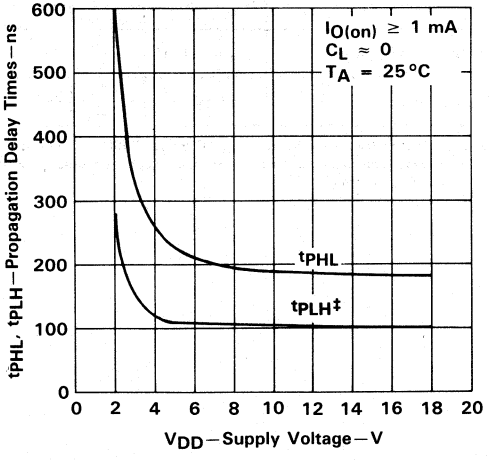


FIGURE 1

PROPAGATION DELAY TIMES
TO DISCHARGE OUTPUT
FROM TRIGGER AND THRESHOLD
SHORTED TOGETHER
vs
SUPPLY VOLTAGE



‡The effects of the load resistance on these values must be taken into account separately.

FIGURE 2

TYPICAL APPLICATION DATA

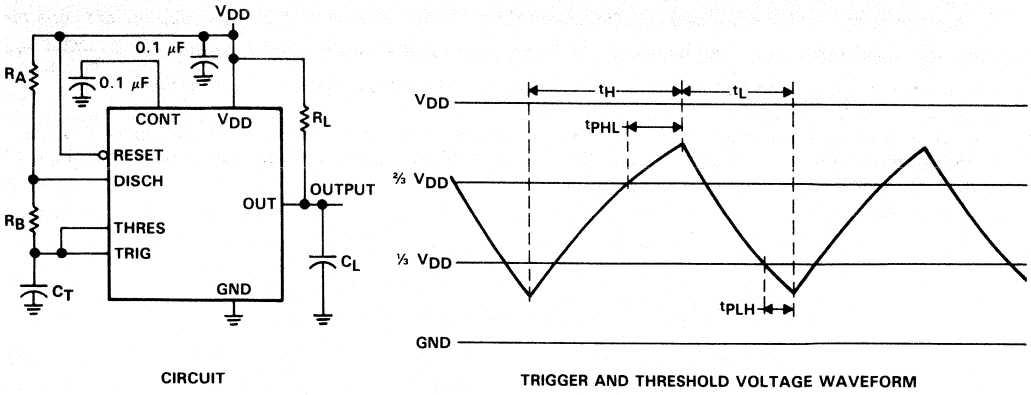


FIGURE 3. ASTABLE OPERATION

Connecting the trigger input to the threshold input, as shown in Figure 3, causes the timer to run as a multivibrator. The capacitor C_T charges through R_A and R_B to the trigger voltage level (approximately $0.67V_{DD}$) and then discharges through R_B only to the value of the threshold voltage level (approximately $0.33V_{DD}$). The output is high during the charging cycle (t_H) and low during the discharge cycle (t_L). The duty cycle is controlled by the values of R_A, R_B, and C_T, as shown in the equations below.

$$t_H \approx C_T (R_A + R_B) \ln 2 \qquad (\ln 2 = 0.693)$$

$$t_L \approx C_T R_B \ln 2$$

$$\text{Period} = t_H + t_L \approx C_T (R_A + 2R_B) \ln 2$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} \approx 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} \approx \frac{R_B}{R_A + 2R_B}$$

The 0.1-μF capacitor at the control pin in Figure 3 decreases the period by about 10%.

The formulas shown above do not allow for any propagation delay from the trigger and threshold inputs to the discharge output. These delay times add directly to the period and create differences between calculated and actual values that increase with frequency. In addition, the discharge output resistance r_{on} adds to R_B to provide another source of error in the calculation when R_B is very low or r_{on} is very high.

The equations below provide better agreement with measured values.

$$t_H = C_T (R_A + R_B) \ln\left[3 - \exp\left(\frac{-t_{PLH}}{C_T (R_B + r_{on})}\right)\right] + t_{PHL}$$

$$t_L = C_T (R_B + r_{on}) \ln\left[3 - \exp\left(\frac{-t_{PHL}}{C_T (R_A + R_B)}\right)\right] + t_{PLH}$$

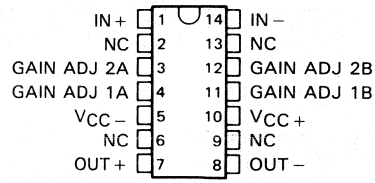
The preceding equations and those given earlier are similar in that a time constant is multiplied by the logarithm of a number or function. The limit values of the logarithmic terms must be between ln 2 at low frequencies and ln 3 at extremely high frequencies. For a duty cycle close to 50%, an appropriate constant for the logarithmic terms can be substituted with good results. Duty cycles less than 50% $\frac{t_H}{t_H + t_L}$ will require that $\frac{t_H}{t_L} < 1$ and possibly $R_A \leq r_{on}$. These conditions can be difficult to obtain.

In monostable applications, the trip point of the trigger input can be set by a voltage applied to the control pin. An input voltage between 10% and 80% of the supply voltage from a resistor divider with at least 500 μA bias provides good results.

D922, NOVEMBER 1970—REVISED APRIL 1988

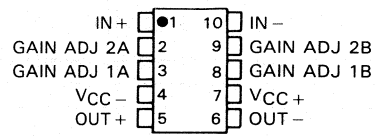
- **200-MHz Bandwidth**
- **250-kΩ Input Resistance**
- **Selectable Nominal Amplification of 10, 100, or 400**
- **No Frequency Compensation Required**
- **Designed to be Interchangeable with Fairchild μA733M and μA733C**

uA733M . . . J DUAL-IN-LINE PACKAGE
uA733C . . . D OR N PACKAGE
(TOP VIEW)



NC—No internal connection

UA733M . . . U FLAT PACKAGE
(TOP VIEW)



description

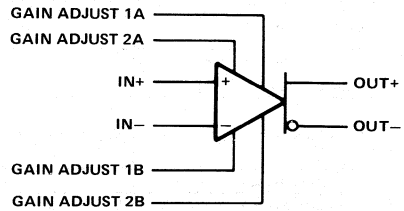
The uA733 is a monolithic two-stage video amplifier with differential inputs and differential outputs.

Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 10, 100, or 400 may be selected without external components, or amplification may be adjusted from 10 to 400 by the use of a single external resistor connected between 1A and 1B. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

symbol



The uA733M is characterized for operation over the full military temperature range of −55°C to 125°C; the uA733C is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		uA733M	UA733C	UNIT
Supply voltage V_{CC+} (See Note 1)		8	8	V
Supply voltage V_{CC-} (See Note 1)		−8	−8	V
Differential input voltage		±5	±5	V
Common-mode input voltage		±6	±6	V
Output current		10	10	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range		−55 to 125	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or U package	300	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or N package		260	°C

NOTE 1. All voltage values, except differential input voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	N/A	N/A	500 mW	N/A
J (uA733M)	500 mW	11.0 mW/°C	104°C	500 mW	275 mW
N	500 mW	N/A	N/A	500 mW	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	135 mW

electrical characteristics, $V_{CC+} = 6$ V, $V_{CC-} = -6$ V, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M MIN	uA733M TYP	uA733M MAX	uA733C MIN	uA733C TYP	uA733C MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	300	400	500	250	400	600	V/V
				2	90	100	110	80	100	120	
				3	9	10	11	8	10	12	
BW	Bandwidth	2	R_S = 50 Ω	1		50			50		MHz
				2		90			90		
				3		200			200		
I_{IO}	Input offset current			Any		0.4	3		0.4	5	μA
I_{IB}	Input bias current			Any		9	20		9	30	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1			±1			V
V_{OC}	Common-mode output voltage	1		Any	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OO}	Output offset voltage	1		1		0.6	1.5		0.6	1.5	V
				2 & 3		0.35	1		0.35	1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	3	4.7		3	4.7		V
r_i	Input resistance	3	$V_{OD} \le 1$ V	1		4			4		kΩ
				2	20	24		10	24		
				3		250			250		
r_o	Output resistance					20			20		Ω
C_i	Input capacitance	3	$V_{OD} \le 1$ V	2		2			2		pF
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	60	86		60	86		dB
			V_{IC} = ±1 V, f = 5 MHz	2		70			70		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50	70		50	70		dB
V_n	Broadband equivalent input noise voltage	5	BW = 1 kHz to 10 MHz	Any		12			12		μV
t_{pd}	Propagation delay time	2	R_S = 50 Ω, Output voltage step = 1 V	1		7.5			7.5		ns
				2		6.0	10		6.0	10	
				3		3.6			3.6		
t_r	Rise time	2	R_S = 50 Ω, Output voltage step = 1 V	1		10.5			10.5		ns
				2		4.5	10		4.5	12	
				3		2.5			2.5		
$I_{sink(max)}$	Maximum output sink current			Any	2.5	3.6		2.5	3.6		mA
I_{CC}	Supply current		No load, No signal	Any		16	24		16	24	mA

† The gain option is selected as follows:
Gain Option1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

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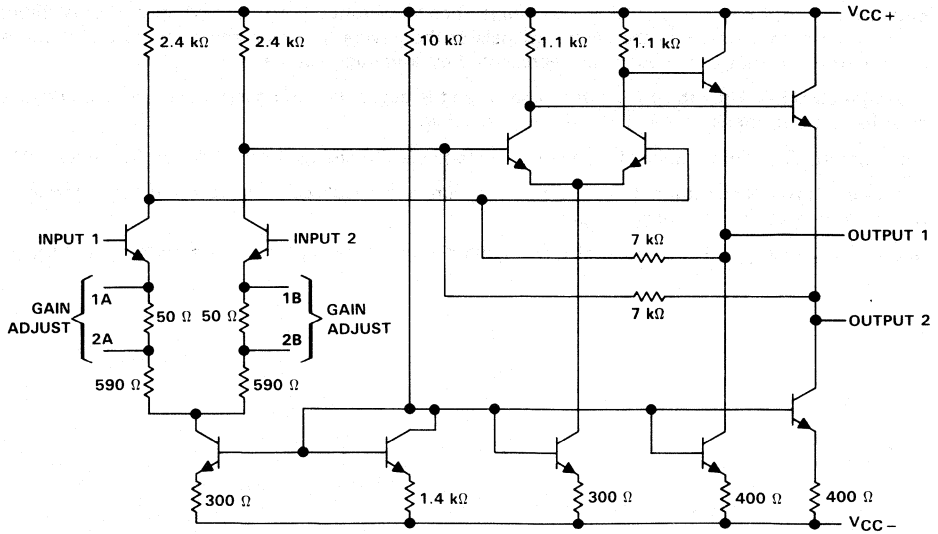
electrical characteristics, V_{CC+} = 6 V, V_{CC-} = −6 V, T_A = −55°C to 125°C for uA733M, 0°C to 70°C for uA733C

PARAMETER		TEST FIGURE	TEST CONDITIONS	GAIN OPTION†	uA733M MIN	uA733M MAX	uA733C MIN	uA733C MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	1	V_{OD} = 1 V	1	200	600	250	600	V/V
				2	80	120	80	120	
				3	8	12	8	12	
I_{IO}	Input offset current			Any		5		6	μA
I_{IB}	Input bias current			Any		40		40	μA
V_{ICR}	Common-mode input voltage range	1		Any	±1		±1		V
V_{OO}	Output offset voltage	1		1		1.5		1.5	V
				2 & 3		1.2		1.5	
V_{OPP}	Maximum peak-to-peak output voltage swing	1		Any	2.5		2.8		V
r_i	Input resistance	3	V_{OD} ≤ 1 V	2	8		8		kΩ
CMRR	Common-mode rejection ratio	4	V_{IC} = ±1 V, f ≤ 100 kHz	2	50		50		dB
			V_{IC} = ±1 V, f = 5 MHz	2					
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	1	ΔV_{CC+} = ±0.5 V, ΔV_{CC-} = ±0.5 V	2	50		50		dB
$I_{sink(max)}$	Maximum output sink current			Any	2.2		2.5		mA
I_{CC}	Supply current		No load, No signal	Any		27		27	mA

†The gain option is selected as follows:
Gain Option 1 . . . Gain-adjust pin 1A is connected to pin 1B, and pins 2A and 2B are open.
Gain Option 2 . . . Gain-adjust pin 1A and pin 1B are open, pin 2A is connected to pin 2B.
Gain Option 3 . . . All four gain-adjust pins are open.

schematic



Component values shown are nominal.

DEFINITION OF TERMS

Large-Signal Differential Voltage Amplification (A_{VD}) The ratio of the change in voltage between the output terminals to the change in voltage between the input terminals producing it.

Bandwidth (BW) The range of frequencies within which the differential gain of the amplifier is not more than 3 dB below its low-frequency value.

Input Offset Current (I_{IO}) The difference between the currents into the two input terminals with the inputs grounded.

Input Bias Current (I_{IB}) The average of the currents into the two input terminals with the inputs grounded.

Input Voltage Range (V_I) The range of voltage that if exceeded at either input terminal will cause the amplifier to cease functioning properly.

Common-Mode Output Voltage (V_{OC}) The average of the d-c voltages at the two output terminals.

Output Offset Voltage (V_{OO}) The difference between the d-c voltages at the two output terminals when the input terminals are grounded.

Maximum Peak-to-Peak Output Voltage Swing (V_{OPP}) The maximum peak-to-peak output voltage swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

Input Resistance (r_i) The resistance between the input terminals with either input grounded.

Output Resistance (r_o) The resistance between either output terminal and ground.

Input Capacitance (C_i) The capacitance between the input terminals with either input grounded.

Common-Mode Rejection Ratio (CMRR) The ratio of differential voltage amplification to common-mode voltage amplification. This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Supply Voltage Rejection Ratio (k_{SVR}) The absolute value of the ratio of the change in power supply voltages to the change in input offset voltage. For these devices, both supply voltages are varied symmetrically.

Equivalent Input Noise Voltage (V_n) The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

Propagation Delay Time (t_{pd}) The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

Rise Time (t_r) The time required for an output voltage step to change from 10% to 90% of its final value.

Maximum Output Sink Current ($I_{sink(max)}$) The maximum available current into either output terminal when that output is at its most negative potential.

Supply Current (I_{CC}) The average of the magnitudes of the two supply currents I_{CC1} and I_{CC2}.

PARAMETER MEASUREMENT INFORMATION

est circuits

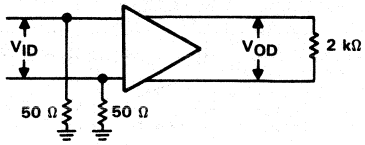


FIGURE 1

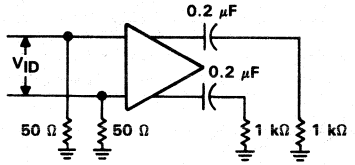


FIGURE 2

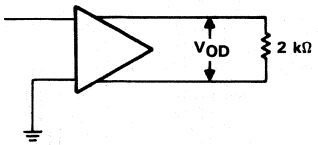


FIGURE 3

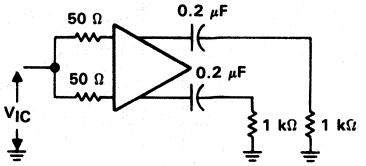


FIGURE 4

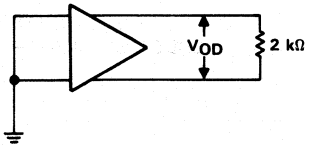
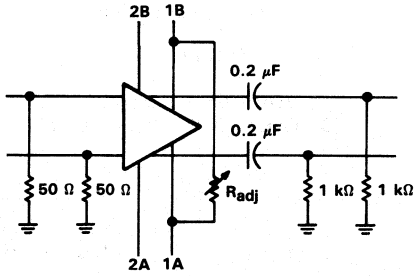


FIGURE 5



VOLTAGE AMPLIFICATION ADJUSTMENT

FIGURE 6

TYPICAL CHARACTERISTICS

PHASE SHIFT
vs
FREQUENCY

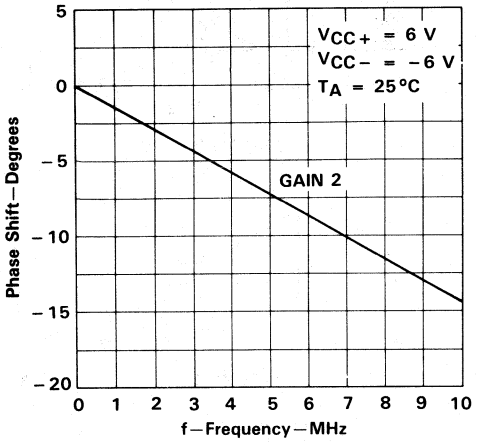


FIGURE 7

PHASE SHIFT
vs
FREQUENCY

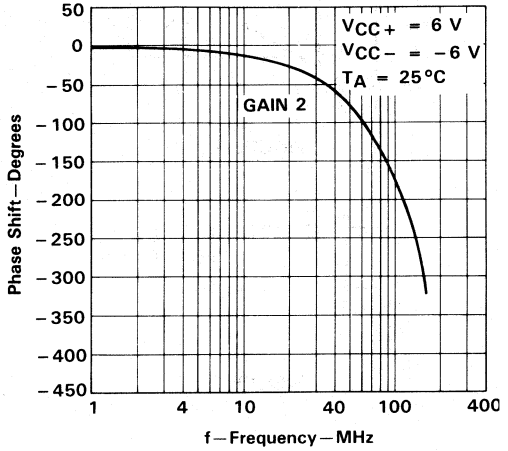


FIGURE 8

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
TEMPERATURE

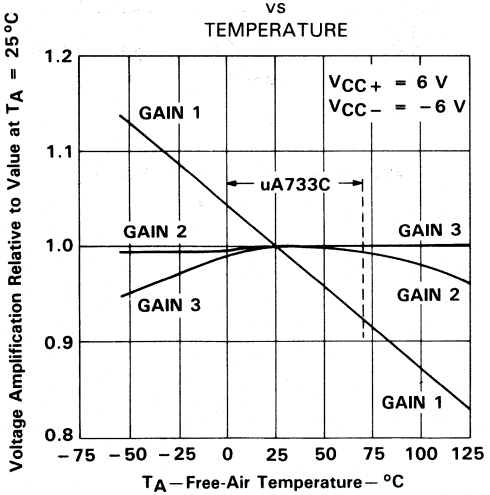


FIGURE 9

VOLTAGE AMPLIFICATION
(SINGLE-ENDED OR DIFFERENTIAL)
vs
SUPPLY VOLTAGE

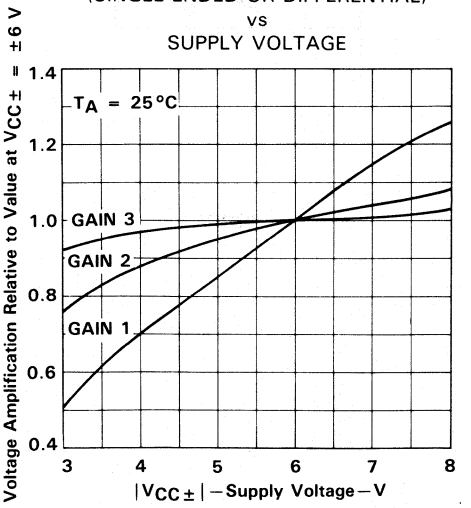


FIGURE 10

4 Special Functions

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
RESISTANCE BETWEEN G1A AND G1B

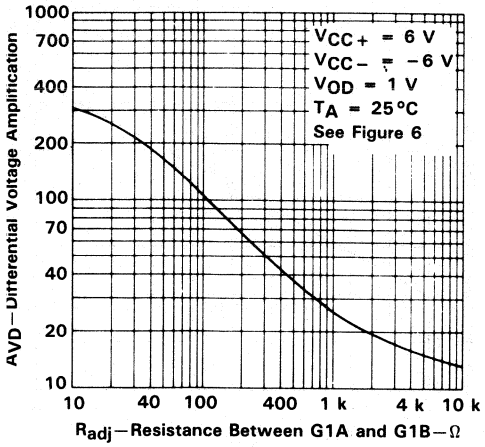


FIGURE 11

SINGLE-ENDED VOLTAGE AMPLIFICATION
vs
FREQUENCY

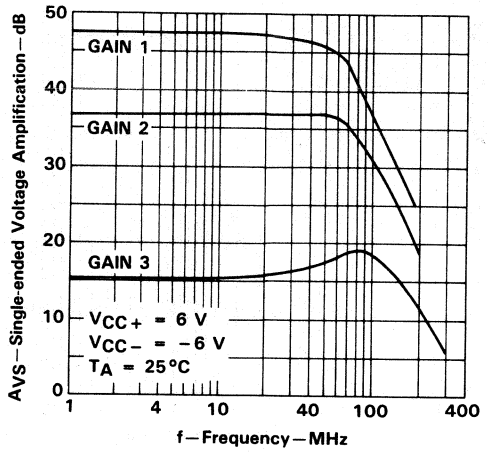


FIGURE 12

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

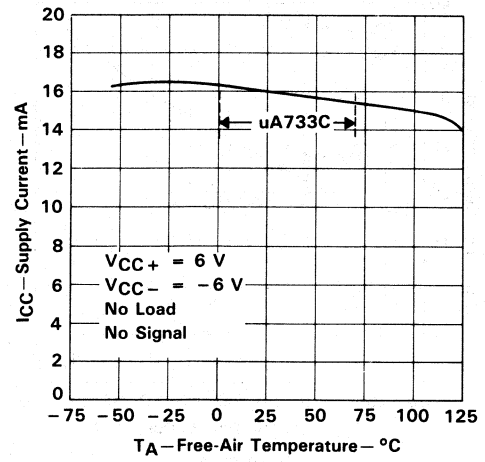


FIGURE 13

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

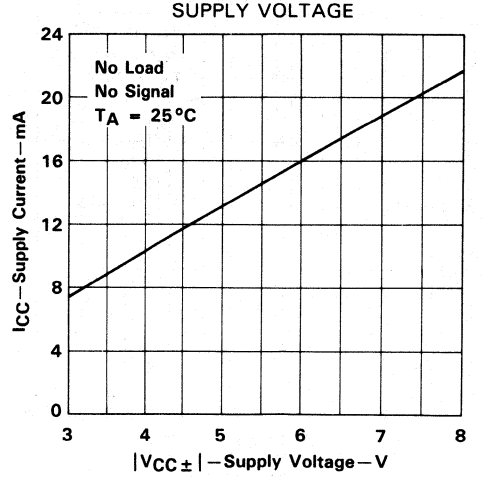


FIGURE 14

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

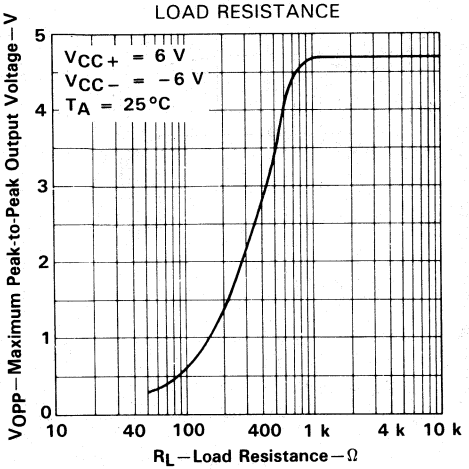


FIGURE 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

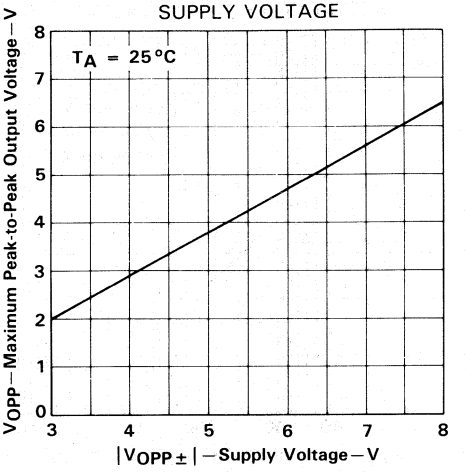


FIGURE 16

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

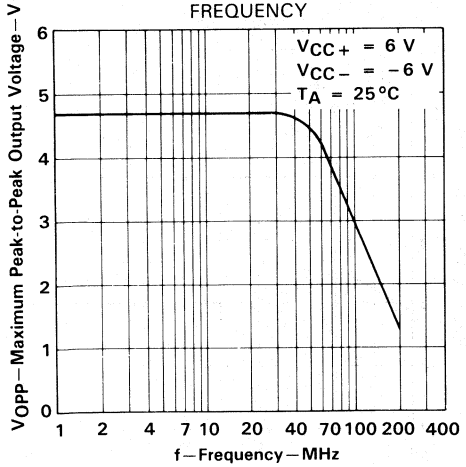


FIGURE 17

INPUT RESISTANCE
vs
FREE-AIR TEMPERATURE

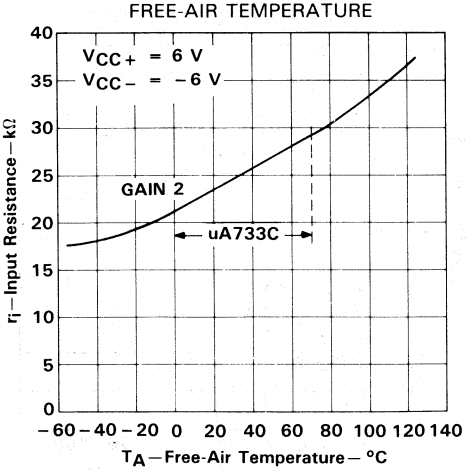
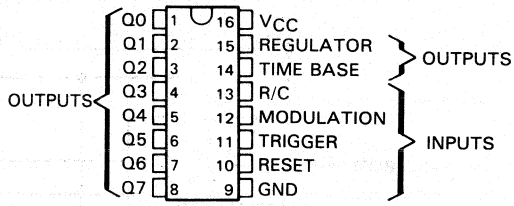


FIGURE 18

D2442, JUNE 1978 – REVISED MAY 1988

- **Accurate Timing from Microseconds to Days**
- **Programmable Delays from 1 Time Constant to 255 Time Constants**
- **Outputs Compatible with TTL and CMOS**
- **Wide Supply-Voltage Range**
- **External Sync and Modulation Capability**

N DUAL-IN-LINE PACKAGE
(TOP VIEW)



escription

These circuits consist of a time-base oscillator, and eight-bit counter, a control flip-flop, and a voltage regulator. The frequency of the time-base oscillator is set by the time constant of an external resistor and capacitor at pin 13 and can be synchronized or modulatd by signals applied to the modulation input. The output of the time-base section is applied directly to the input of the counter section and also appears at pin 14 (time base). The time-base pin may be used to monitor the frequency of the oscillator, to provide an output pulse to other circuitry, or (with the time-base section disabled) to drive the counter input from an external source. The counter input is activated on a negative-going transition. The reset input stops the time-base oscillator and sets each binary output, Q0 through Q7, and the time-base output to a TTL high level. After resetting, the trigger input starts the oscillator and all Q outputs go low. Once triggered, the uA2240C will ignore any signals at the trigger input until it is reset.

The uA2240C timer/counter may be operated in the free-running mode or with output-signal feedback to the reset input for automatic reset. Two or more binary outputs may be connected together to generate complex pulse patterns, or each output may be used separately to provide eight output frequencies. Using two circuits in cascade can provide precise time delays of up to three years.

The uA2240C is characterized for operation from 0°C to 70°C.

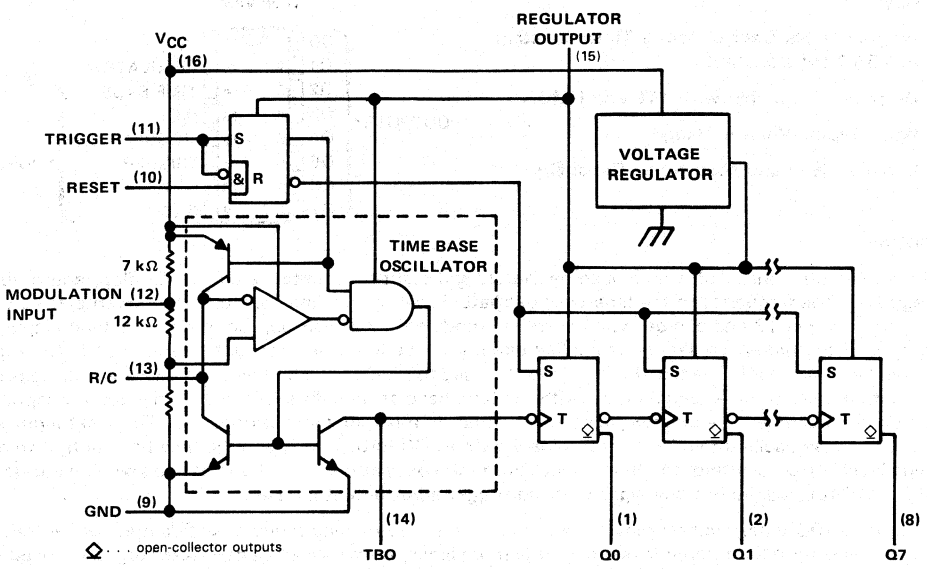
AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE	V_T MAX at 25°C
DEVICE	PACKAGE SUFFIX		
uA2240C	N	0°C to 70°C	2 V

4

Special Functions

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 18 V
Output voltage: Q0 thru Q7 . . . . . 18 V
Output current: Q0 thru Q7 . . . . . 10 mA
Regulator output current . . . . . −5 mA
Continuous dissipation at (or below) 25°C free-air temperature . . . . . 650 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4		14	V
Timing resistor	0.001		10	MΩ
Timing capacitor	0.01		1000	μF
Counter input frequency (Pin 14)		1.5		MHz
Pull-up resistor, time-base output		20		kΩ
Trigger and reset input pulse voltage	2	3		V
Trigger and reset input pulse duration	2			μs
External clock input pulse voltage	3			V
External clock input pulse duration	1			μs

NOTE 2: For operation with $V_{CC} \leq 4.5$ V, short regulator output to V_{CC}.

ectrical characteristics at 25°C free-air temperature

PARAMETER	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Regulator output voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	3.9	4.4		V
	2	V_{CC} = 15 V, Trigger and reset open or grounded	5.8	6.3	6.8	
Modulation input open circuit voltage	1	V_{CC} = 5 V, Trigger and reset open or grounded	2.8	3.5	4.2	V
		V_{CC} = 15 V, Trigger and reset open or grounded		10.5		
Trigger threshold voltage	1	V_{CC} = 5 V, Reset at 0 V		1.4	2	V
High-level trigger current	1	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V		10		μA
Reset threshold voltage	1	V_{CC} = 5 V, Trigger at 0 V		1.4	2	V
High-level reset current	1	V_{CC} = 5 V, Trigger at 0 V		10		μA
Counter input (time base) threshold voltage	2	V_{CC} = 5 V, Trigger and reset open or grounded	1	1.4		V
Low-level output current, Q0 thru Q7	2	V_{CC} = 5 V, Trigger at 2 V, Reset at 0 V, V_{OL} < 0.4 V	2	4		mA
High-level output current, Q0 thru Q7	2	V_{OH} = 15 V, Reset at 2 V, Trigger at 0 V		0.01	15	μA
Supply current	1	V_{CC} = 5 V, Trigger at 0 V, Reset at 5 V		4	7	mA
	1	V_{CC} = 15 V, Trigger at 0 V, Reset at 5 V		13	18	
	3	V+ = 4 V		1.5		

perating characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER	TEST CIRCUIT	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Initial error of time base‡	1	V_{CC} = 5 V, Trigger at 5 V, Reset at 0 V			±0.5	±5	%
Temperature coefficient of time-base period	1	T_A = 0°C to 70°C	V_{CC} = 5 V		−200		ppm/°C
			V_{CC} = 15 V		−80		
Supply voltage sensitivity of time-base period	1	V_{CC} ≥ 8 V			−0.08	−0.3	%/V
Time-base output frequency	1	V_{CC} = 5 V, R = MIN, C = MIN			130		kHz
Propagation delay time		see Note 3	From trigger input		1		μs
			From reset input		0.8		
Output rise time	2	R_L = 3 kΩ, C_L = 10 pF	Q0 thru Q7		180		ns
Output fall time					180		

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
This is the time-base period error due only to the uA2240C and expressed as a percentage of nominal (1.00 RC).
OTE 3: Propagation delay time is measured from the 50% point on the leading edge of an input pulse to the 50% point on the leading edge of the resulting change of state at Q0.

PARAMETER MEASUREMENT INFORMATION

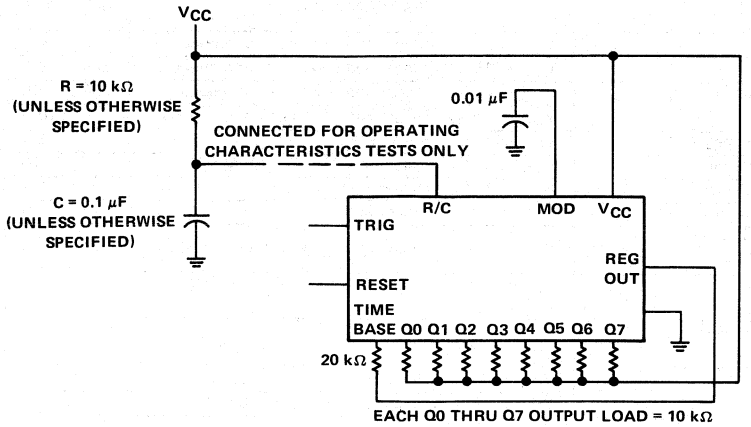


FIGURE 1. GENERAL TEST CIRCUIT

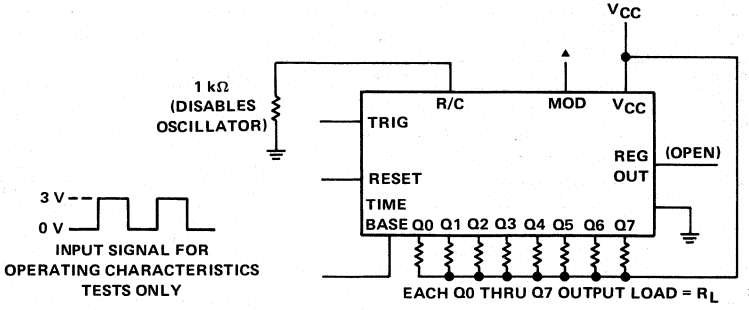


FIGURE 2. COUNTER TEST CIRCUIT

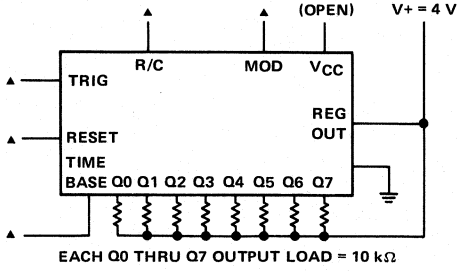


FIGURE 3. REDUCED-POWER TEST CIRCUIT (TIME BASE DISABLED)

▲These connections may be open or grounded for this test.

TYPICAL CHARACTERISTICS

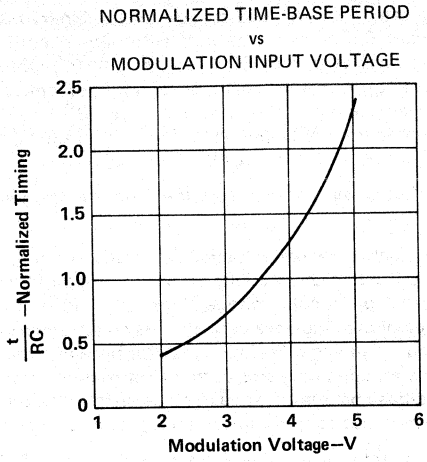


FIGURE 4

TYPICAL APPLICATION INFORMATION

Figure 5 shows voltage waveforms for typical operation of the uA2240C. If both reset and trigger inputs are low during power-up, the timer/counter will be in a reset state with all binary (Q) outputs high and the oscillator stopped. In this state, a high level on the trigger input starts the time-base oscillator. The initial negative-going pulse from the oscillator sets the Q outputs to low logic levels at the beginning of the first time-base period. The uA2240C will ignore any further signals at the trigger input until after a reset signal is applied to the reset input. With the trigger input low, a high level at the reset input will set Q outputs high and stop the time-base oscillator. If the reset signal occurs while the trigger input is high, the reset is ignored. If the reset input remains high when the trigger input goes low, the uA2240C will reset.

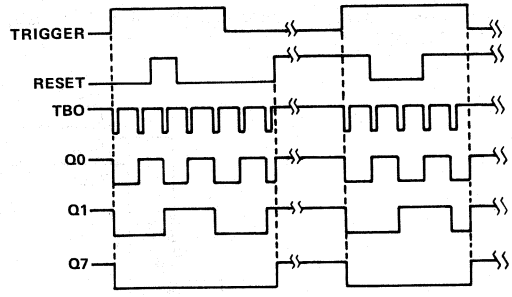


FIGURE 5. TIMING DIAGRAM OF OUTPUT WAVEFORMS

TYPICAL APPLICATION INFORMATION

In monostable applications of the uA2240C, one or more of the binary outputs will be connected to th reset terminal as shown in Figure 6. The binary outputs are open-collector stages that can be connecte together to a common pull-up resistor to provide a "wired-OR" function. The combined output will b low as long as any one of the outputs is low. This type of arrangement can be used for time delays tha are integer multiples of the time-base period. For example, if Q5 ($2^5 = 32$) only is connected to the rese input, every trigger pulse will generate a 32-period active-low output. Similarly, if Q0, Q4, and Q5 ar connected to reset, each trigger pulse creates a 49-period delay.

In astable operation, the uA2240C will free-run from the time it is triggered until it receives an externa reset signal.

The period of the time-base oscillator is equal to the RC time constant of an external resistor and capacitc connected as shown in Figure 6 when the modulation input is open (approximately 3.5 V internal, se Figure 4). Under conditions of high supply voltage ($V_{CC} > 7$ V) and low value of timing capacitc ($C < 0.1\ \mu F$), the pulse duration of the time-base oscillator may be too short to properly trigger the counters This situation can be corrected by adding a 300-pF capacitor between the time-base output and grounc The time-base output (TBO) is an open-collector output that requires a 20-kΩ pull-up resistor to Pin 1 for proper operation. The time-base pin may also be used as an input to the counters for an external time base or as an active-low inhibit input to interrupt counting without resetting.

The modulation input varies the ratio of the time-base period to the RC time constant as a function o the dc bias voltage (see Figure 4). It can also be used to synchronize the timer/counter to an external cloc or sync signal.

The regulator output is used internally to drive the binary counters and the control logic. This termina can also be used to supply voltage to additional uA2240C devices to minimize power dissipation whe several timer circuits are cascaded. For circuit operation with an external clock, the regulator output ca be used as the V_{CC} input terminal to power down the internal time base and reduce power dissipation When supply voltages less than 4.5 V are used with the internal time base, Pin 15 should be shorted t Pin 16.

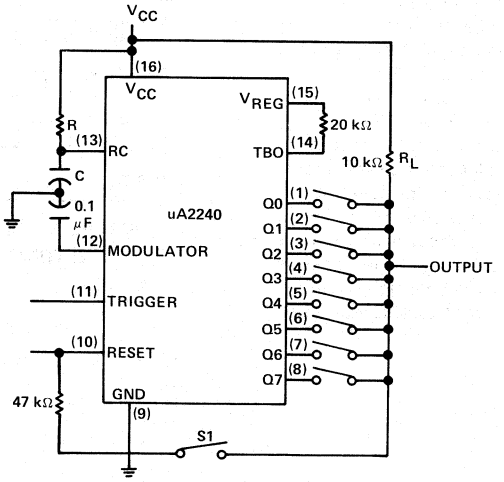


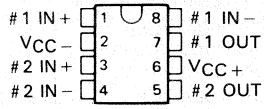
FIGURE 6. BASIC CONNECTIONS FOR TIMING APPLICATIONS

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

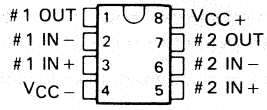
D3237, MAY 1988 – REVISED FEBRUARY 1989

- **Single-Supply Operation:**
  Input Voltage Range Extends to Ground
  Output Swings to Ground While Sinking Current
- **Input Offset Voltage . . . 150 μA Max at 25°C for LT1013AM, LT1013AC**
- **Offset Voltage Temperature Coefficient . . . 2 μV/°C Max for LT1013AM, LT1013AC**
- **Input Offset Current . . . 0.8 nA Max at 25°C for LT1013AM, LT1013AC**
- **High Gain . . . 1.5 V/μV Min (R_L = 600 Ω), 0.8 V/μV Min (R_L = 2 kΩ) for LT1013AM, LT1013AC**
- **Low Supply Current . . . 0.5 mA Max at 25°C for LT1013AM, LT1013AC**
- **Low Peak-To-Peak Noise Voltage . . . 0.55 μV Typ**
- **Low Current Noise . . . 0.07 pA/$\sqrt{Hz}$ Typ**

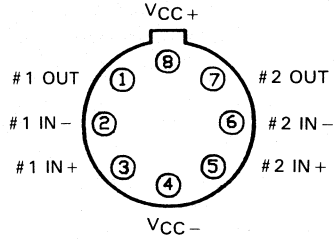
D PACKAGE
(TOP VIEW)



JG OR P PACKAGE
(TOP VIEW)



L PACKAGE
(TOP VIEW)



Pin 4 (L package) is in electrical contact with the case.

Description

The LT1013 is a precision dual operational amplifier with an 8-pin industry-standard configuration. It features low offset voltage temperature coefficient, high gain, low supply current, and low noise.

The LT1013 can be operated from a single 5-V power supply; the common-mode input voltage range includes ground, and the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent in previous single-supply designs, is eliminated. The LT1013 is fully specified for both dual ±15-V and single 5-V supplies.

The LT1013AM and LT1013M are characterized for operation over the full military temperature range of −55°C to 125°C. The LT1013AC, LT1013C, and LT1013D are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX at 25°C	PACKAGE			
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
0°C to 70°C	150 μV		LT1013ACJG	LT1013ACL	
	300 μV		LT1013CJG	LT1013CL	LT1013CP
	800 μV	LT1013DD			LT1013DP
−55°C to 125°C	150 μV		LT1013AMJG	LT1013AML	
	300 μV		LT1013MJG	LT1013ML	

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LT1013DDR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1) . . . . . 22 V
Supply voltage, V_{CC-} . . . . . −22 V
Differential input voltage . . . . . ±30 V
Input voltage range, V_I . . . . . V_{CC-} −5 V to V_{CC+}
Duration of output short-circuit at (or below) 25°C . . . . . unlimited
Operating free-air temperature range: LT1013AM, LT1013M . . . . . −55°C to 125°C
LT1013AC, LT1013C, LT1013D . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG or L package . . . . . 300°C

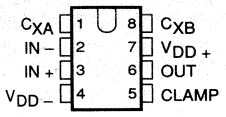
NOTE 1: All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

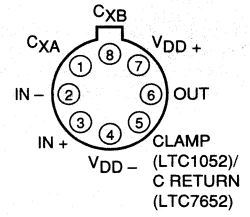
D3238, MAY 1988 – REVISED MARCH 1989

- **Input Offset Voltage . . . 5 μV Max at 25°C**
- **Temperature Coefficient of Input Offset Voltage . . . 0.01 μV/°C Typ**
- **Long-Term Drift of Input Offset Voltage . . . 100 nV/mo Typ**
- **Maximum Input Bias Current . . . 30 pA at 25°C**
- **Minimum Differential Voltage Amplification Over Full Temperature Range . . . 120 dB**
- **Minimum Common-Mode Rejection Ratio Over Full Temperature Range . . . 120 dB**
- **Minimum Supply Voltage Rejection Ratio Over Full Temperature Range . . . 120 dB**
- **Single-Supply Operation from 4.75 V to 16 V (Input Voltage Range Extends to Ground)**
- **External Capacitors Can Be Returned to V_{DD-} with No Noise Degradation**

LTC1022 . . . JG OR P PACKAGE
(TOP VIEW)



LTC1052, LTC7652 . . . L PACKAGE
(TOP VIEW)



Pin 4 (L package) is in electrical contact with the case.

AVAILABLE OPTIONS

T_A	PACKAGE		
	CERAMIC DIP (JG)	METAL CAN (L)	PLASTIC DIP (P)
– 40°C to 85°C	LTC1052CJG	LTC1052CL LTC7652CL	LTC1052CP
– 55°C to 125°C	LTC1052MJG	LTC1052ML	LTC1052MP

description

The LTC1052 and LTC7652 are low-noise chopper-stabilized operational amplifiers manufactured using CMOS silicon-gate technology. The devices are well-suited for applications such as thermocouple amplifiers, strain-gauge amplifiers, low-level signal processing, and medical instrumentation.

Chopper stabilization constantly corrects input offset voltage errors, including both errors in the initial input offset voltage and errors in input offset voltage due to time, temperature, and common-mode input voltage. The chopper circuitry is internal and completely transparent to the user. Only two external capacitors are required to alternately sample and hold the offset correction voltage and the amplified input signal.

Low-frequency (1/f) noise is also improved by the chopping technique. Instead of noise increasing continuously at a rate of 3 dB/octave, the internal chopping causes noise to decrease at low frequencies. Picoampere input currents further enhance the performance of these devices.

The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C. The C-suffix devices are characterized for operation from –40°C to 85°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD+} (see Notes 1 and 2) . . . . . 8 V
Supply voltage, V_{DD-} (see Notes 1 and 2) . . . . . −8 V
Input voltage range, V_I (any input, see Note 1) . . . . . ±16 V
Duration of short-circuit current at (or below) 25°C (see Note 2) . . . . . unlimited
Operating free-air temperature, T_A: M-suffix . . . . . −55°C to 125°C
C-suffix . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or L package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Connecting any terminal to voltages greater than V_{DD+} or less than V_{DD-} may cause destructive latch-up. No sources operating from external supplies should be applied prior to device power-up.
3. The output may be shorted to either supply.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, $V_{DD\pm}$ = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	LTC1052M			LTC1052C, LTC7652C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		0.5	5		0.5	5	μV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.01	0.05		0.01	0.05	μV/°C
	Long-term drift of input offset voltage		25°C		100			100		nV/mo
I_{IO}	Input offset current		25°C		5	30		5	30	pA
			Full range			2000			350	
I_{IB}	Input bias current		25°C		1	30		1	30	pA
			Full range			1000			175	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	−5 to 2.7			−5 to 2.7			V
V_{OM}	Maximum peak output voltage swing	R_L = 100 kΩ, See Note 4	25°C		4.95			4.95		V
		R_L = 10 kΩ, See Note 4	Full range	4.7			4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 10 kΩ	25°C	120	150		120	150		dB
			Full range	120			120			
f_{ch}	Internal chopping frequency		25°C		330			330		Hz
	On-state clamp current	R_L = 100 kΩ	25°C		100			100		μA
			Full range	25			25			
	Off-state clamp current	V_O = −4 V to 4 V	25°C		10	100		10	100	pA
			Full range			2			1	nA
CMRR	Common-mode rejection ratio	V_O = 0, V_{IC} = V_{ICR} min, R_S = 50 Ω	25°C	120	140		120	140		dB
			Full range	120			120			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	$V_{CC\pm}$ = ±2.375 V to ±8 V, V_O = 0, R_S = 50 Ω	25°C	120	150		120	150		dB
			Full range	120			120			
I_{DD}	Supply current	V_O = 0, No load	25°C		1.7	2		1.7	2	mA
			Full range			3			3	

†Full range is −55°C to 125°C for the LTC1052M and −40°C to 85°C for the LTC1052C and LTC7652C.
NOTE 4: Output clamp is not connected.

operating characteristics, $V_{DD\pm}$ = ±5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate	R_L = 10 kΩ, C_L = 50 pF		4		V/μs
V_{NPP}	Peak-to-peak equivalent input noise voltage	R_S = 100 Ω to 10 Hz		1.5		μV
		R_S = 100 Ω to 1 Hz		0.5		
I_n	Input noise current (see Note 5)	f = 10 Hz		0.6		fA/√Hz
GBP	Gain bandwidth product			1.2		MHz

NOTE 5: Equivalent input noise current is calculated as follows: $I_n = (2q \times I_{IB})^{1/2}$, where $q = 1.6 \times 10^{-19}$.

- **Excellent Input Offset Voltage Stability with Temperature . . . 2 μV/°C Typ**
- **Long-Term Drift of Input Offset Voltage . . . 0.005 μV/mo Typ**
- **High Slew Rate . . . 0.9 V/μs Typ**
- **High Unity-Gain Bandwidth . . . 2 MHz Typ**
- **Low Supply Current . . . 200 μA/Amplifier**
- **Phase-Reversal Protection**
- **Stable Supply Current with Temperature . . . 0.08 μA/°C Typ**
- **Full Electrical Parameters Specified at $V_{CC\pm}$ = ±15 V and V_{CC} = 5 V to GND**
- **Common-Mode Input Voltage Range Includes the Negative Rail**

description

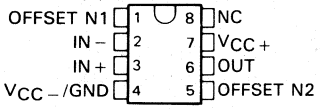
The TLE2021, TLE2022, and TLE2024 are high-precision, high-speed, low-power operational amplifiers using Texas Instruments patent-pending Excalibur process. Available in standard-pinout single, dual, and quad configurations, these devices offer improved slew rate and unity-gain bandwidth performance over the popular OP21, OP22I, and OP42I. A wide variety of packaging options is available, including small-outline (SO) and chip carrier versions for high-density systems applications.

The complementary bipolar Excalibur process uses isolated vertical P-N-P transistors that yield dramatic improvement in gain-bandwidth product and slew rate compared to similar devices. The addition of a patent-pending bias circuit in conjunction with this process results in unsurpassed parameter stability with both time and temperature. This means that a "precision" device remains a precision device even with extreme changes in temperature and over years of use.

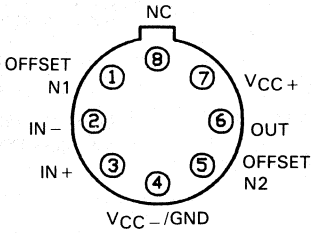
The combination of excellent dc performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for low-level signal conditioning applications in either single-supply or split-supply configurations. Additionally, these devices offer phase-reversal protection circuitry that eliminates an unexpected change in output states when one of the inputs goes below the negative supply rail.

The M-suffix devices are characterized for operation over the full military temperature range of −55°C to 125°C. The I-suffix devices are characterized for operation from −40°C to 85°C, and the C-suffix devices are characterized for operation from 0°C to 70°C.

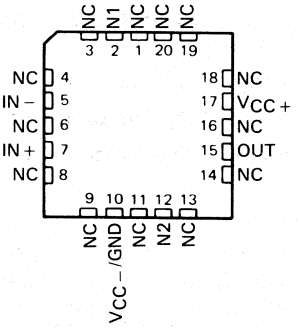
TLE2021 . . . D, JG, OR P PACKAGE
(TOP VIEW)



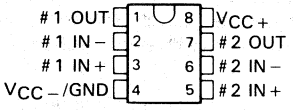
TLE2021 . . . L PACKAGE
(TOP VIEW)



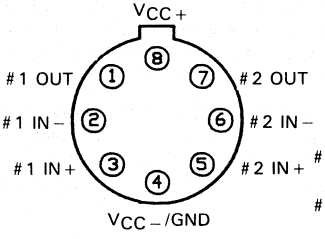
TLE2021 . . . FK PACKAGE
(TOP VIEW)



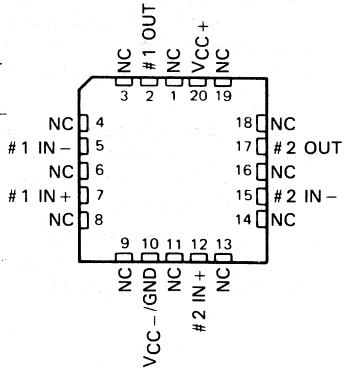
TLE2022 . . . D, JG, OR P PACKAGE
(TOP VIEW)



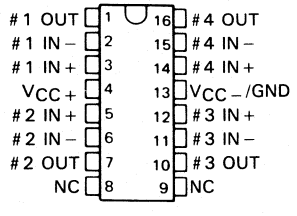
TLE2022 . . . L PACKAGE
(TOP VIEW)



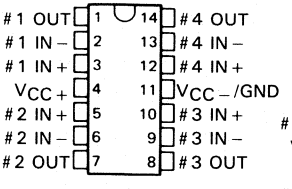
TLE2022 . . . FK PACKAGE
(TOP VIEW)



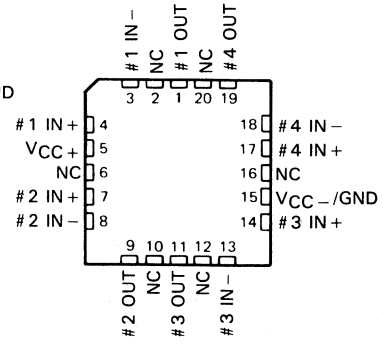
TLE2024 . . . DW PACKAGE
(TOP VIEW)



TLE2024 . . . J OR N PACKAGE
(TOP VIEW)



TLE2024 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Contents

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.

EXAMPLE: TL 514M J /883B

Prefix

MUST CONTAIN TWO OR THREE LETTERS

SN . . . TI Special Functions or Interface Products
TL, TLE . . . . . TI Linear Products
TLC . . . . . TI Linear Silicon-Gate CMOS Products

STANDARD SECOND-SOURCE PREFIXES

LT . . Linear Technology
LTC . Linear Technology
MC . . . . . Motorola
LF, LM, LP, or MF . . . . . National
uA . . . . . Fairchild/National
OP. . . . . PMI
RC, RM, or RV . Raytheon
NE, SA, or SE . . Signetics

Unique Circuit Description Including Temperature Range

MUST CONTAIN TWO TO SIX CHARACTERS
(From Individual Data Sheets)

Examples: 853 1078 2652A 27M2AC

Package

MUST CONTAIN ONE OR TWO LETTERS

D, DW, FK, FN, J, JG, L, LP, LU, N, NT, P, U, W
(From Pin-Connection Diagrams on Individual Data Sheet)

MIL-STD-883B, Method 5004, Class B

OMIT/883B WHEN NOT APPLICABLE

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

Small Outline (D, DW)
Dual-In-Line (J, JG, N, NT, P)
—Slide Magazines
—A-Channel Plastic Tubing
—Sectioned Cardboard Box
—Individual Cardboard Box

Chip Carriers (FK, FN)
—Anti-Static Plastic Tubing

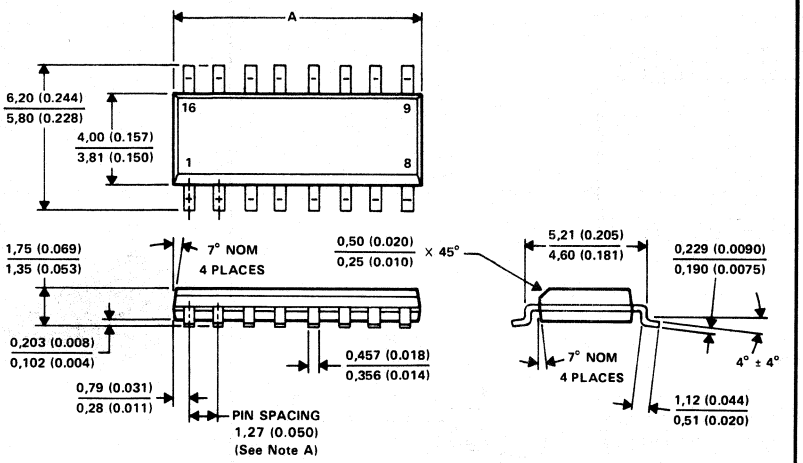
Flat (U, W)
—Milton Ross Carriers

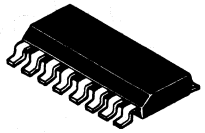
Plug-In (L, LP, LU)
—Sectional Cardboard Box
—Individual Cardboard Box

D008, D014, and D016 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)





DIM \ PINS	8	14	16
A MIN	4,80	8,55	9,80
	(0.189)	(0.337)	(0.386)
A MAX	5,00	8,74	10,00
	(0.197)	(0.344)	(0.394)

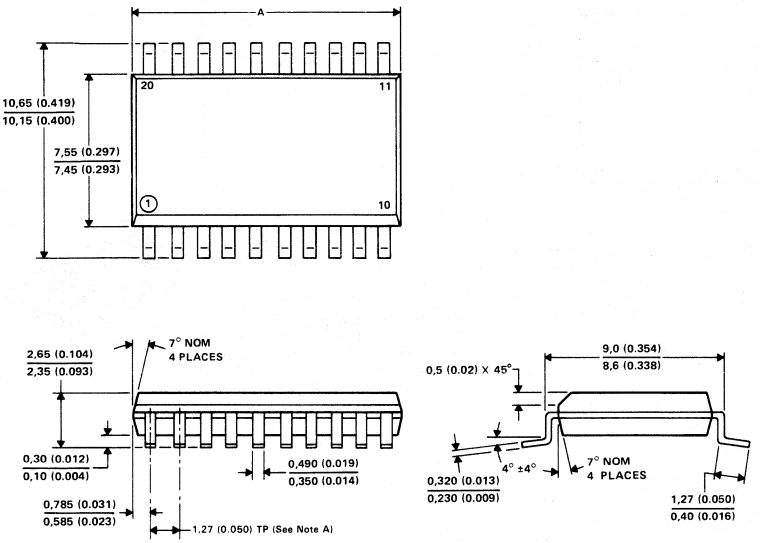
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

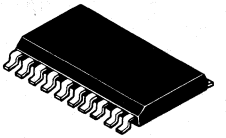
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

DW016, DW020, DW024, and DW028 plastic "small outline" packages

Each of these "small outline" packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

DW016, DW020, DW024, and DW028
(20-pin package used for illustration)





DIM \ PINS	16	20	24	28†
A MIN	10,16	12,70	15,29	17,68
	(0.400)	(0.500)	(0.602)	(0.696)
A MAX	10,36	12,90	15,49	17,88
	(0.408)	(0.508)	(0.610)	(0.704)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

†The 28-pin package drawing is presently classified as Advance Information.

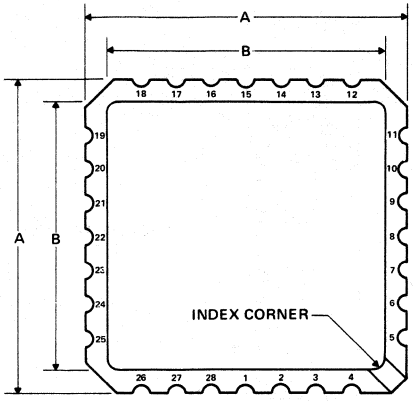
NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

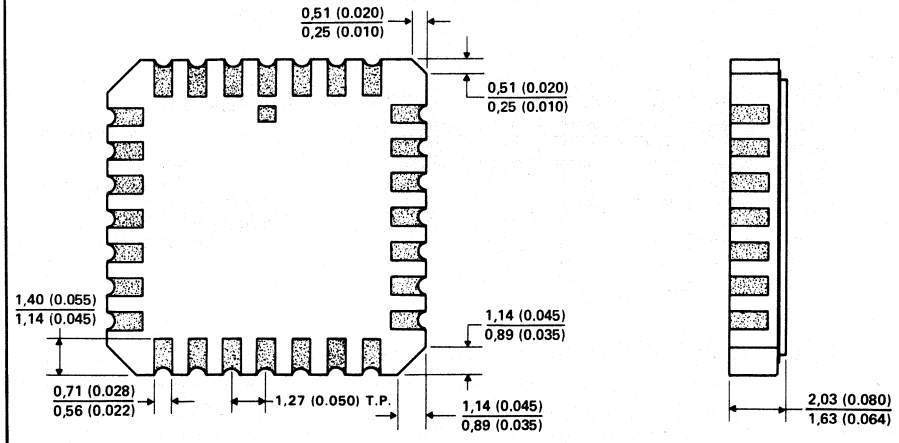
FK020 and FK028
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.

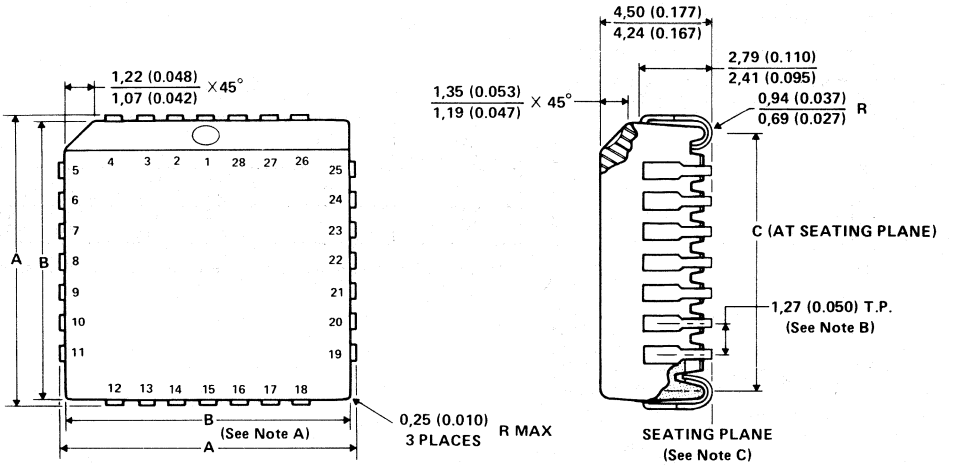


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

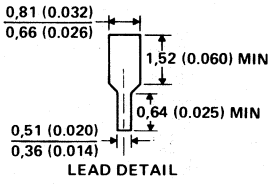
FN020, FN028, FN044, FN068, and FN084 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020, FN028, FN044, FN068, and FN084
(28-terminal package used for illustration)



NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
20	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,87 (0.310)	8,38 (0.330)
28	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,41 (0.410)	10,92 (0.430)
44	17,40 (0.685)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,49 (0.610)	16,00 (0.630)
68	25,02 (0.985)	25,27 (0.995)	24,13 (0.950)	24,33 (0.956)	23,11 (0.910)	23,62 (0.930)
84	30,10 (1.185)	30,35 (1.195)	29,21 (1.150)	29,41 (1.158)	27,69 (1.090)	28,70 (1.130)



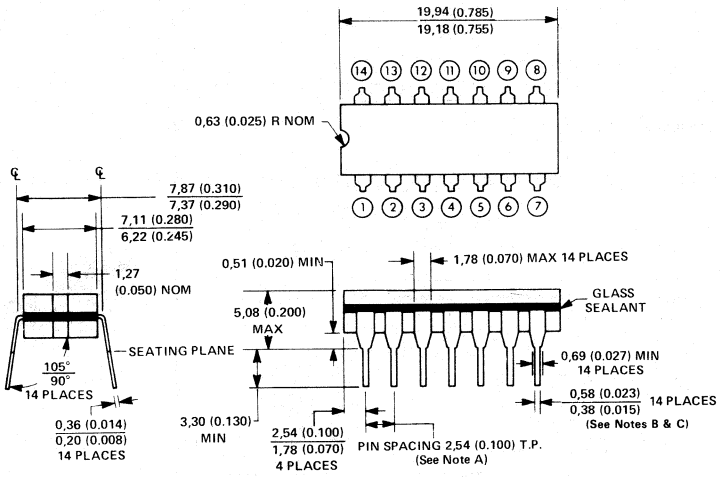
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

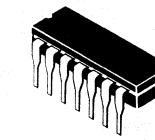
NOTES: A. Centerline of center pin each side is within 0,10 (0.004) of package centerline as determined by dimension B.
B. Location of each pin is within 0,127 (0.005) of true position with respect to center pin on each side.
C. The lead contact points are planar within 0,10 (0.004).

J014 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

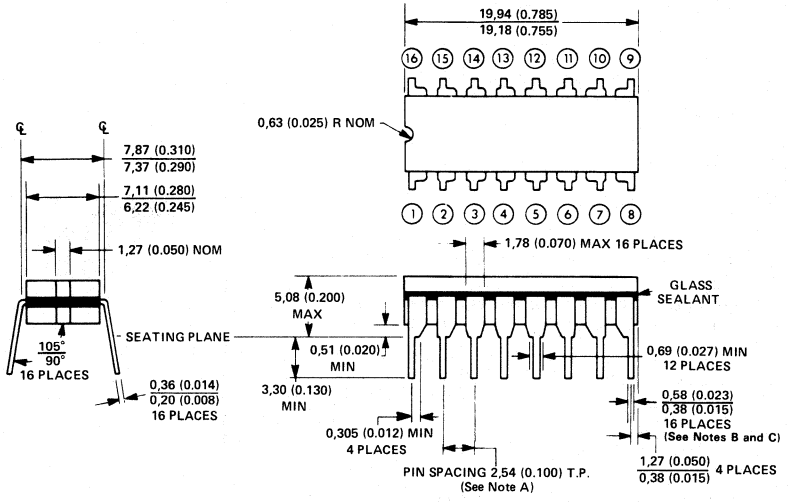
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

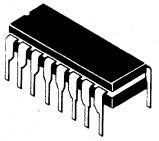
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

J016 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J016





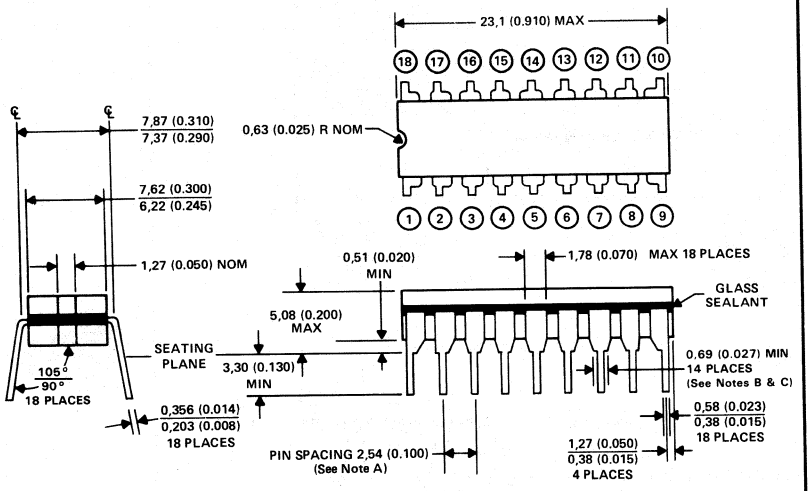
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

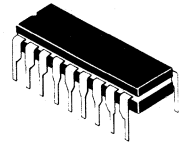
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

018 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated (''bright-dipped'') leads require no additional cleaning or processing when used in soldered assembly.

J018



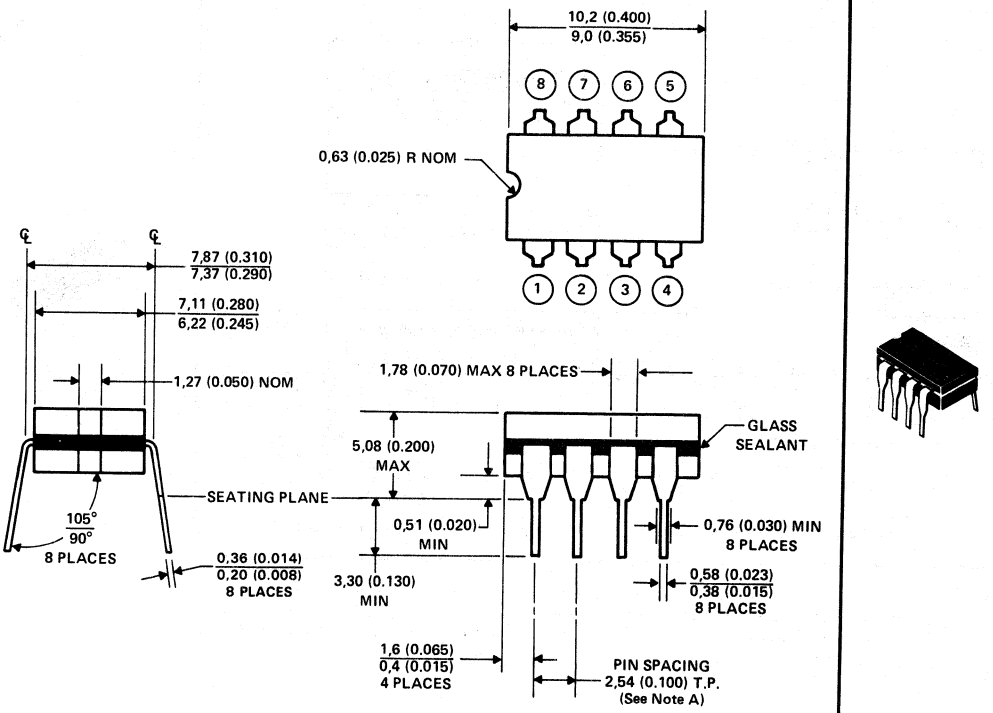


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

JG008 ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and an 8-pin leac frame. The package is intended for insertion in mounting-hole rows 7,62 (0.300) centers (see Note A) Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering.

JG008



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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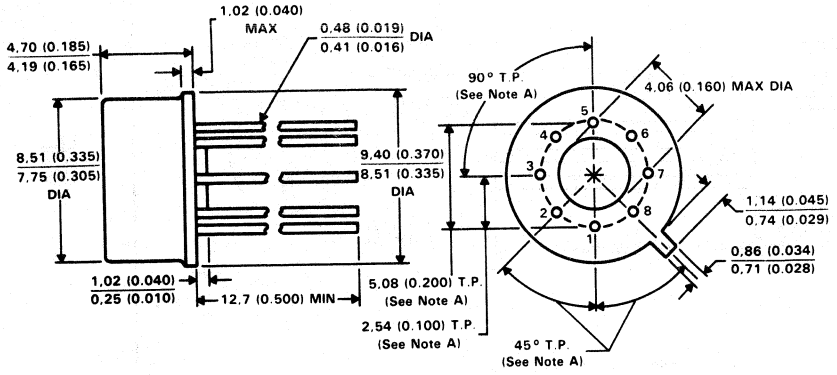
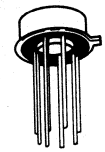
008 metal cylindrical package

This hermetically sealed cylindrical package consists of a welded metal base and cap with individual leads secured by an insulating glass sealant. The gold-plated leads (—00) require no additional cleaning or processing when used in soldered assembly.

L008





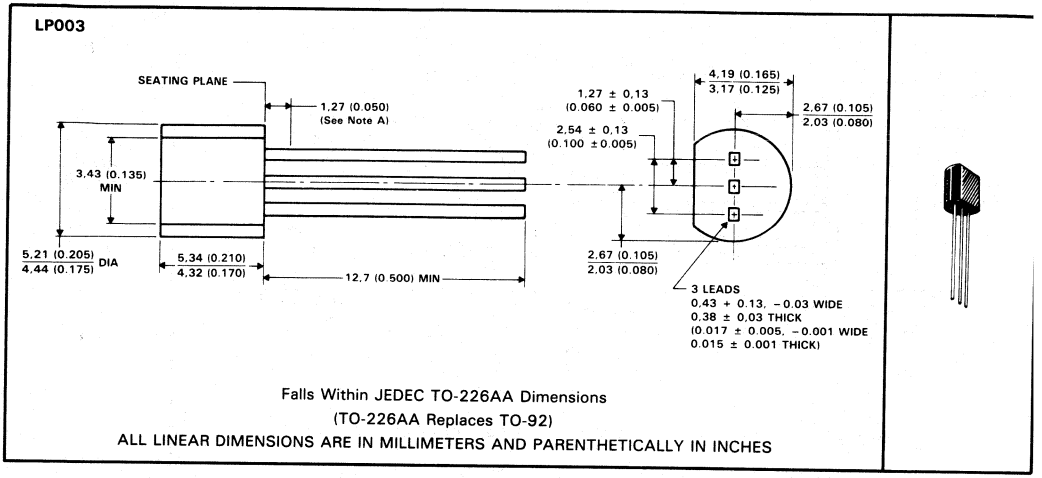
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

Same as JEDEC TO-99 and MO-002AK except for diameter of standoff

NOTE A: Each lead is located within 0,18 (0.007) of its true position at maximum material condition.

LP003 cylindrical plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTE A: Lead dimensions are not controlled within this area.

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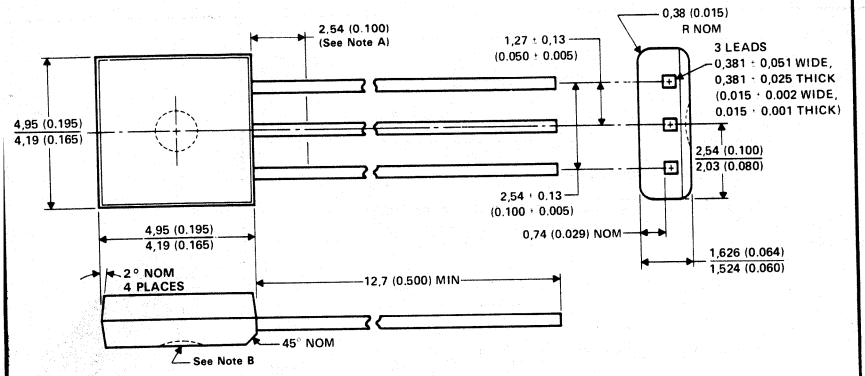
U003 plastic package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

LU003



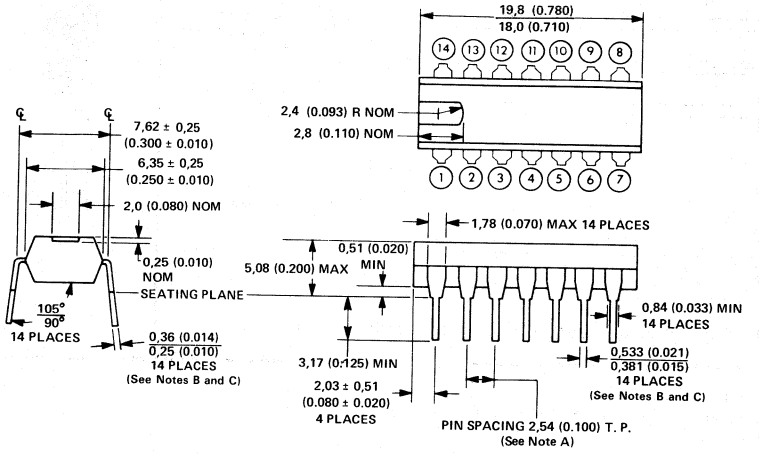
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

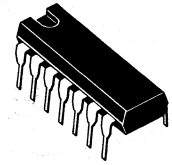
NOTES: A. Lead dimensions are not controlled in this area.
B. The shape, dimensions, and placement of the index mark is not guaranteed.

N014 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (see Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014





Falls Within JEDEC TO-116 and EIA MO-001AA Dimensions

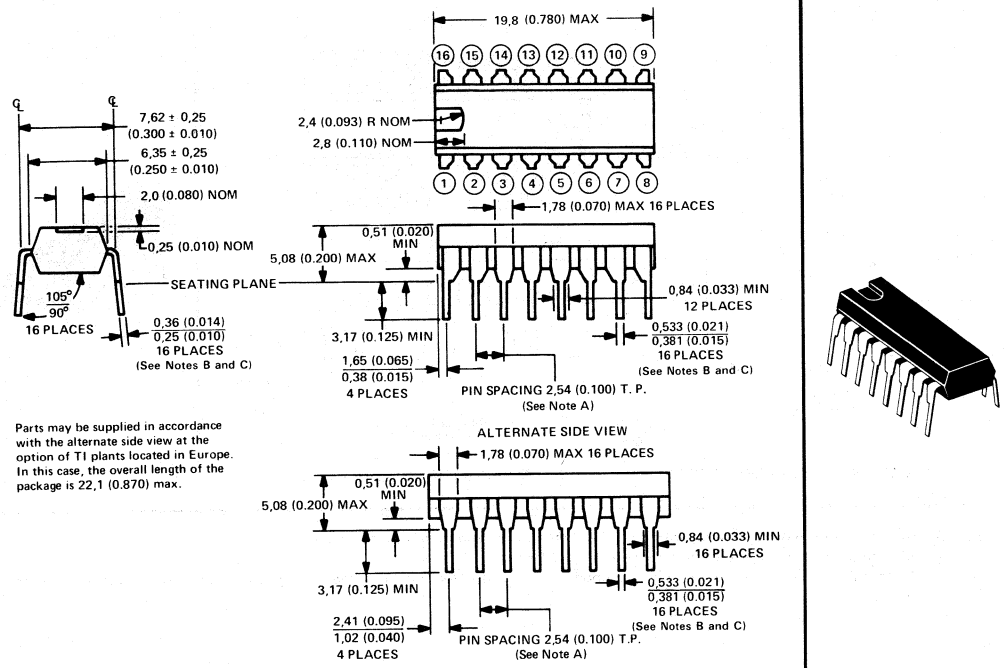
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N016 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N016

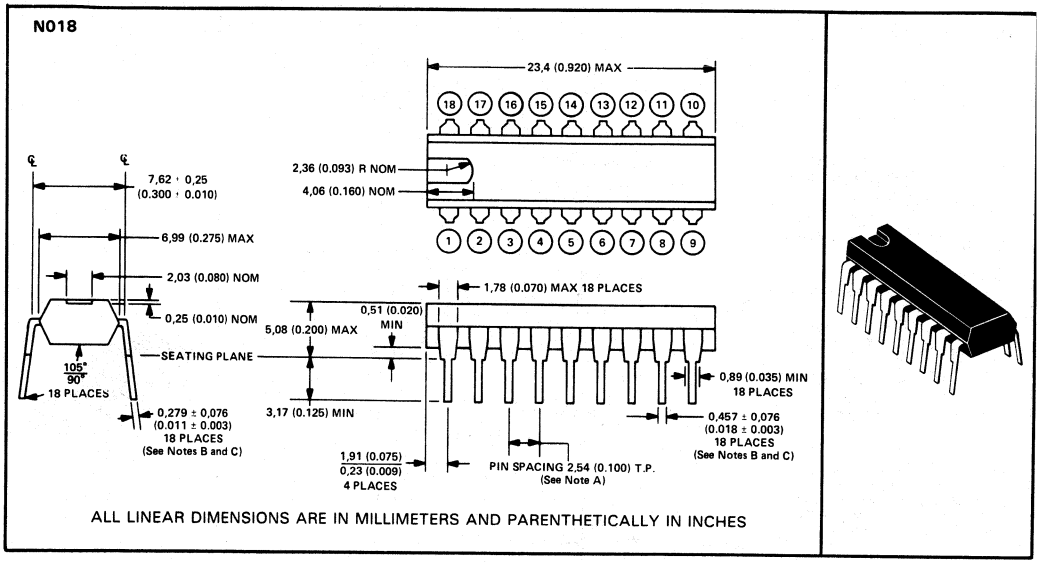


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N018 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

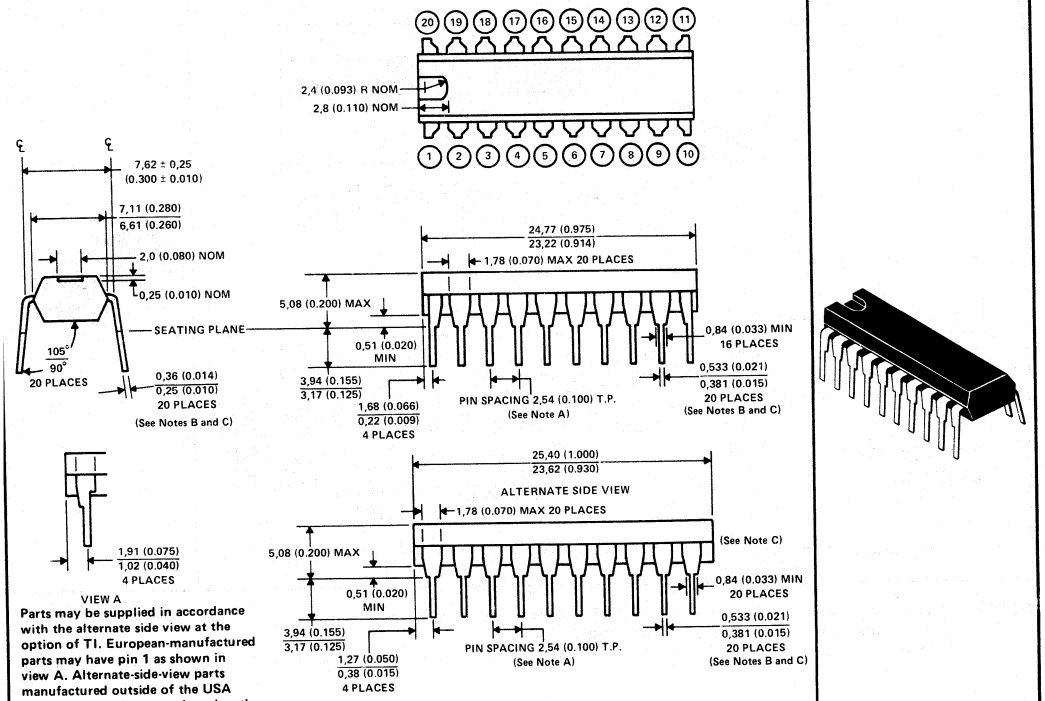


NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

020 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N020



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

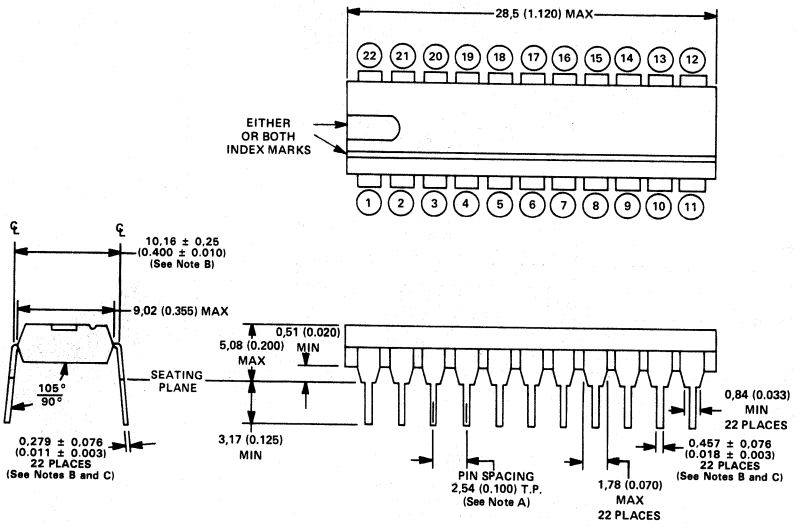
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

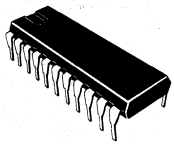
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N022 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electricall nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. Th package is intended for insertion in mounting-hole rows on 10,16 (0.400) centers. Once the leads ar compressed and inserted, sufficient tension is provided to secure the package in the board during soldering Leads require no additional cleaning or processing when used in soldered assembly.

N022



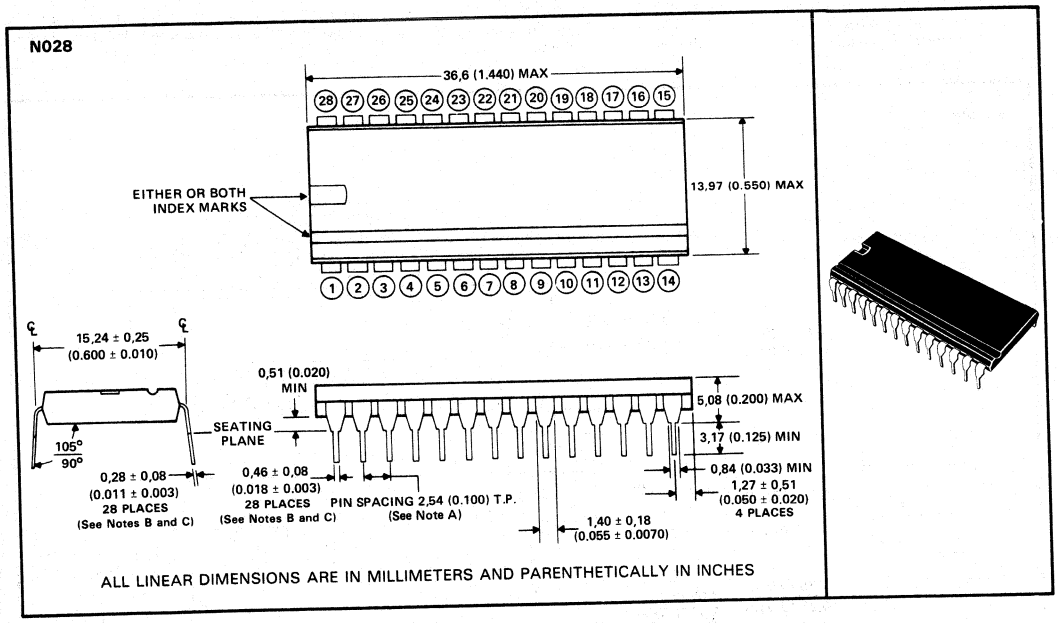


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



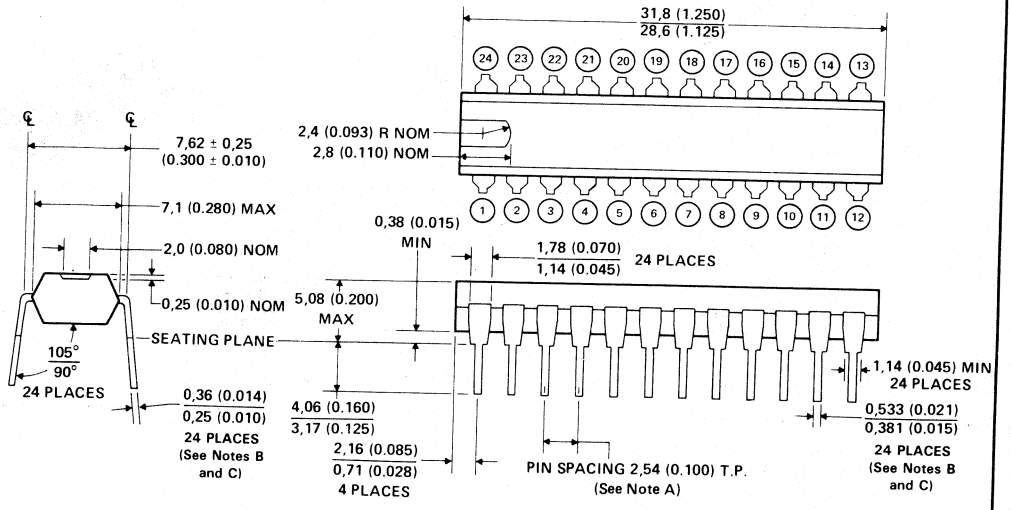
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 plastic dual-in-line package

This dual-in-line package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For all except 24-pin packages, the letter N is used by itself since only the 24-pin package is available in more than one row-spacing. For the 24-pin package, the 7,62 (0.300) version is designated NT; the 15,24 (0.600) version is designated NW. If no second letter or row-spacing is specified, the package is assumed to have 15,24 (0.600) row-spacing.

NT024



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane.

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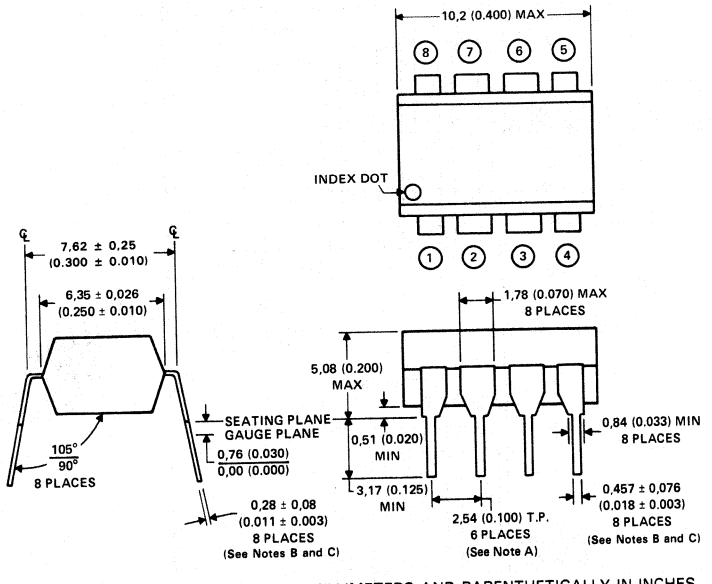
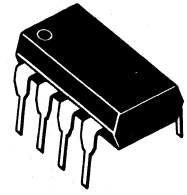
P008 dual-in-line plastic package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers (See Note A). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated leads require no additional cleaning or processing when used in soldered assembly.

P008



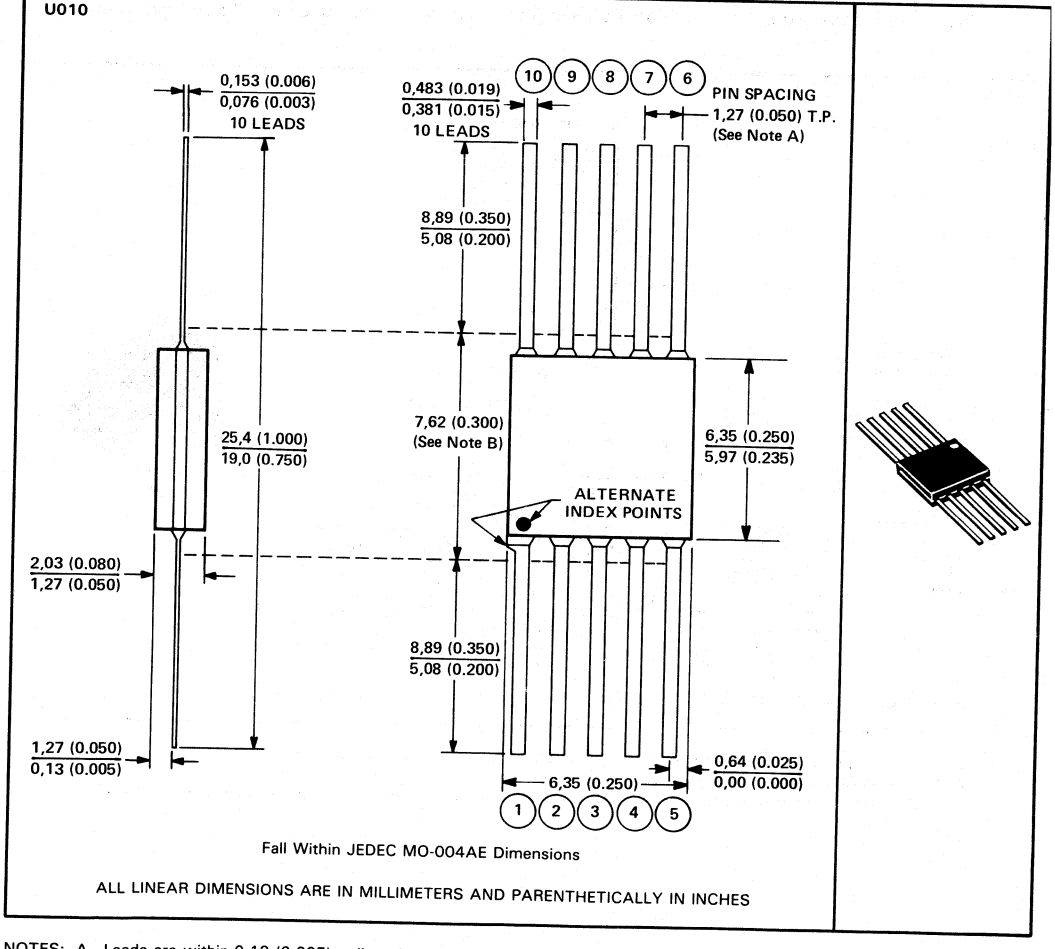


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

U010 ceramic flat package

This flat package consists of a ceramic base, ceramic cap, and lead frame. Circuit bars are alloy mounted. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.
B. This dimension determines a zone within which all body and lead irregularities lie.

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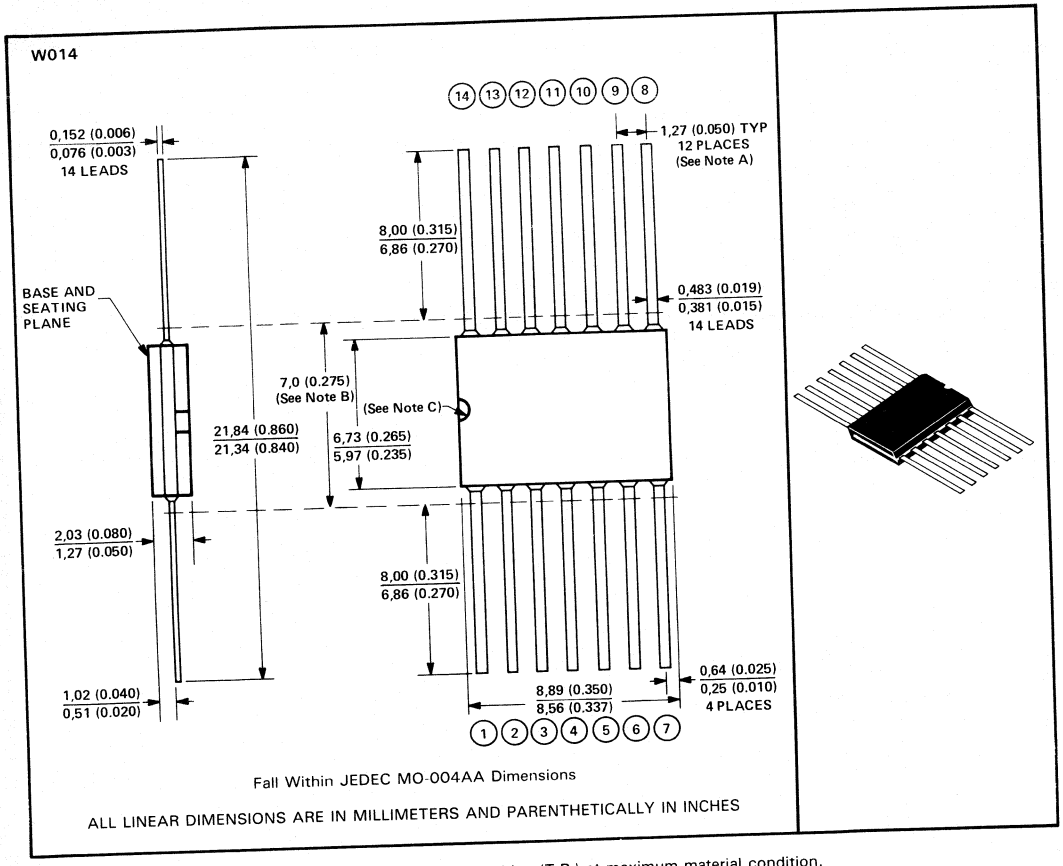
W014 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

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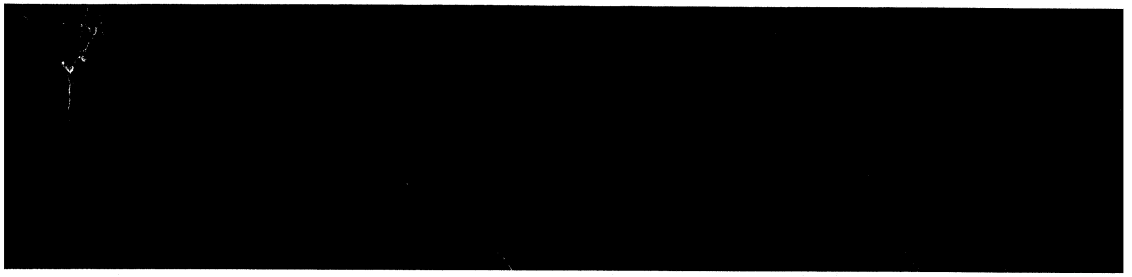
TAIWAN: Texas Instruments Supply Co., 9th Floor Bank Tower, 205 Tun Hwa N. Rd., Taipei, Taiwan, Republic of China, 2 + 713-9311.

UNITED KINGDOM: Texas Instruments Limited: Manton Lane, Bedford, MK41 7PA, England, 0234 270111.



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